3D electronics

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MIT Lincoln Laboratory-USA

3-D Integrated Circuit Fabrication Technology for High Density Electronics

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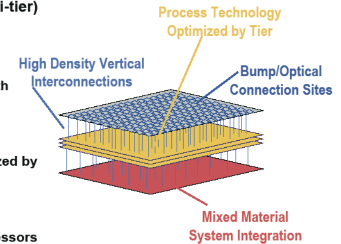
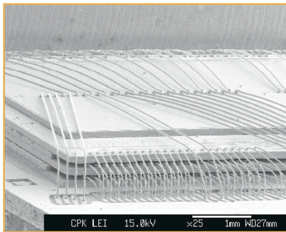
Motivation for 3-D Circuit Technology

- 3-D Circuit = Multi-layer (multi-tier) stacked circuit
- Advantages
  - Reduced interconnect length
  - Reduced chip size
  - Reduced parasitics
  - Reduced power
  - Fabrication process optimized by tier function
- Applications
  - High bandwidth microprocessors
  - Mixed material system integration
  - Advanced focal planes
    - Local computation and/or memory
    - 100% fill-factor diodes



Pad-Level "3D Integration"
Die Stacking

Stacked-Die Wire Bonding



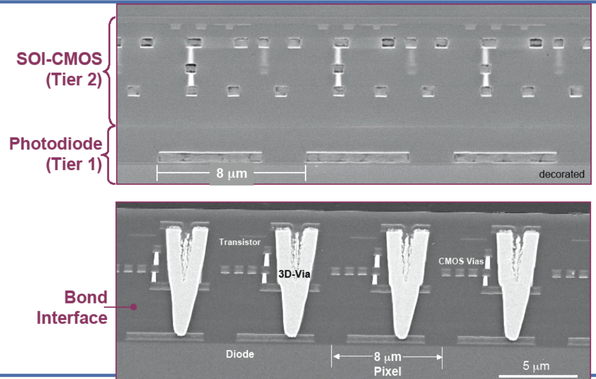
ChipPAC, Inc.

Stacked Chip-Scale Packages

Tessera, Inc.

In Production!

Pixel-Level 3-D Integration
Cross Sections Through Two-Tier Imager

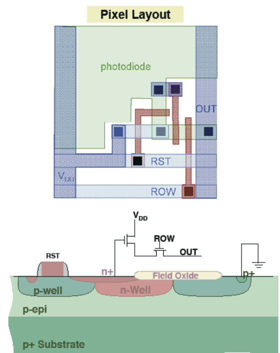


Outline

- Advantages of Vertical Integration for Focal Planes
  - MIT-LL Demonstration of Three-tier ring oscillators
- Fabrication Sequence
- MIT Lincoln Laboratory Demonstrations
  - Two-tier backside-illuminated visible imager
  - Three-tier laser radar focal plane
  - Three-tier 3-D IC Multiproject Run
  - Two-tier bonding and interconnection to InP detector material
- Summary

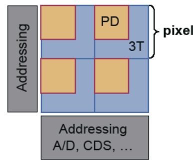
Limitations – Standard Bulk CMOS APS
Monolithic APS – MAPS

- Fill factor compromised
  - Photodetector and pixel transistors share same area
- Low photoresponsivity
  - Shallow junctions
  - High doping
  - Limited depletion depth
- High leakage
  - LOCOS/STI, salicide
  - Transistor short channel effects
- Substrate bounce and transient coupling effects



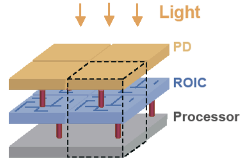
Advantages of Vertical Integration

Conventional Monolithic APS



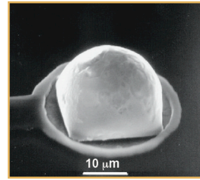
- Pixel electronics and detectors share area
- Fill factor loss
- Co-optimized fabrication
- Control and support electronics placed outside of imaging area

3-D Pixel

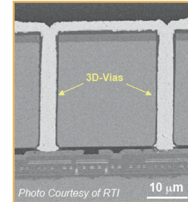


- 100% fill factor detector
- Fabrication optimized by layer function
- Local image processing
  - Power and noise management
- Scalable to large-area focal planes

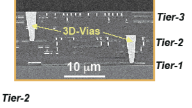
Approaches to 3D Integration
(Photos Shown to Scale)



Bump Bond used to flip-chip interconnect two circuit layers



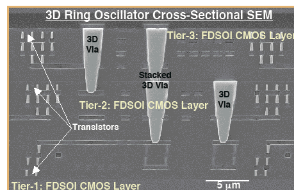
Two-layer stack with insulated vias through thinned ***bulk*** Si

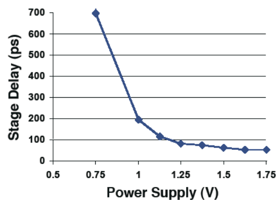


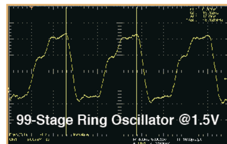
Three-layer circuit using Lincoln's SOI-based vias

3-Tier, 3D-Integrated Ring Oscillator
(DARPA 3DL1 *Multiproject Run*)

- Functional 3-tier, 3D-integrated ring oscillator
  - Uses all three active transistor layers, 10 levels of metal and experimental *stacked 3D-vias*
  - Demonstrates viability of 3D integration process







Outline

- Advantages of Vertical Integration for Focal Planes
- Fabrication Sequence and Five Key Elements
  - Low dark current photodiodes
  - Silicon on Insulator (SOI) circuits
  - Low-temperature, wafer-scale oxide-to-oxide bond
  - Precision overlay
  - High-density vertical interconnection
- MIT Lincoln Laboratory Demonstrations
  - Three-tier ring oscillators
  - Two-tier backside-illuminated visible imager
  - Three-tier laser radar focal plane
  - Three-tier 3-D IC Multiproject Run
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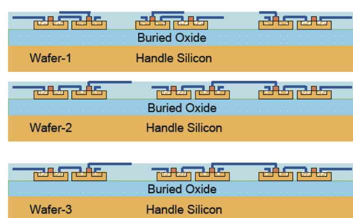
3-D Circuit Integration Flow-1

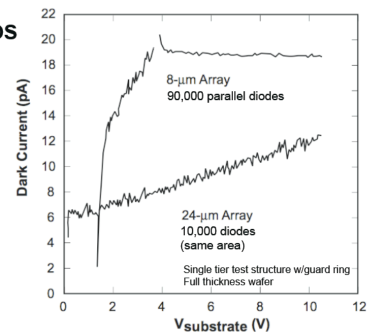
- Fabricate circuits on SOI wafers
  - SOI wafers greatly simplify 3D integration
- 3-D circuits of two or more active silicon layers can be assembled

Wafer-1 can be either Bulk, SOI, or Compound Semiconductor



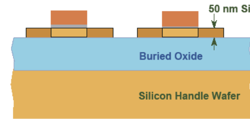
1. Low Dark Current Photodiodes

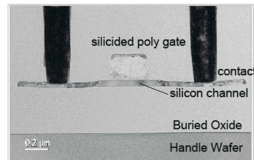
- Photodiode independent of CMOS
- High-resistivity substrates
- Back-illumination process
- Photodiode leakage <0.2nA/cm^2 @ 25ºC
- Similar results after 3D-stacking



2. Silicon-On-Insulator Circuits

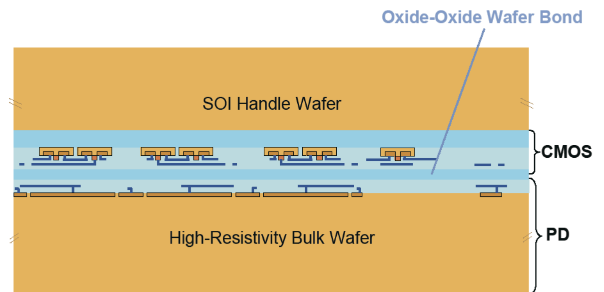
- 3.3-V, 350-nm gate length, fully depleted SOI CMOS
- Buried oxide
  - Dielectric isolation
  - Reduced parasitic capacitances
  - Enhanced radiation performance
  - Essential wafer-thinning etch stop





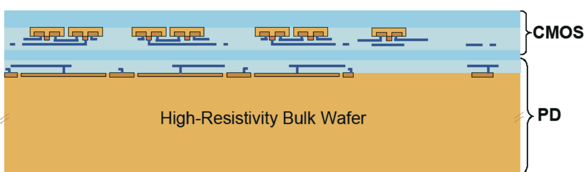
3-D Circuit Stacking

- Invert, align, and bond Tier 2 to Tier 1



3-D Circuit Stacking

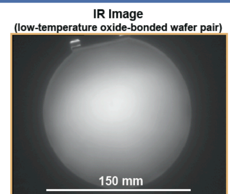
- Remove handle silicon from Tier-2



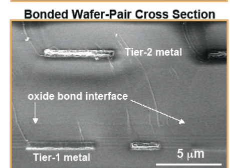
3. Low Temperature Oxide Layer-to-Layer Bonding

- Deeply scaled 3-D interconnect technology requires robust wafer-to-wafer bonding technology
- MIT-LL low temperature oxide bonding process provides
  - Thin and controllable bondline
  - Enables use of standard IC high aspect ratio contact etch and plug fill technologies
    - ~475ºC process
  - Allows for 3-D interconnect to be sintered
  - Standard, high reliability semiconductor material

IR Image
(low-temperature oxide-bonded wafer pair)



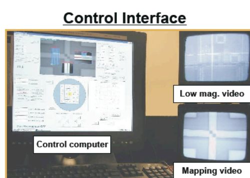
Bonded Wafer-Pair Cross Section

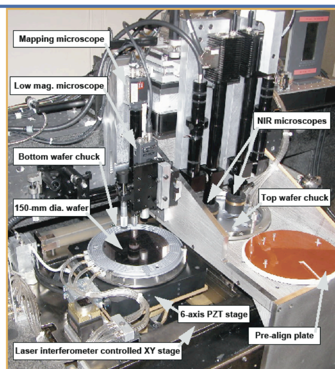


4. Precision wafer-to-wafer overlay

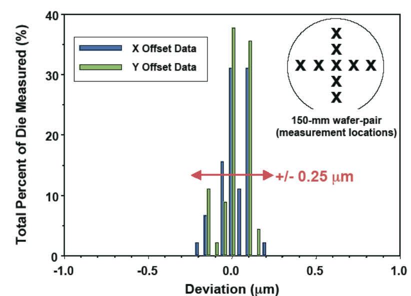
- Provide a wafer-to-wafer alignment accuracy compatible with a submicron 3D Via
- Tool based on modern IC wafer stepper technology
- 0.5 μm 3-sigma overlay demonstrated

Control Interface



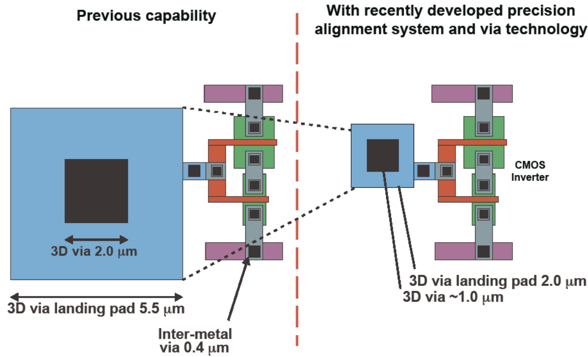


Repeatability Data MIT-LL Precision Aligner

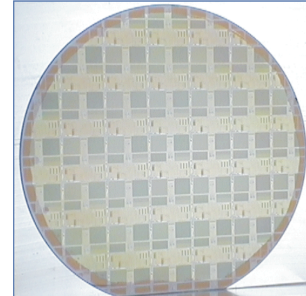


- Data from five repeated alignments of same wafer pair
- Nine die measured per alignment

3D Via Layout Comparison
(Based on MIT-LL 180nm FDSOI CMOS rules)



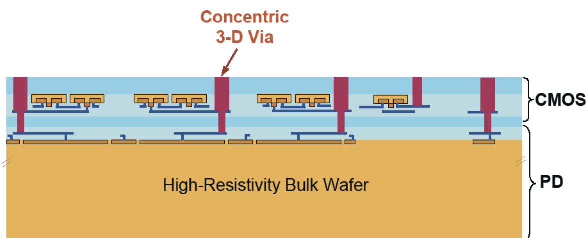
Bonded Two Wafer Imager Stack



150-mm Diameter Wafer Pair

Inter-Tier Via Connections

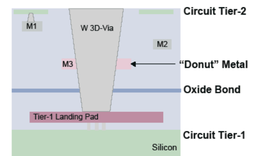
- Pattern, etch, and fill 3-D vias
- (Additional circuit tiers could be added)

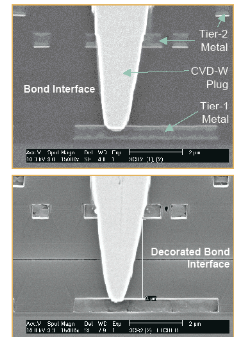


5. High Density, High Yield, Compact 3D-Via

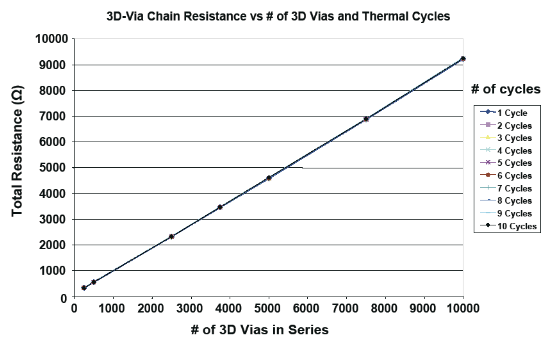
- Leverages standard high-yield IC process technology for 3D interconnection
  - High density plasma oxide etch of via hole
  - Chemical vapor deposition of tungsten plug
  - Chemical mechanical planarization (CMP) to form damascene plug

3D Via Cross-sections



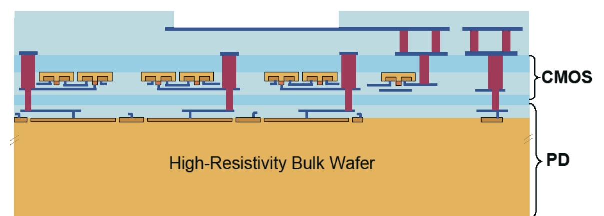


Thermal Cycle Effects on 3D-Via Chains
Thermal Cycle: 300 K/ 77 K/ 300 K



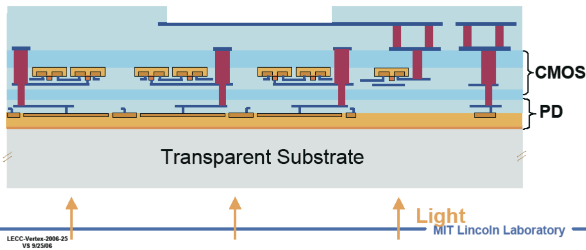
Back Metal-1 and Back Metal-2

- Deposit and pattern Back Metal-1
- Deposit and CMP ILD
- Deposit and pattern Back Metal-2
- Sinter



Completed Back-Illuminated CMOS Imager

- Thin photodiode substrate to 50μm
- Epoxy bond to quartz

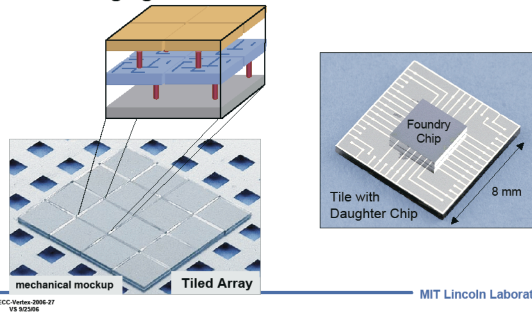


Outline

- Advantages of Vertical Integration for Focal Planes
- Fabrication Sequence
- MIT Lincoln Laboratory Demonstrations
  - Three-tier ring oscillators
  - **Two-tier backside-illuminated visible imager**
  - Three-tier laser radar focal plane
  - Three-tier 3-D IC Multiproject Run
  - Two-tier bonding and interconnection to InP detector material
- Summary

Four-Side Abuttable Goal

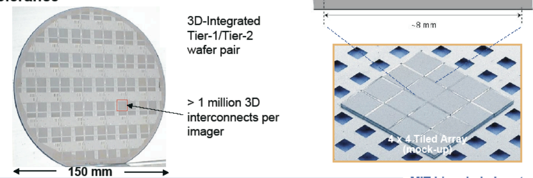
- 3-D CMOS imagers tiled for large-area focal planes
- Foundry fabricated daughter chip bump bonded to non-imaging side



Four-Side Abuttable Vertically Integrated Imager

- Silicon photodetector layer (Tier-1)
  - Four-side abuttable 1024 x 1024 array of 8μm x 8μm pixels
- Address and readout layer (Tier-2)
  - 3.3 volt FDSOI CMOS layer
- Timing, control, and analog-to-digital electronics (Tier-3)
  - MOSIS fabricated chip bump bonded to detector array
- Active-pixel architecture for radiation tolerance

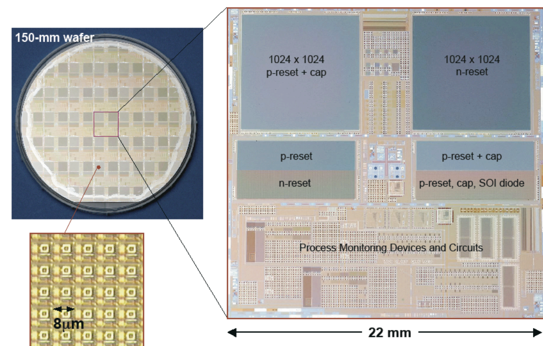
Light
Transparent Support Layer
Photodetector Array
FDSOI CMOS
Bias & Master Clock
Control Logic & Clock Generation
Output



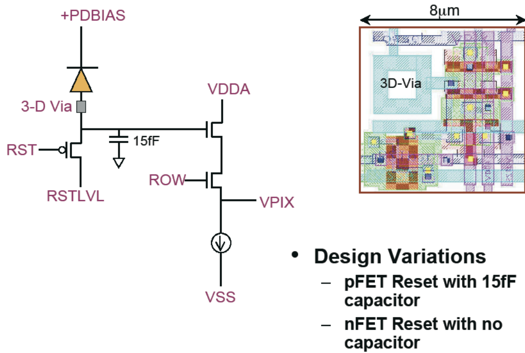
Design Goals

- Four-side abuttable Active Pixel Sensor
- 1024 x 1024 array of 8μm x 8μm pixels
- 3-D interconnections per pixel
- 3.3-V operating voltage
- Full digital control and readout at 10 fps

Completed 3D-Stacked Imager Wafer and Die Layout

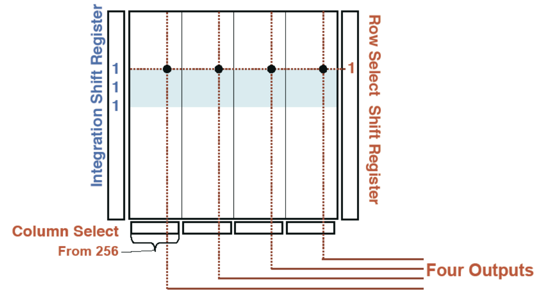


3T Pixel Schematic and Layout



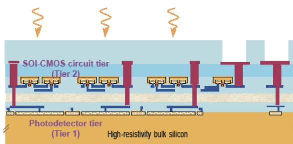
- **Design Variations**
  - pFET Reset with 15fF capacitor
  - nFET Reset with no capacitor

1024 x 1024 Imager Array Architecture



Preliminary Tier-1-2 3D Imager Test Results

- Electrical probe station preliminary imager test result using *frontside* illumination
  - Final processing steps will result in unobstructed backside illuminated device



**35-mm slide image projected through CMOS-circuit-side of 3D-integrated imager on chip test station*

1024 x 1024 Image
from *FIRST* 3D-Integrated Wafer Pair*

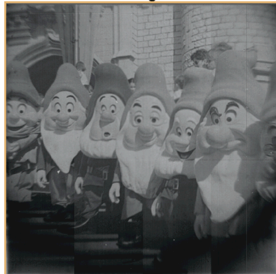


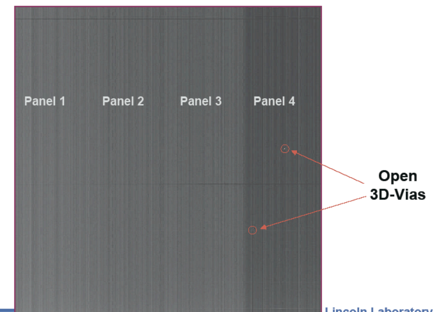
Image acquired at 10 frames/sec
(Background Subtracted, Pixel Yield > 99.9%, 3.8M transistors)

Presented at 2005 ISSCC

Sample Dark Background

- Raw image without fixed pattern noise suppression
- Dominant yield detractor is row/column drop-outs

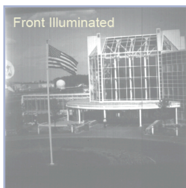
Four Analog Outputs

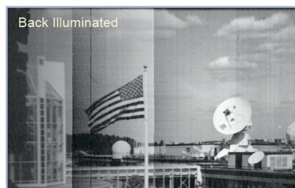


Open 3D-Vias

Four-Side Abuttable Vertically Integrated Imaging Tile

- Wafer-Scale 3D circuit stacking technology
  - Silicon photodetector tier
  - SOI-CMOS address and readout tier
    - Per-pixel 3D interconnections
  - 1024 x 1024 array of 8 µm x 8 µm pixels
  - 100% fill factor
  - >1 million vertical interconnections per imager





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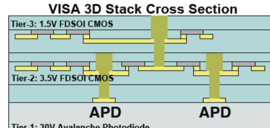
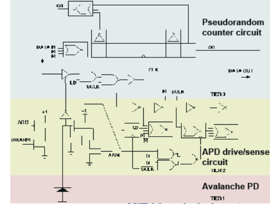
Three-Tier Laser Radar Focal Plane

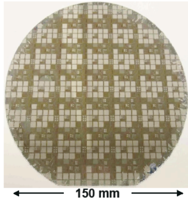
- Based on single-photon-sensitive Geiger-mode avalanche photodiodes
  - 64 x 64 demonstration circuit (scalable to large imager formats)
  - Pixel size reduction from 100 µm to 30 µm
  - Timing resolution reduction from 1 ns to 0.1 ns
  - 100x reduction in voxel volume

VISA 3D Stack Cross Section



VISA APD Pixel Circuit (~250 transistors/pixel)

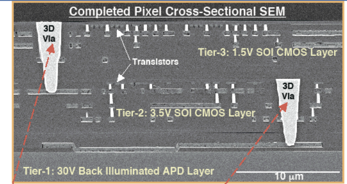




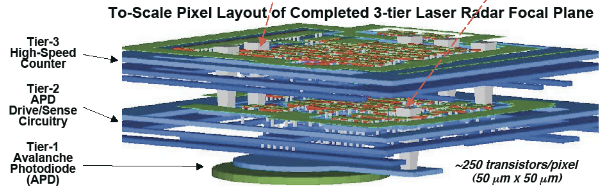
Completed Backside-illuminated 3-tier, 3D Laser Radar wafer

Functional 3D-Integrated, 3-Tier Avalanche Photodiode Focal Plane

- *VISA* laser radar focal plane based on single-photon-sensitive Geiger-mode avalanche photodiodes
  - 64 x 64 format
  - 50-µm pixel size



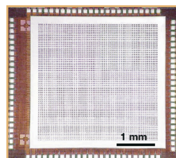
To-Scale Pixel Layout of Completed 3-tier Laser Radar Focal Plane



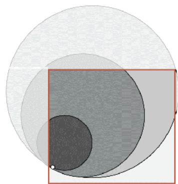
Presented at 2006 ISSCC

64x64 LADAR Focal Plane
First Demonstration of 3-Tier Focal Plane

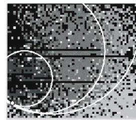
- Rudimentary ladar image of 28” long cone with 8-in timing resolution
  - Timing circuit limited to only 9-bits of its full 12-bit range



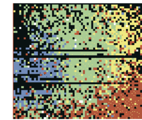
Complete 3-tier, back-illuminated 64 x 64 APD Laser Radar



Orientation of cone image on focal plane



Grayscale range image with superimposed contours



False color range image

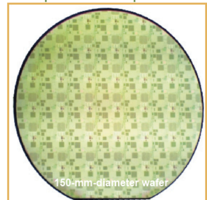
Outline

- Advantages of Vertical Integration for Focal Planes
- Fabrication Sequence
- MIT Lincoln Laboratory Demonstrations
  - Three-tier ring oscillators
  - Two-tier backside-illuminated visible imager
  - Three-tier laser radar focal plane
  - Three-tier 3-D IC Multiproject Run
  - Two-tier bonding and interconnection to InP detector material
- Summary

3-D IC *Multiproject Run* Completed
(Three 180-nm, 1.5 volt FDSOI CMOS Tiers)

- MIT-LL 3D circuit integration technology
- Preliminary 3D design kits developed
  - Mentor Graphics – *MIT-LL*, Cadence – *NCSU*, Thermal Models – *CFRDC*
- Design guide release 11/04, fab start 6/05, 3D-integration complete 3/06

Wafer photo of completed tier-1



Concepts being explored in run:

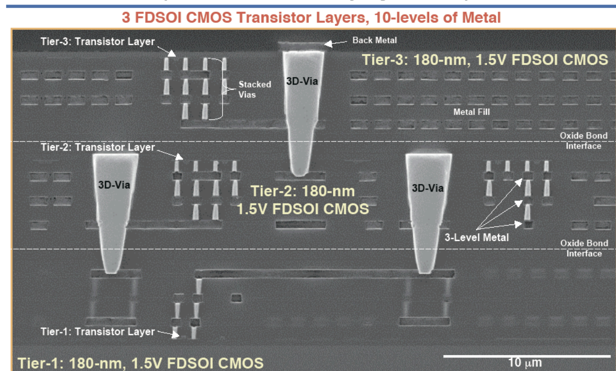
3D FPGAs, digital, and digital/mixed-signal/RF
ASICs exploiting parallelism of 3D-interconnects
3D analog continuous-time processor
3D-integrated S-band digital beam former
Stacked memory (SRAM, Flash, and CAM)
Self-powered CMOS logic (scavenging)
Integrated 3D Nano-radio and RF tags
Intelligent 3D-interconnect evaluation circuits
DC and RF-coupled interconnect devices
Low Power Multi-gigabit 3D data links
Noise coupling/cross-talk test structures and circuits
Thermal 3D test structures and circuits

3DL1 Participants (Industry, Universities, Laboratories)

BAE	Lincoln Laboratory	Purdue
Cornell	Maryland	RPI
Delaware	Minnesota	Stanford
HRL	MIT	Tennessee
Idaho	North Carolina State	UCLA
Johns Hopkins	NRL	Washington
LPS	Pennsylvania	Yale

Cross-Section of 3-Tier 3D-integrated Circuit
(DARPA 3DL1 *Multiproject Run*)

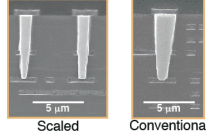
3 FDSOI CMOS Transistor Layers, 10-levels of Metal



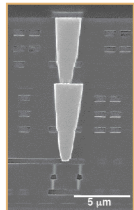
3D Technology Improvements
(DARPA 3DL1 *Multiproject Run*)

- 3D technology enhancements successfully demonstrated in 3DL1 Run
  - Stacked 3D-vias for electrical and thermal interconnect
  - 2X reduction in 3D-via size
  - Improved tier-to-tier overlay

High-Yield on >5000-link Scaled 3D-via Chains



Scaled Conventional



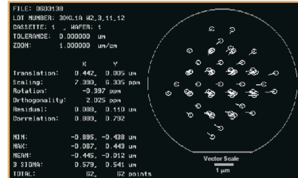
Stack 3D-vias demonstrated

>95% yield on 4800 link chains

Stacked 3D-via resistance ~1Ω

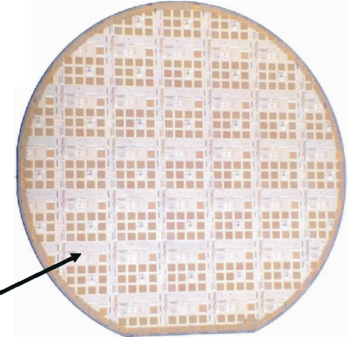
Can be used as thermal vias

~0.5 µm 3σ Tier-to-Tier Registration



Silicon to InP Wafer Bonding

- Successful demonstration of 3D-bonding of SOI CMOS circuit layer to InP handle wafer
- Enables extension of 3D-integration technology to higher density, longer wavelength focal plane detectors
  - Tight pixel-pitch IR focal planes and APD arrays
  - InGaAsP (1.06-µm), InGaAs (1.55-µm)



150-mm-diameter InP Wafer

Summary

- MIT Lincoln Laboratory-developed 3D circuit integration technology has been applied to advanced focal planes and three-tier computational circuits
- Successful demonstrations:
  - Two-tier visible imager: 1024x1024 array of 8µm x 8µm pixels integrated to 100% fill factor photodiodes, backside illuminated
  - Three-tier ring oscillators in 180-nm gate length technology
  - Three-tier laser radar focal plane: 64x64 array of Geiger-mode avalanche photodiodes with per-pixel timing and bias circuitry
  - Three-tier 3-D IC Multiproject Run in 180-nm gate length technology
  - Two-tier bonding and interconnection to SWIR-sensitive detector materials (InP)