Contribution ID: **88** Type: **Poster**

n-XYTER - A CMOS read-out ASIC for a new generation of high rate multichannel counting mode neutron detectors

Wednesday, 27 September 2006 16:20 (25 minutes)

For a new generation of 2-D neutron detectors developed in the framework of the EU NMI3 project DETNI [8], the 128-channel frontend chip n-XYTER has been developed. To facilitate the reconstruction of single neutron incidence points, the chip has to provide a spatial coordinate (represented by the channel number), as well as time stamp and amplitude information to match the data of x- and y-coordinates. While the random nature of the input signals call for self-triggered operation of the chip, on-chip derandomisation and sparsification is required to exploit the enormous rate capability of these detectors (up to 10ˆ5/s/channel). The chosen architecture implements a preamplifier driving two shapers with different time constants per channel. The faster shaper drives a single-pulse discriminator with subsequent time-walk compensation. The output of this circuit is used to latch a 14-bit time stamp with a 2ns resolution and to enable a peak detector circuit fed by the slower shaper branch. The analogue output of the peak detector as well as the time stamp are fed to a 4-stage FIFO for derandomisation. The readout of these FIFOs is accomplished by a token-ring based multiplexer working at 32MHz, which accounts for further derandomisation, sparsification and dynamic bandwidth distribution. The chip will be submitted for manufacturing in AMS's C35B4M3 0.35um CMOS technology in June 2006.

Summary

In the framework of the EU NMI3 project DETNI [8] a new generation of detectors for imaging and time-of-flight applications with neutrons is under development. The project targets the realisation of three different high rate, solid neutron converter based detectors, one of which is a double-sided Silicon micro-strip detector, coupled to a Gadolinium neutron-converter layer (Si-MSD). The other two detector types are gas based: The "Cascade" GEM detector using a Boron converter and a Hybrid-MSGC detector with Gd-converter. Either one of the detectors is characterised by a comparatively high number of readout channels per coordinate (up to 640 x 640 for the Si-MSD) and a specified event-rate, unprecedented in single event counting neutron or X-ray detection technology.
To accomplish the readout of these detectors the 128-channel n-XYTER readout ASIC has been developed. It will allow determining both, time of incidence as well as pulse height of the detected signals. The former will allow localising the point of conversion of neutrons through coincidence on both coordinates, the latter serves to further enhance spatial resolution through centre of gravity calculation on one hand and to realise X-ray background discrimination on the other hand. Particular attention is paid to address the statistical nature of the incoming signals in the purely data driven acquisition architecture.
Either one of the DETNI detectors is inherently capable of enormous neutron conversion rates. The targeted rate capability for these detectors will entirely be limited by the bandwidth of readout electronics and time resolution, which determines coincidence resolution for position correlation. With an expected neutron conversion rate of 100MHz on the detector, each signal needs to be tagged with a 2ns resolution. Further, as neutron data is statistical in nature, and readout bandwidth limited, a derandomization scheme together with a sparsification concept needs to be employed. To achieve these goals, the chosen architecture implements a charge-sensitive preamplifier for ultra low-noise and wide dynamic range. It drives two shaper stages with different time constants per channel. The time constant of the faster shaper was chosen just long enough to completely integrate the signal of a silicon sensor. It drives a single-pulse discriminator with subsequent time-walk compensation. The

latter is required to restrict the amplitude-dependent time walk of the discriminator to less than 2ns. The output of this circuit is used to latch a 14-bit time stamp from a 500MHz grey code counter and to enable an auto-resetting peak detector circuit fed by the slower shaper branch. The noise of the discriminator readout path is expected to be only ˜1000e with a 30pF detector, which together with threshold correction on a per-channel basis will ensure a sufficient S/N ratio without compromising efficiency. The analogue output of the peak detector as well as the time stamp are fed to a 4-stage FIFO for derandomisation. The readout of these FIFOs is accomplished by a token-ring based multiplexer working at 32MHz, which accounts for further derandomisation, sparsification and dynamic bandwidth distribution. Due to the unique properties of this architecture, implementations with a lower number of channels, targeted for applications with even higher rates, are also planned.
We present the scientific output of an evaluative prototype together with the design and implementation of the first full scale version. realised in silicon on the AMS 0.35um C35B4M3 process.

[8] (http://jra1.neutron-eu.net/jra1)

Primary author: TRUNK, Ulrich (Max-Planck-Institut f. Kernfphysik)

Co-authors: BROGNA, Andrea (Physikalisches Institut, Universität Heidelberg); Prof. GEBAUER, Burckhard (Hahn-Meitner-Institut, Berlin); SCHMIDT, Christian (Gesellschaft für Schwerionenforschung, Darmstadt); SOLTVEIT, Hans Kristian (Physikalisches Institut, Universität Heidelberg); KLEIN, Martin (Physikalisches Institut, Universität Heidelberg); WIACEK, Piotr (AGH University of Science and Technology, Krakow); SZCZYGIEL, Robert (Institute of Nuclear Physics, Polish Academy of Sciences, Krakow); BUZZETTI, Siro (INFM & Politecnico di Milano); FIUTOWSKI, Thomasz (University of Science and Technology, Krakow); Prof. DABROWSKI, Wladyslaw (AGH University of Science and Technology, Krakow)

Presenter: TRUNK, Ulrich (Max-Planck-Institut f. Kernfphysik)

Session Classification: Poster sessions