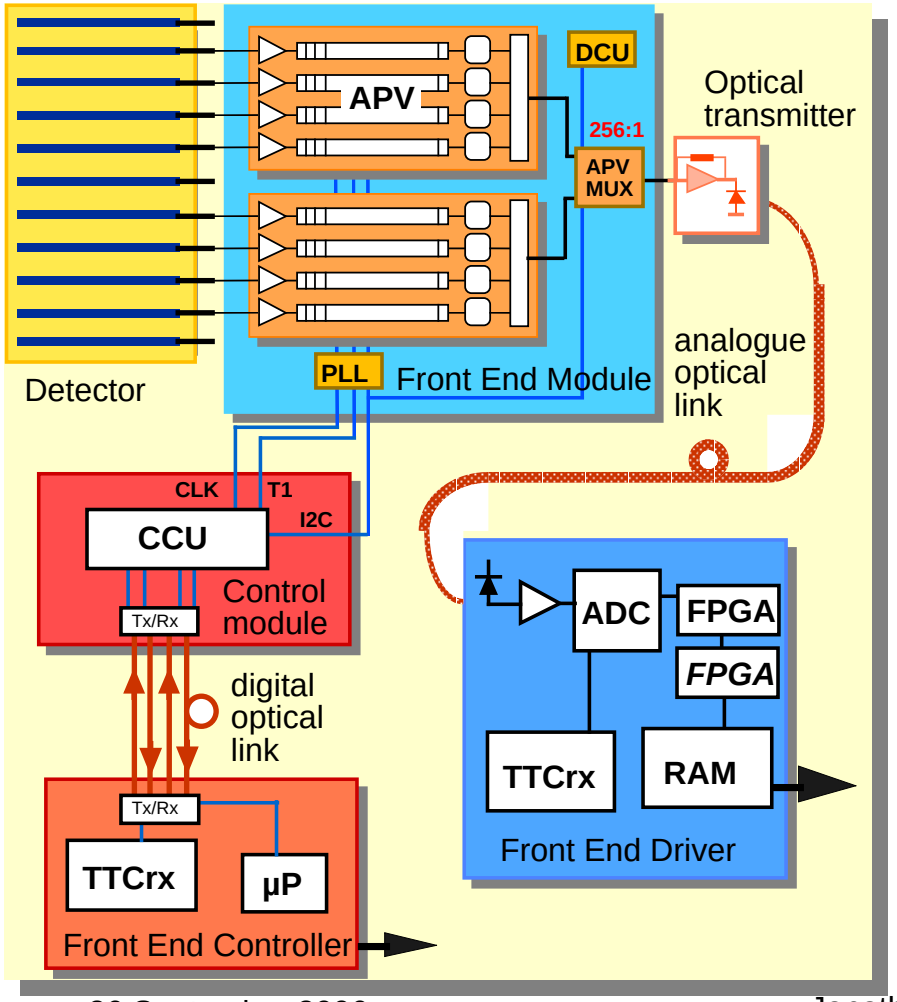
Tracker Fed DAQ Tests In 904

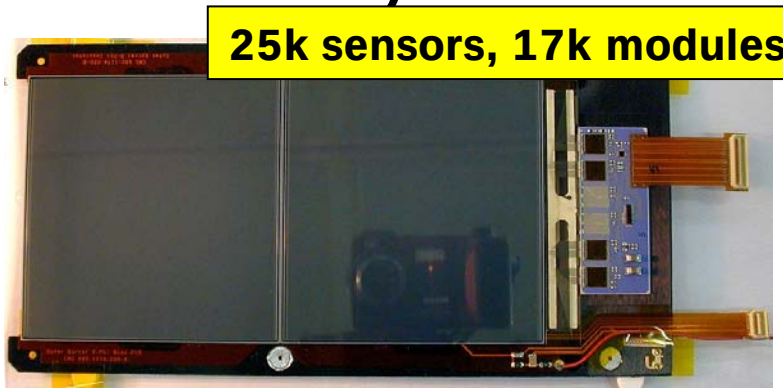
J. Fulcher

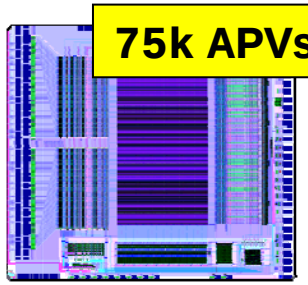
Imperial College

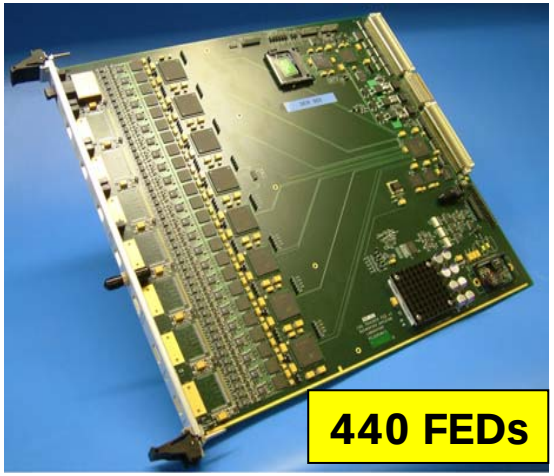
Control and Readout Systems

Silicon strip tracker has 10M channels!



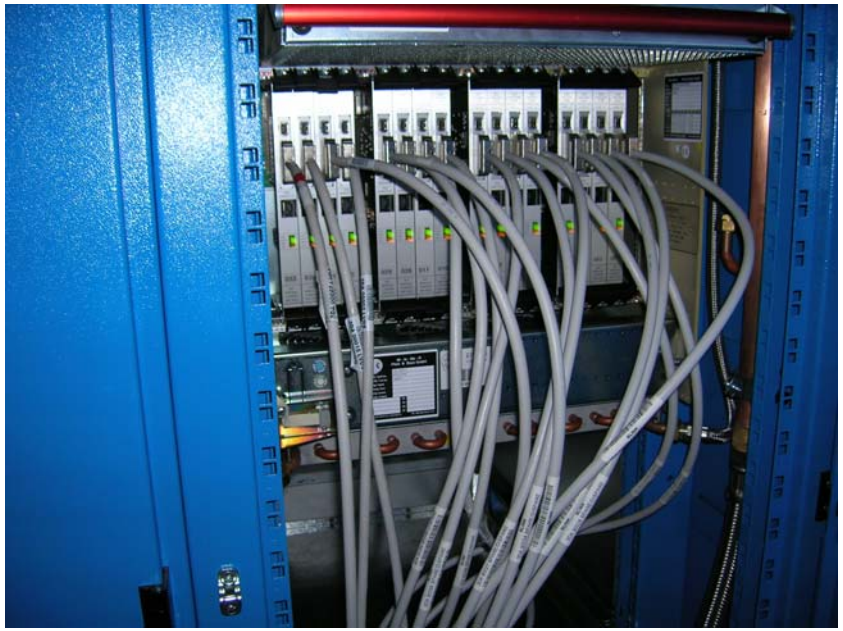






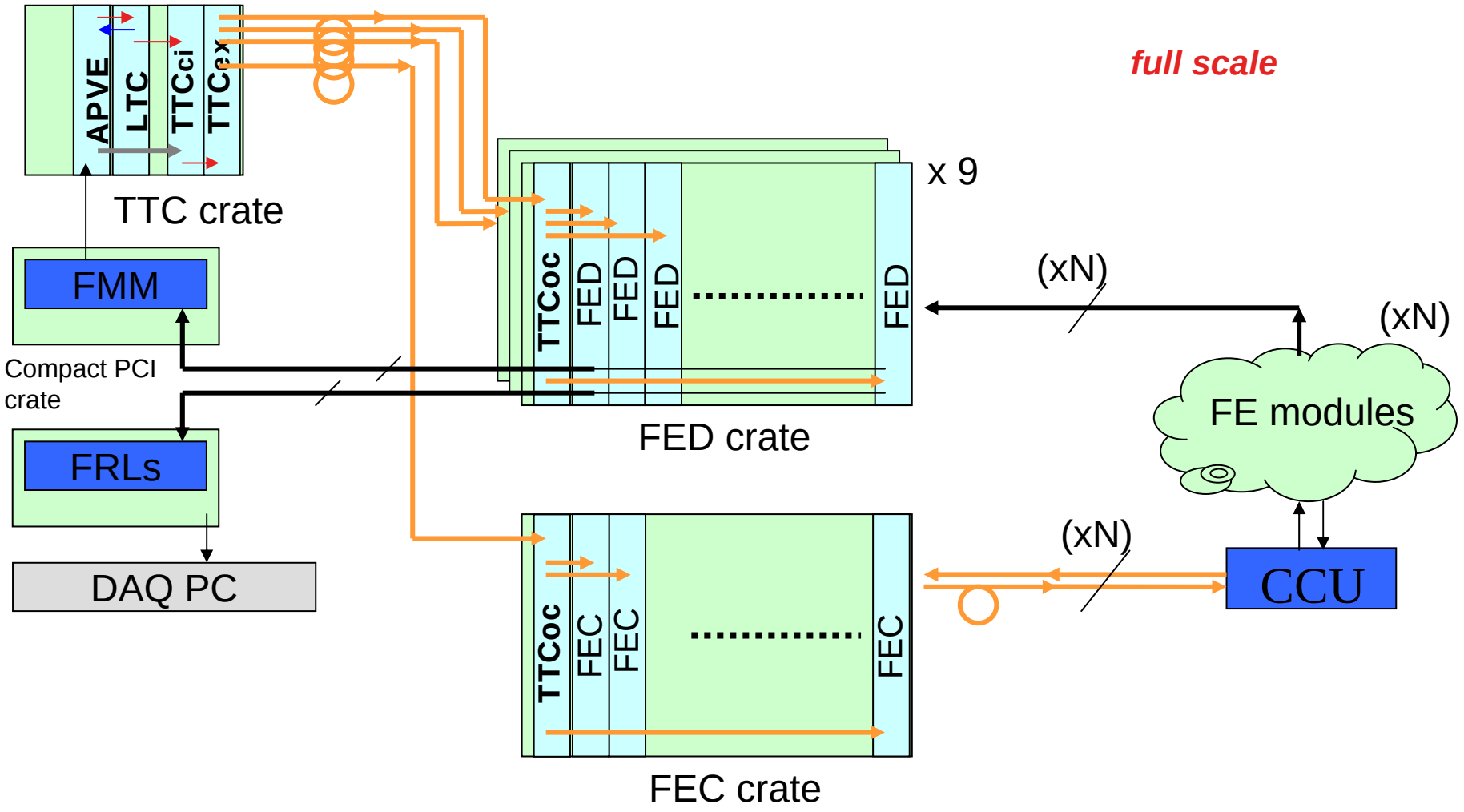
Tracker FED Racks in open area

Final system is coming together...



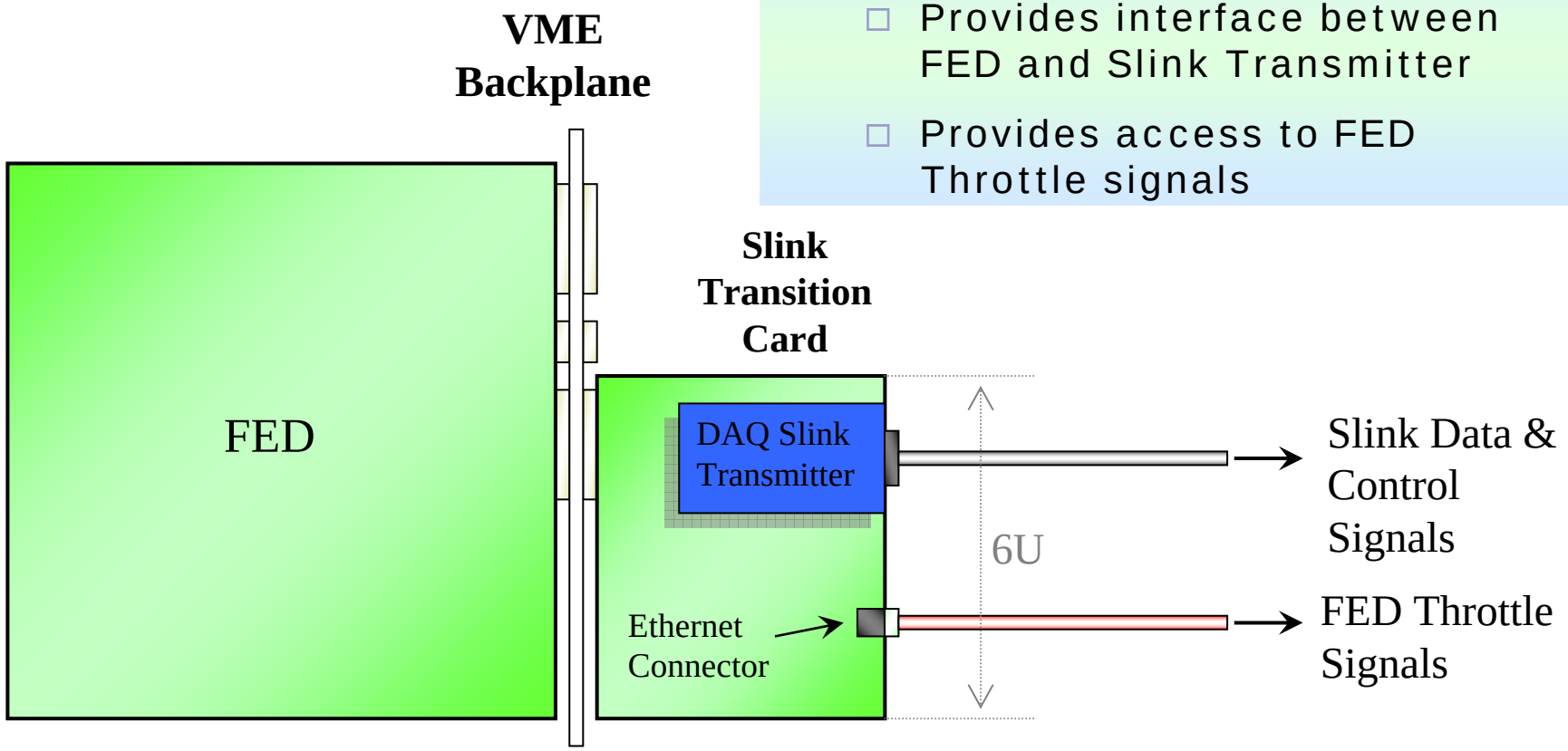
Rear of Crate showing
6U Transition cards with SLINK cables

Full System setup in CERN B904

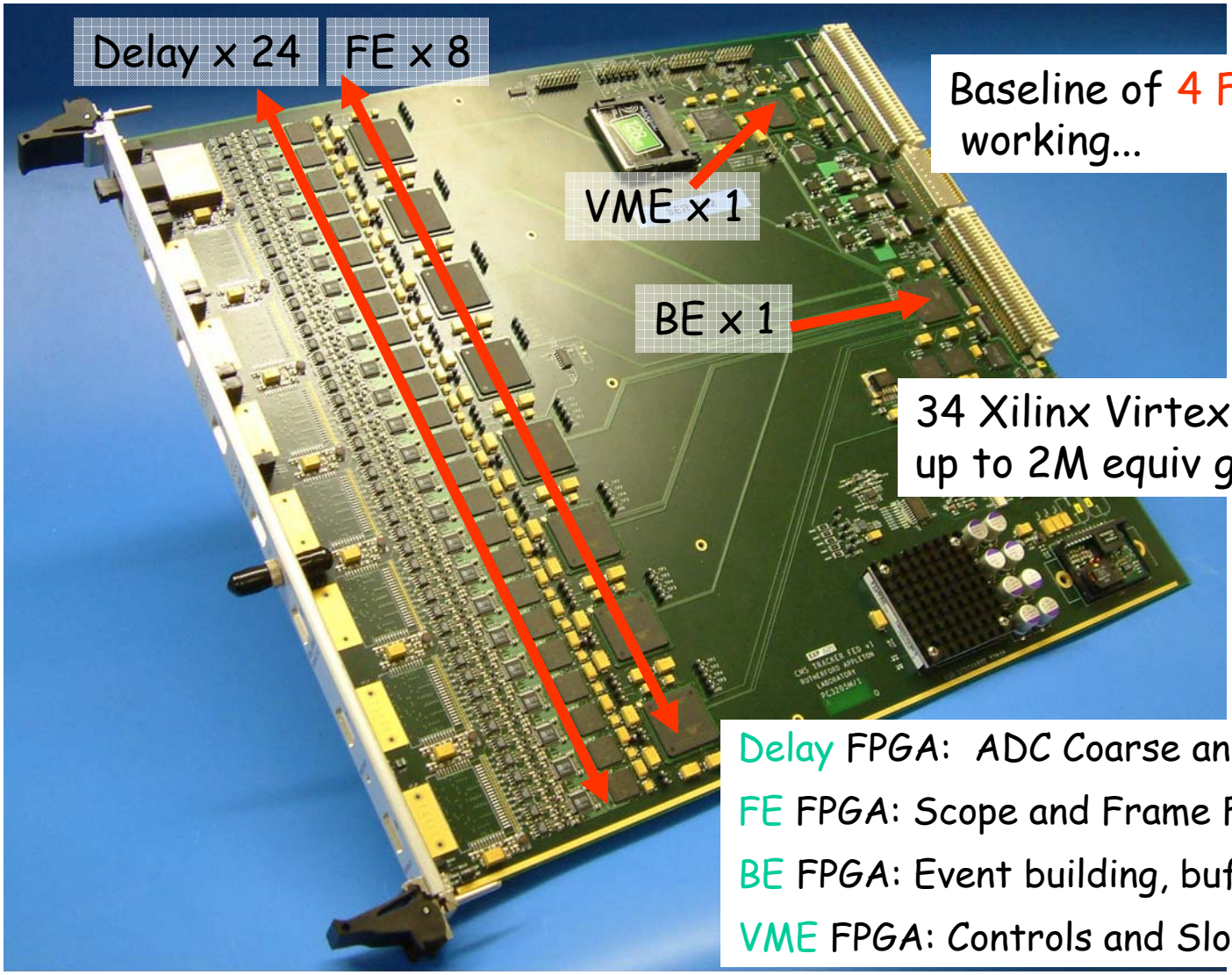


S-LINK VME Transition Card

- Simple 6U board:
  - Provides interface between FED and Slink Transmitter
  - Provides access to FED Throttle signals



Transition Cards out to manufacture back for test in September.
(compatible with both FEDv1 and FEDv2)



Baseline of 4 FPGA Final Designs working...

34 Xilinx Virtex II FPGAs
up to 2M equiv gates each

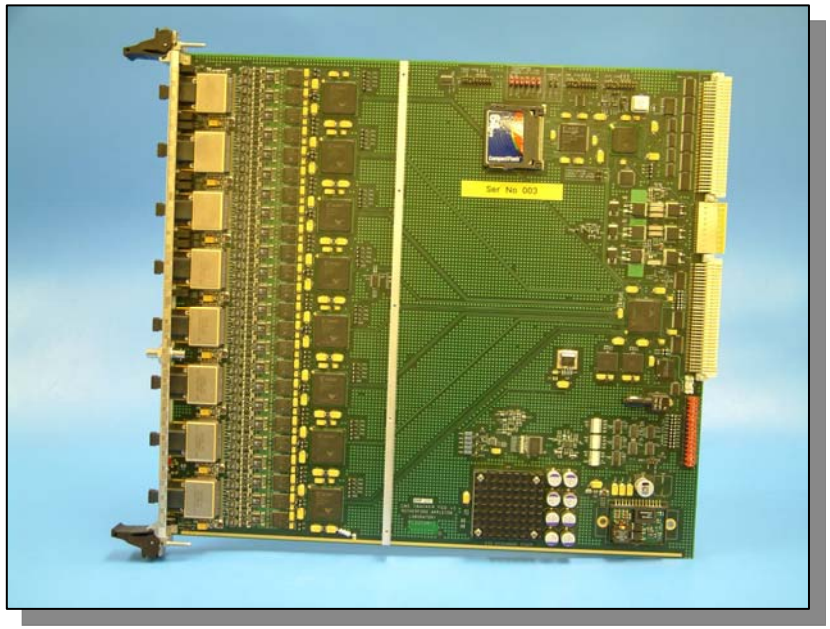
Delay FPGA: ADC Coarse and Fine Clock Skewing.

FE FPGA: Scope and Frame Finding modes.

BE FPGA: Event building, buffering and formatting.

VME FPGA: Controls and Slow Readout path.

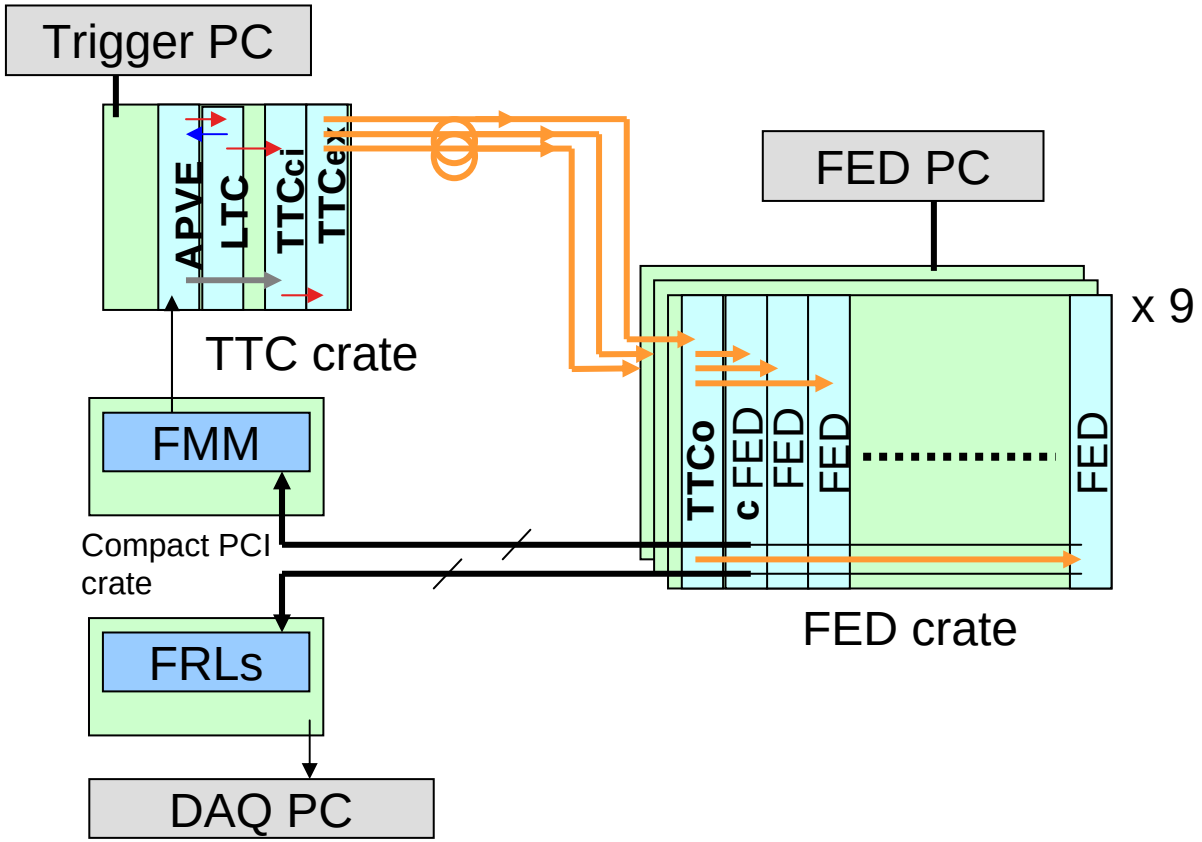
No Need for Cables! Fake Events are dead easy!



QuickTime™ and a
TIFF (Uncompressed) decompressor
are needed to see this picture.

2 Crate FRL Test - Hardware:

- 2 Crates:
  - 30 * FED
  - 2 * TTCoc
- 1 Crate with
  - 15 * FRL
  - 2 * FMM
- 1 Crate with
  - 1 * APVE
  - 1 * LTC
  - 1 * TTCci
  - 1 * TTCex



Configuration

- LTC set as trigger controller
  - Simulated Poisson Triggers at any rate
  - Throttled via APVE
- TTCci set as messenger
- FRLs in merging mode with maximum throughput per channel of ~ 230 MBytes/s
- FEDs
  - Random Fake Event Zero Suppression mode
  - occupancies from 1% - 50%

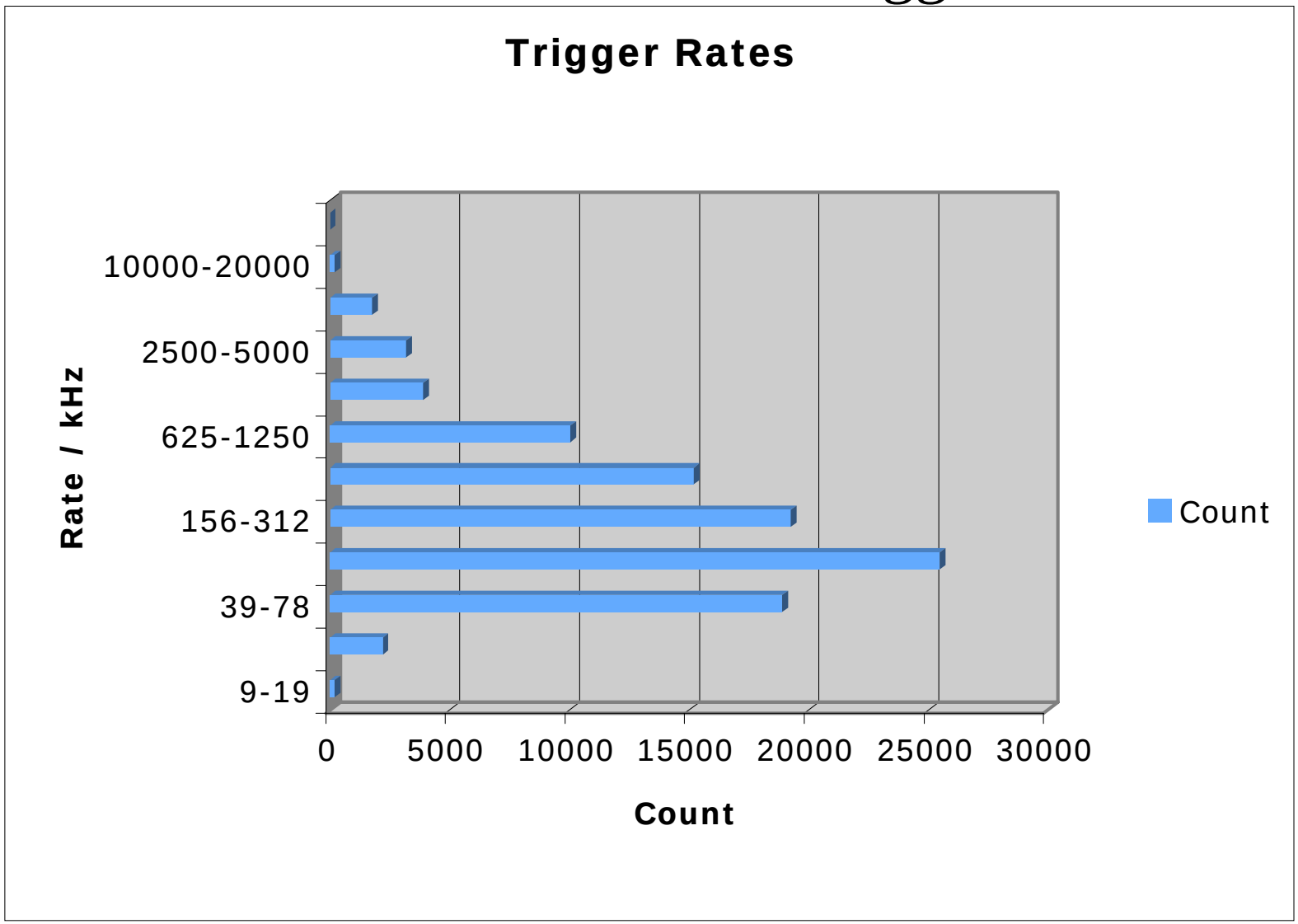
Test Purpose

- The purpose of the tests were twofold
  - To create a platform where batches of 30 FEDs can be tested at high rate over long runs of 24 hours, with FRLs to officially qualify them for installation in P5
  - To push the DAQ to it's limits in order to confirm the final trigger rates and data throughput capability of the complete final system

Results of 24 hour test

- All FEDs tested in batches of 30
  - run for 24 hours
  - 5% occupancy
  - 140 KHz Instantaneous Poisson Trigger
  - Sustained Trigger rate of 75 KHz
  - Total events read per test ~ 6.5 billion
  - Total CRC errors during stable operation - 0

Simulated 140 KHz Poisson Triggers



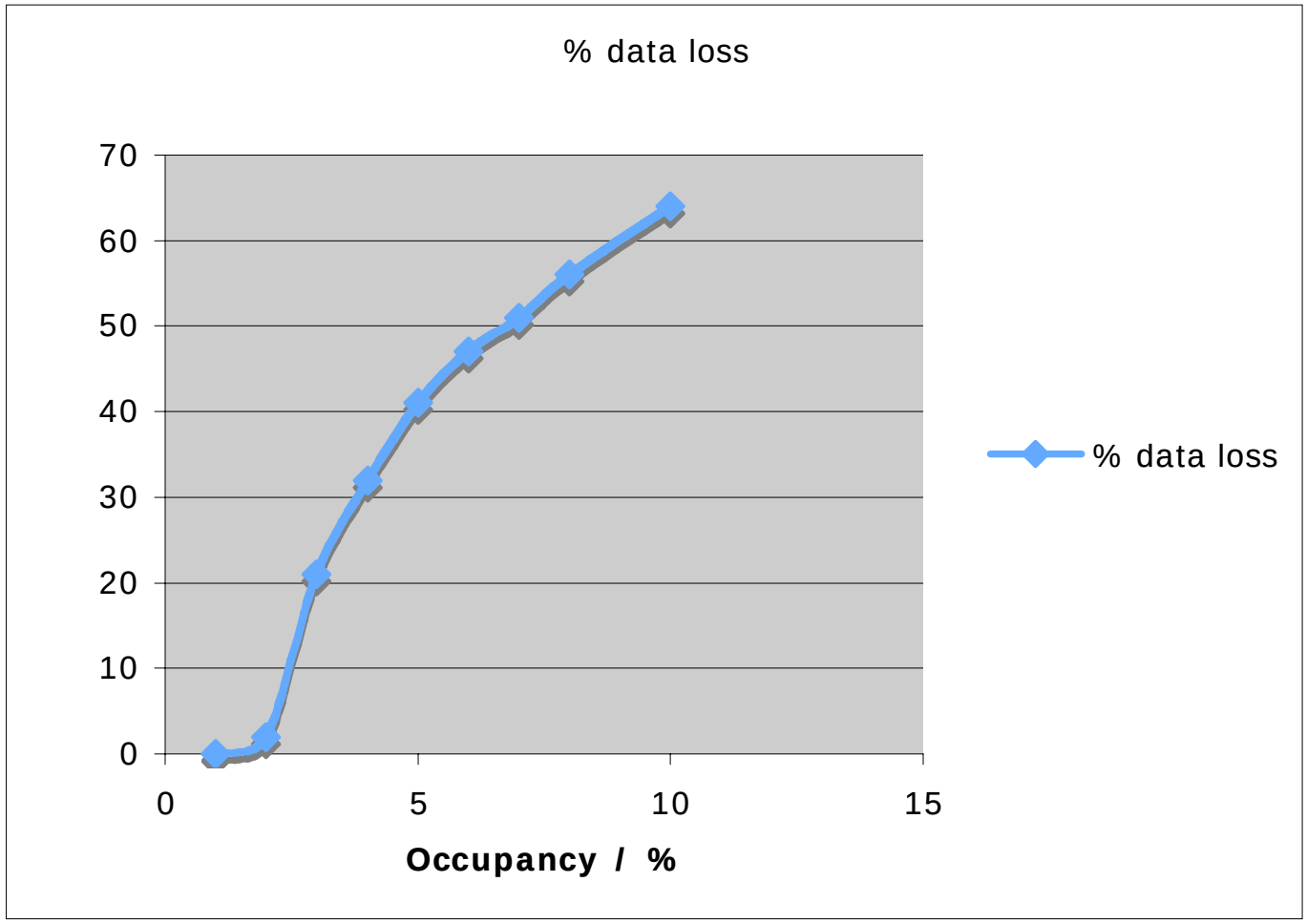
Results

- 140 KHz - Full Debug header Mode - Full Zero Suppressed header mode

Trigger Rate / kHz	Hits / 2APVs	occupancy
133 □	3	1%
98	5	2%
79	8	3%
68	10	4%
59	13	5%
53	15	6%
49	18	7%
44	20	8%
36	25	10%

% Data loss @ 100kHz

Full Debug Header Mode - Zero Suppressed



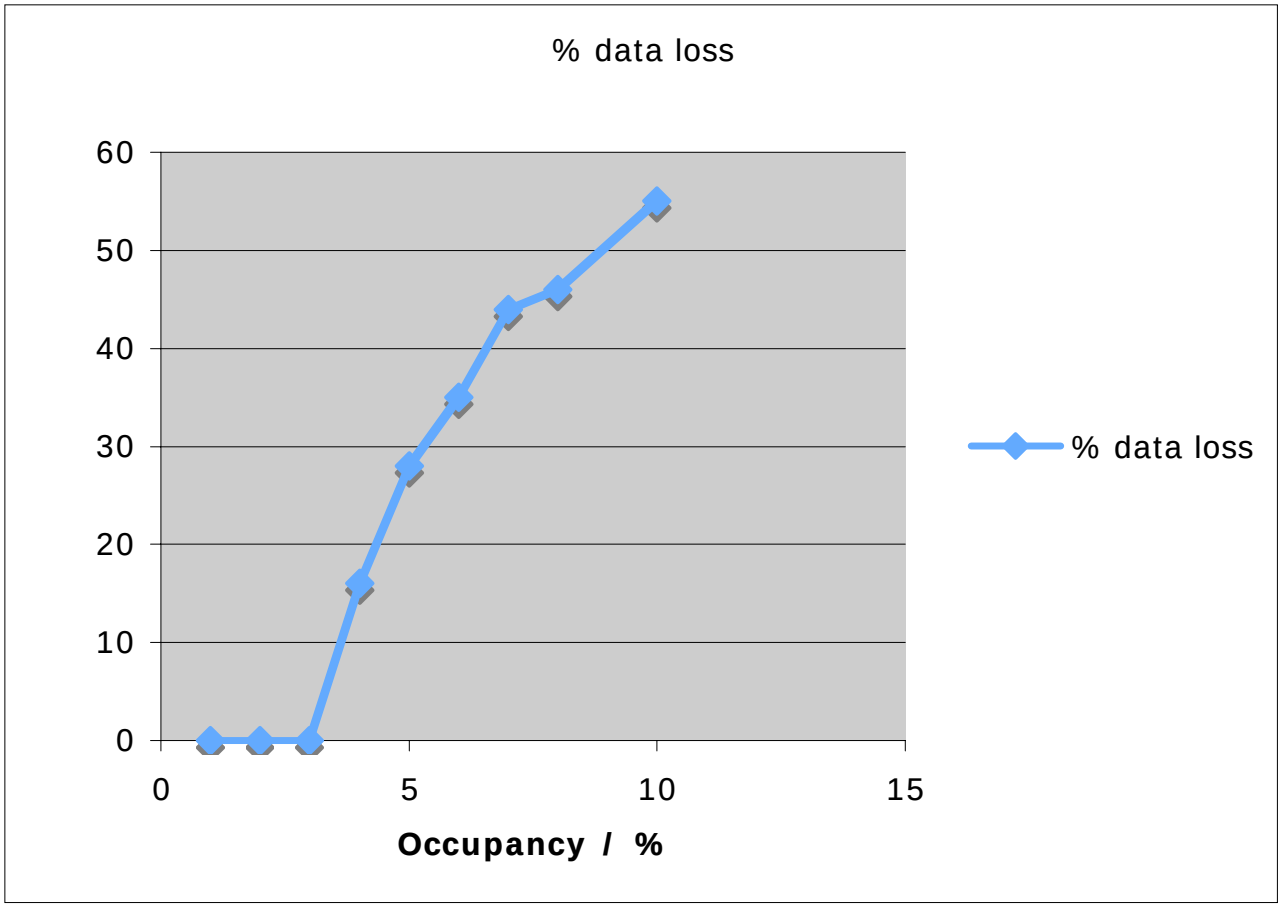
Results

- 140 KHz - APV Error Header - Zero Suppressed Lite

Trigger Rate / kHz	Hits / 2 APVs	occupancy
137	3	1%
135	5	2%
102	8	3%
84	10	4%
72	13	5%
65	15	6%
56	18	7%
54	20	8%
45	25	10%

% Data loss @ 100kHz

Zero Suppressed Lite Header Mode



Summary

- CMS Tracker DAQ Works at predicted trigger rate
- Sustained trigger rate - 100 kHz for 3% occupancy with Zero data loss

Acknowledgements

- Thanks go to…
- R Arcidiacono, J Gomez, C Schwick - FRL and FMM
- L Mirabito, R Bainbridge, F Drouhin - DAQ software and debugging
- O Zorba - Hardware organisation
- J Jones, M Pesaresi, M Noy - APVE
- E Corrin, T Christianson - LTC, TTCci
- J Coughlan, S Tagavarid, I Church, J Jole, G Rogers- FED support