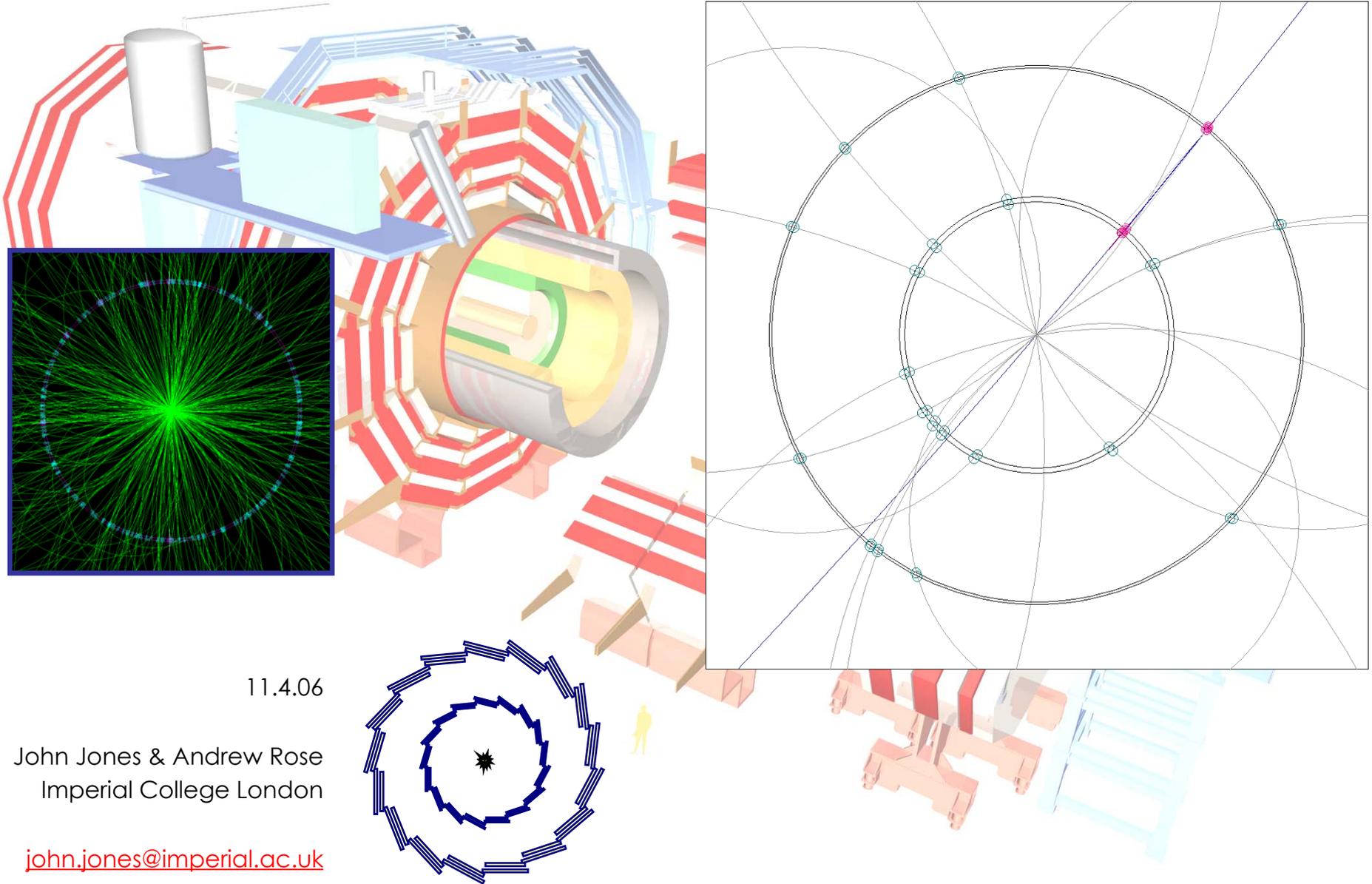


# Stacked Tracking in CMS at Super-LHC



11.4.06

John Jones & Andrew Rose  
Imperial College London

[john.jones@imperial.ac.uk](mailto:john.jones@imperial.ac.uk)

# CMS and The Super LHC

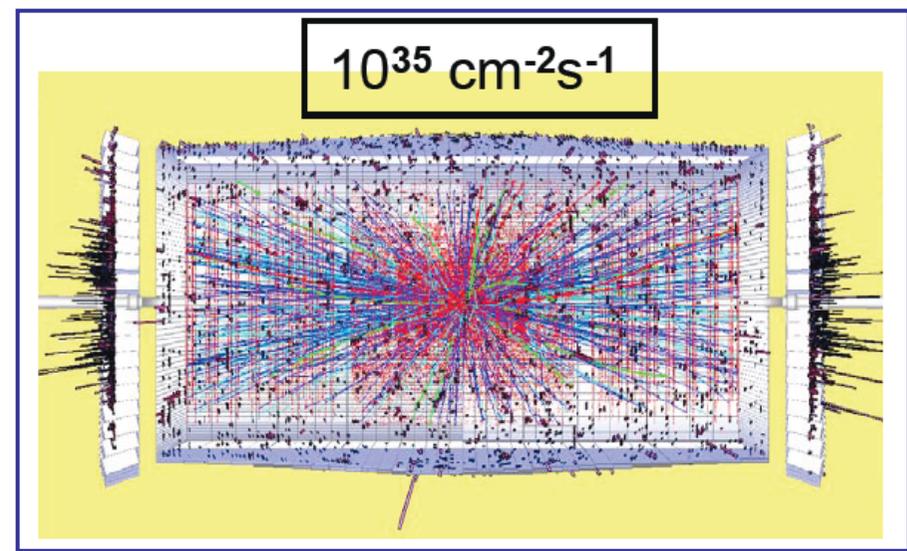
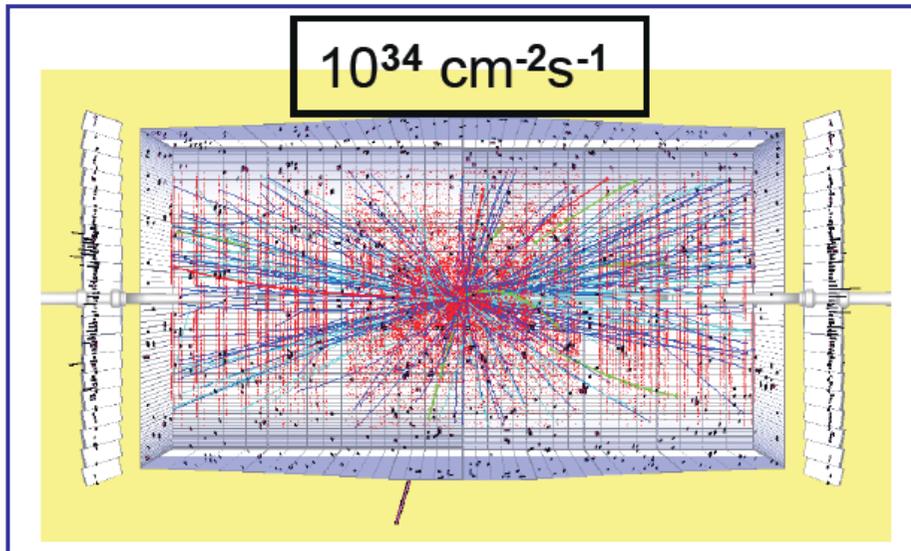
- Current CMS trigger is designed for 'clean' (relatively unambiguous) signatures
  - Higgs → **Muons, di-photons**, (jets, 4 leptons)
  - SUSY → **Missing  $E_T$ , leptons**, (topological triggers)
- 1<sup>st</sup> level of triggering in CMS has to perform fast, complex calculations in  $\sim 1.5\mu\text{s}$
- Design of trigger was driven by many constraints
  - **Money, power, cabling, radiation tolerance, hardware capability, speed, availability of components, programmability**

It has been proposed that LHC be upgraded x10 nominal luminosity in 2015

$$\underline{10^{35}\text{cm}^2\text{s}^{-1}}$$

- Requires an improvement in detector performance to allow efficient triggering
- CMS requires tracking information in L1 trigger in the future
- Tracker is not currently used for many reasons
  - Data rate is too great, even for nominal LHC environment
  - In upgrade, rate at  $r=10\text{cm}$  is  $\sim 10\text{Gbit}/\text{cm}^2/\text{s}$  when zero-suppressed

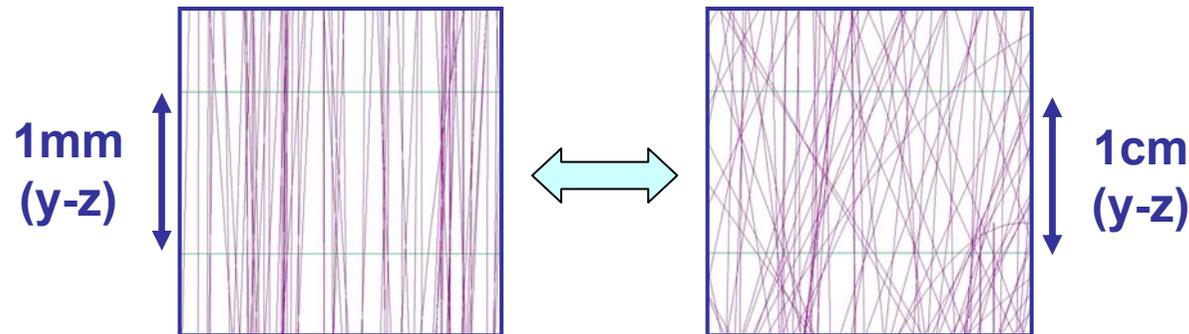
## What Does It Look Like? (Why It's A Problem)



- Leptons, photons and pions look like jets (lack of isolation)
  - Incorrect energy, no isolation
- Jets look like clusters of jets (lack of isolation)
  - Incorrect count, incorrect energy, incorrect missing  $E_T$
- Muon chambers lose ability to threshold rate of trigger based on  $p_T$  of track
  - Inability to control single-muon trigger rate (although use not certain in SLHC)
- Bandwidth of DAQ system increases x10 if trigger rate same as current LHC
  - If we allow trigger rate to increase, requirement grows x100 – UNACCEPTABLE

# The Proposal

- We want tracker information in the L1 trigger in SLHC



- Use two **stacks** of **closely-spaced** coupled stitched Sol-MAPS sensors
  - Reduces **combinatorials** to manageable levels on-detector
- **Geometrical  $p_T$ -cut** - [J. Jones](#), [A. Rose](#), [C. Foudas](#) LECC 2005
  - + Lower power consumption (than reading everything out)
  - +  $\sim O(100)$ Mbit/cm<sup>2</sup>/s optical links (reduced cabling requirements / power)
  - + Close electrical coupling - avoids the need for detector-wide communication
  - + Can be used to infer  $p_T$  using two '**super layers**'
- Places strict demands on mechanical aspect of design
- Material budget of detector must not increase significantly

# Why MAPS?

- Standard technology which will exist in some form for many years
  - Development / technology scaling done for us by industry
  - Sol approaches now offered by some foundaries...(e.g. OKI 0.15)
- Already shown to be rad-hard to  $>10^{14}$  p/cm<sup>2</sup>
  - Not close, but careful design may improve on this
  - Could still be useful as a starting point for prototyping (we don't have much time!)
- Can use stitching technologies to make sensors ~ wafer size
  - 10cm 'pixel strips'

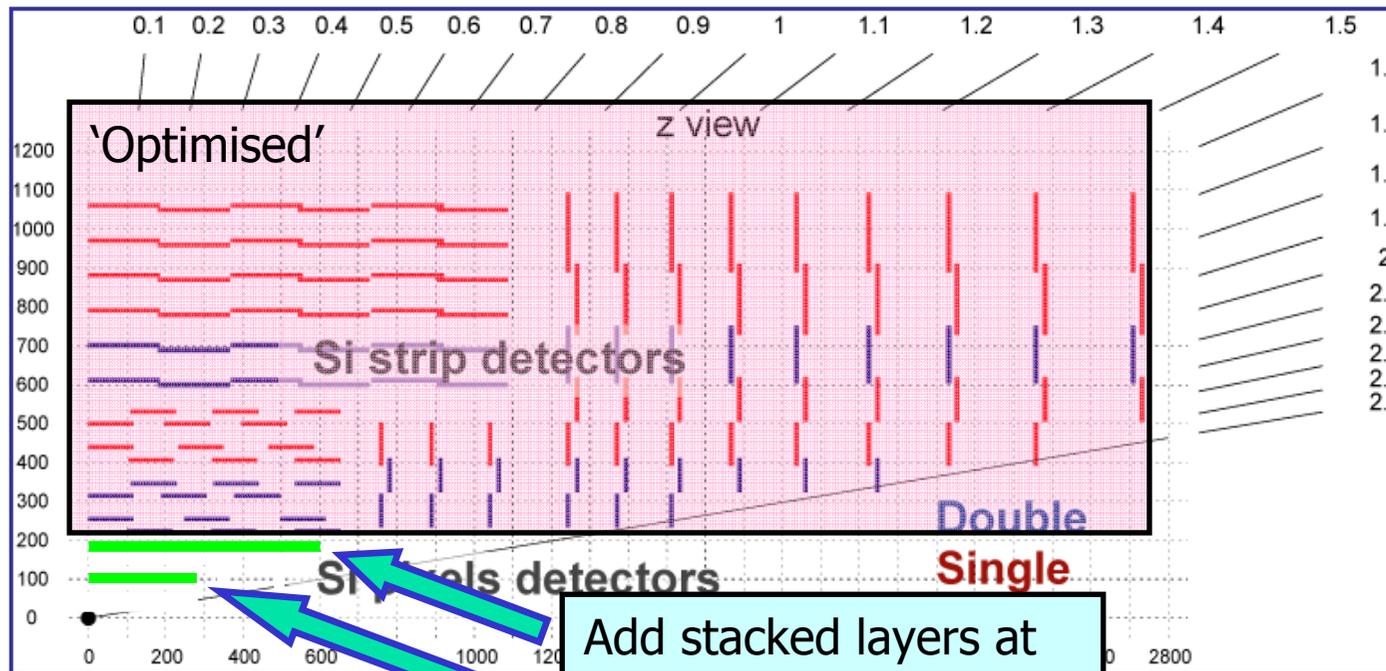
## CHEAP

- If radiation tolerance not enough, replace!

	<u>Pixel (now)</u>	<u>Large pixels</u>	<u>Macropixels</u>	<u>MAPS</u>	<u>CMOS+Sensor</u>
Pixel Area	0.015 mm <sup>2</sup>	0.15 mm <sup>2</sup>	1.5 mm <sup>2</sup>	---	---
Sensor/ROC	1 / 1	1 / 1	10 / 1	0 / 1	1 / 1
Tiling unit	10 cm <sup>2</sup>	40 cm <sup>2</sup>	100 cm <sup>2</sup>	4 cm <sup>2</sup>	4 cm <sup>2</sup>
Bumping	320	20*	2*	0	0
Sensors	80	10	10	0	10+10? <sup>(4)</sup>
ROC	25	50	2	50	200? <sup>(3)</sup>
HDI	30	30	3	30	30
Cables	8	8	0.8	8	8
Baseplate	5	5	0.5	5	5
Pitchadjust	0	0	15 <sup>(2)</sup>	0	0
Optical Link <sup>(1)</sup>	32	6	0.6	6	32
pxFED	25	4	0.4	4	25
<b>Total</b>	<b>525</b>	<b>~130</b>	<b>~35</b>	<b>~105</b>	<b>~320?</b>

R. Horisberger  
4<sup>th</sup> CMS SLHC Workshop

# Detector Layout (I)



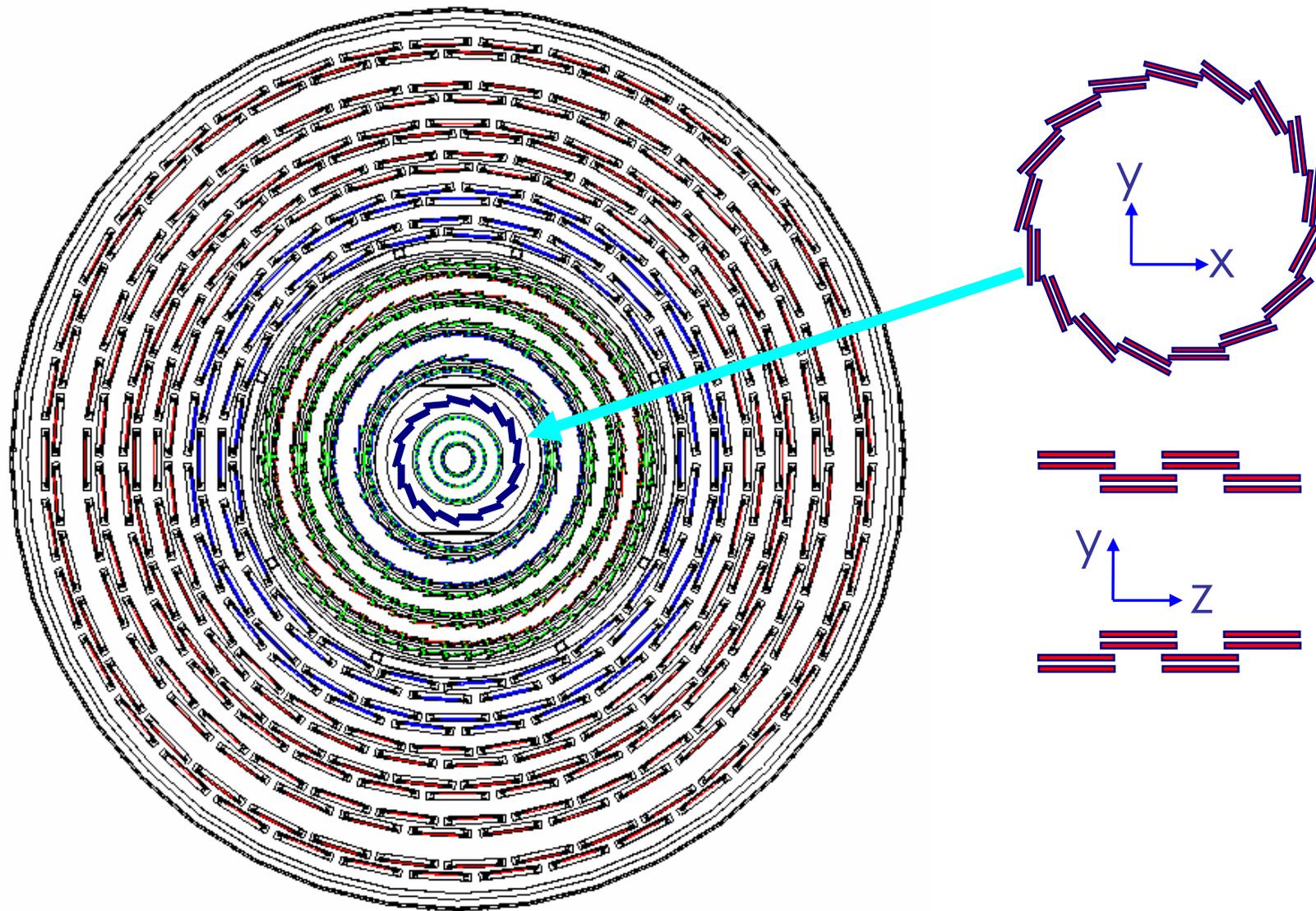
Add stacked layers at  $r \sim 10\text{cm}$  &  $r \sim 20\text{cm}$

Detector Dimensions:  
Tiled, each tile  $\sim 10\text{cm}(z) \times 2\text{cm}(r) - 20\text{cm}^2$   
Total size  $120\text{cm}(z) \times 20\text{cm}(r)$  &  $60\text{cm}(z) \times 10\text{cm}(r)$

Pixel Pitch:  $50\mu\text{m}(r) \times 50\mu\text{m}(z) \times 50\mu\text{m}(\phi)$

← Relaxed from 2005

## Detector Layout (II) – Possibility of ‘Phase 1’ Intermediate Upgrade



# Tangent-Point Reconstruction

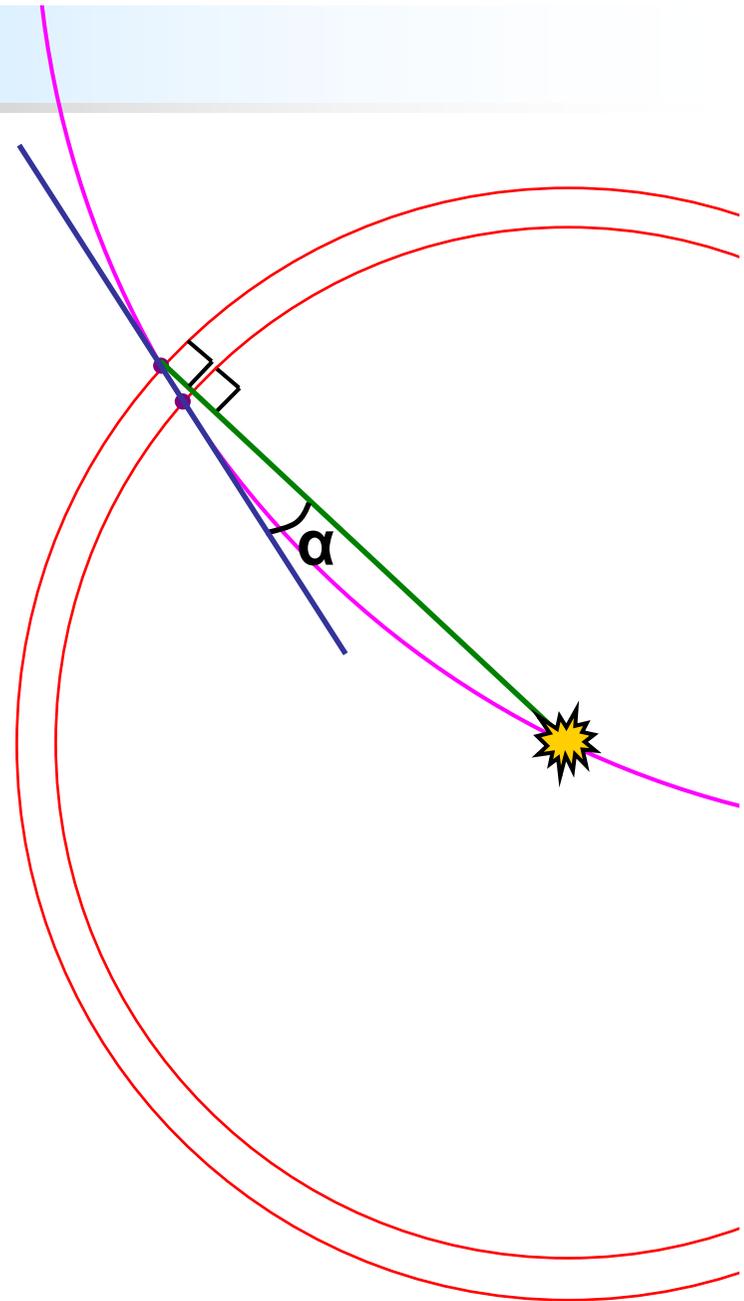
- Assume IP  $r=0$
- Angle  $\alpha$  determines  $p_T$  of track

## Smaller $\alpha$ = greater $p_T$

- Can find high- $p_T$  tracks by looking for small angular separation of hits in the two layers
- Correlation is fairly 'pure' provided separation is small and pixel pitch is small

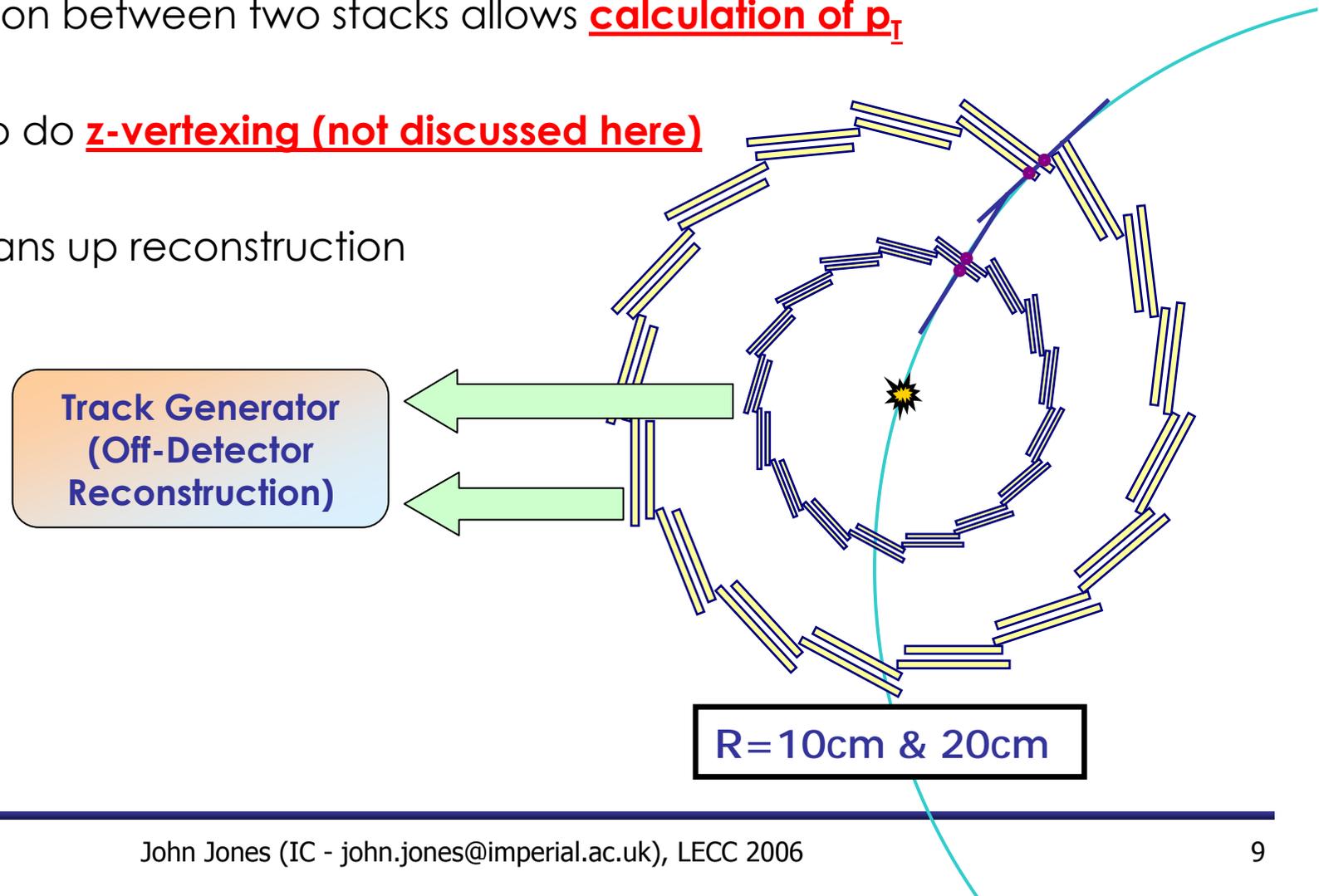
## Matching hits tend to be from the same track

- If sensors are precisely aligned, column number for hit pixels in each layer can be compared
- Finding high- $p_T$  tracks becomes a relatively simple difference analysis



# The Double-Stack Method

- Close space minimises combinatorials in each layer and allows  $p_T$  cut to be applied 'easily' **on-detector, but in each stack separately**
- Separation between two stacks allows **calculation of  $p_T$**
- Can also do **z-vertexing (not discussed here)**
- Also cleans up reconstruction



# Double Stack Reconstruction Theory

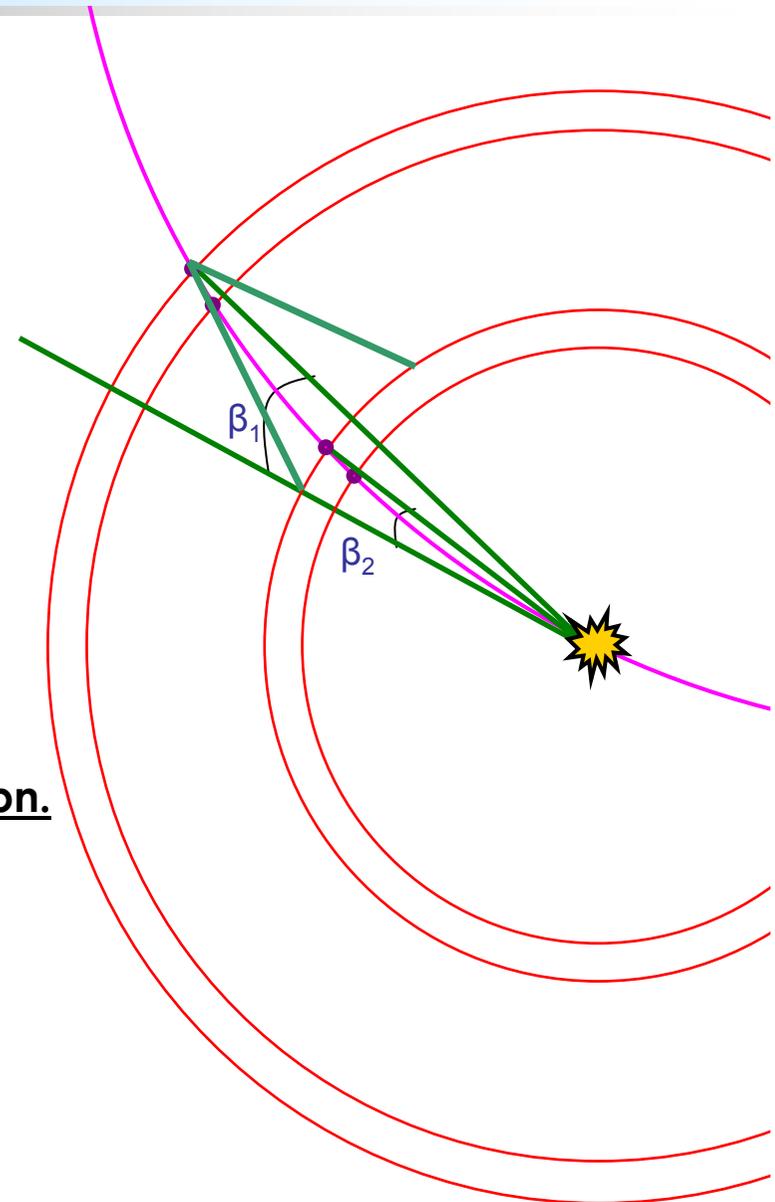
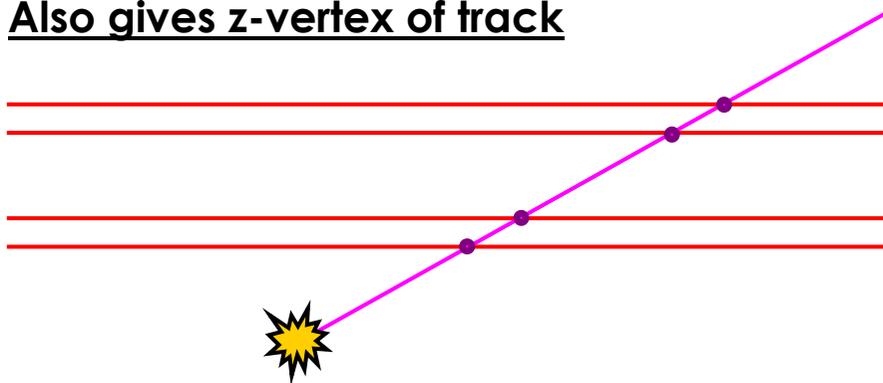
- You might think:

Project backwards from outer→inner stack

- This actually makes things worse
  - Combinatorials actually increase

Correct way is to use z information as well

- Introduces a requirement on z-pitch
  - Must be < 100 microns depending on stack sepn.
  - Also gives z-vertex of track



# DS Reconstruction in Practice

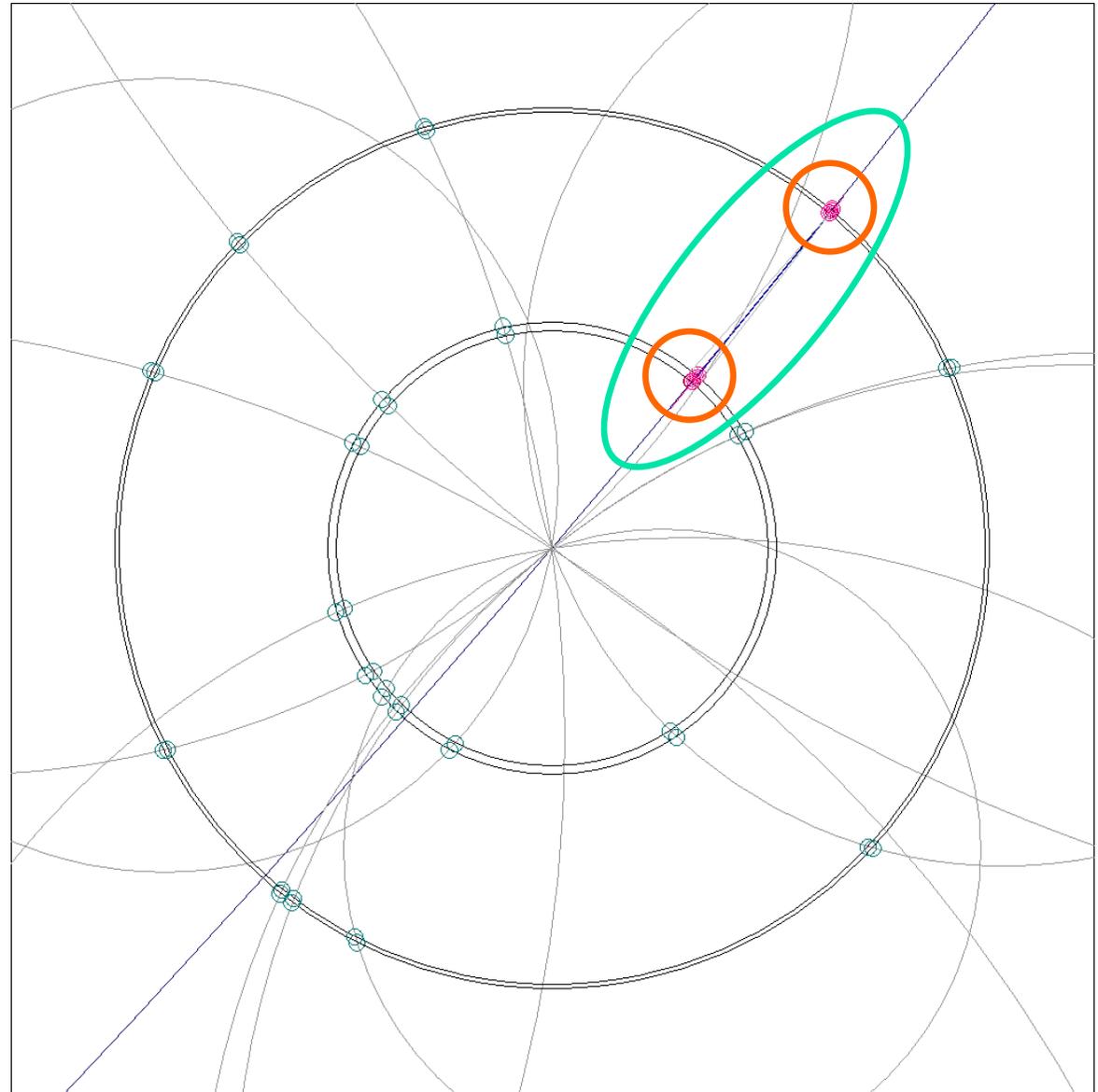
1 event to show principle

1) Hits detected in both stacks

2) Correlator isolates high- $p_T$  tracks in each superlayer

Data shipped off-detector

3) Hits in each stack are paired in off-detector track finder



# DS Parameter Space

- Bigger parameter space than single stack
  - There we had 3 pitch parameters, radius & separation
  - Here this doubles to 10 parameters, but can rationalise
  - Inner & outer radii somewhat arbitrary choice (could be tuned); say  $r=10\text{cm}$  &  $r=20\text{cm}$
  - Separation of  $r=10\text{cm}$  stack is logically related to  $r=20\text{cm}$  stack
    - $p_T$  cut in outer stack should be similar to inner stack, so  $2 \cdot r_{\text{SEP\_OUTER}} \sim r_{\text{SEP\_INNER}}$
  - Keep pitches identical
    - Having searched parameter space, square 50 micron pixels good compromise
- Assume cut at  $\sim 3.5\text{GeV}$  (50 micron pitch)
- Separation  $\sim 4\text{mm}$  @  $r=10\text{cm}$ ,  $\sim 2\text{mm}$  @  $r=20\text{cm}$

# DS Rates / Purities / Efficiencies

- $r=10, 10.2, 20, 20.4\text{cm}$ ; Global  $p_T$  cut  $< 4\text{GeV}$
- 200 events / BX ( $10^{35}\text{cm}^2\text{s}^{-1}$  @ 40MHz)

Output data rate relative to raw data rate

Number of reconstructed tracks / BX

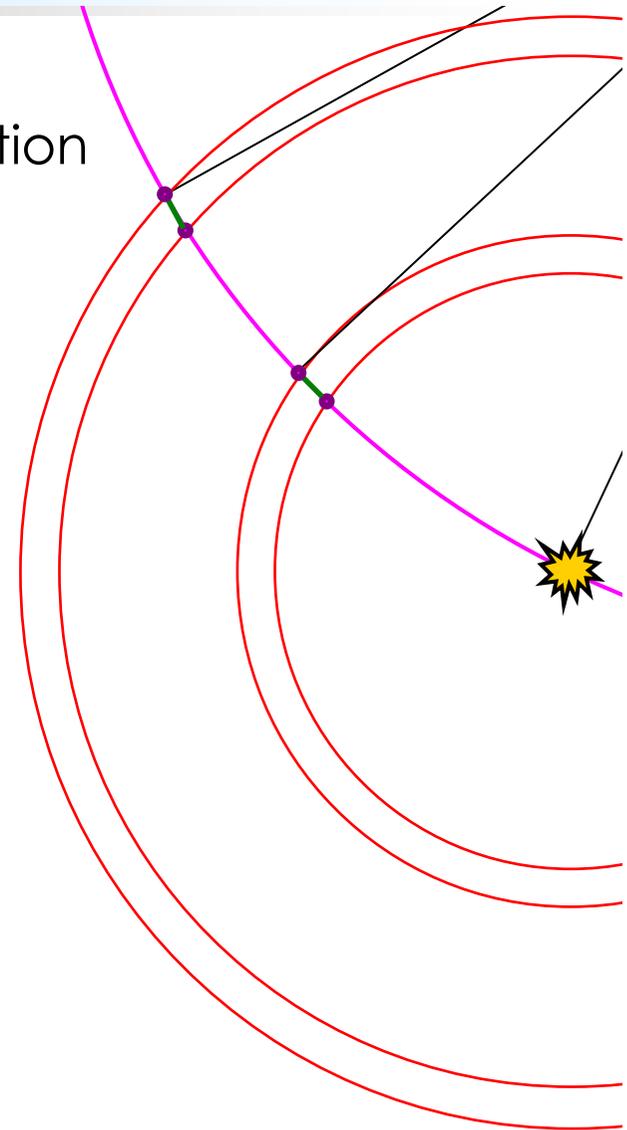
Likelihood that reconstructed track is a ghost

Number of 'real' available tracks

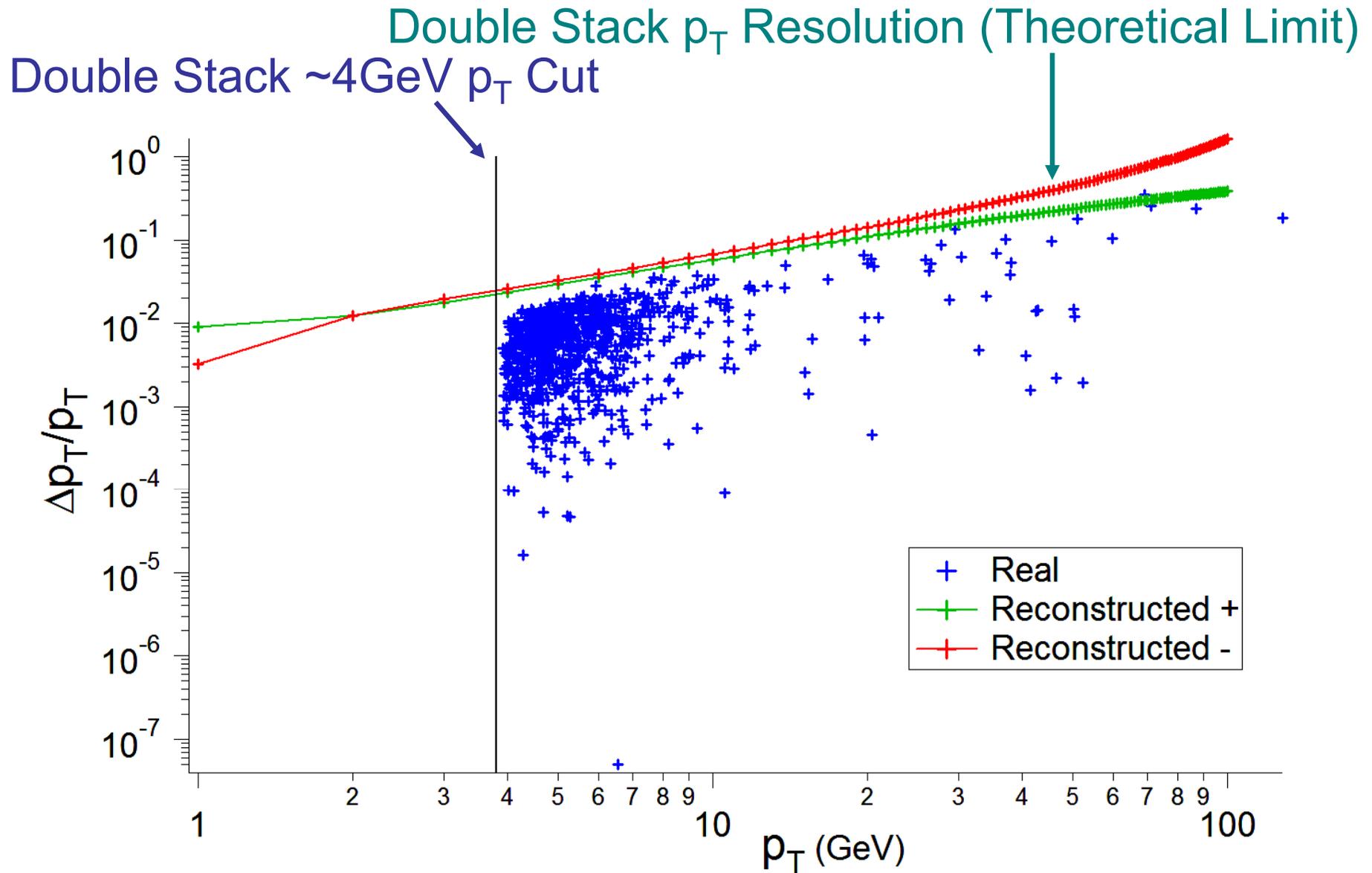
Phi Pitch ( $\mu\text{m}$ )	Z Pitch ( $\mu\text{m}$ )	Inner Stub Rate (%)	Outer Stub Rate (%)	Reconstructed Tracks / BX	Available Tracks / BX	Purity (%)
20	50	1.42	1.52	1.24	1.24	100
40	50	3.31	3.55	8.84	8.84	99.6
60	50	5.38	5.85	21.74	38.16	99.4
80	50	7.61	8.28	22.36	97.52	98.9
100	50	9.96	10.93	22.20	177.12	97.2
50	10	4.32	4.69	16.78	19.68	99.8
50	20	4.31	4.69	16.78	19.68	99.6
50	40	4.29	4.69	16.74	19.68	99.4
50	100	4.31	4.67	16.80	19.70	98.2
50	200	4.23	4.66	16.70	19.64	96.8

# Double Stack $p_T$ Measurement

- Tangent itself doesn't give you useful information
  - Coarse-grained  $p_T$  information from cutting useless
  - Throw it away...
- Use outer point of each pair for sagitta
  - Calculate  $p_T$  in the usual way... (assuming  $r=0$ )

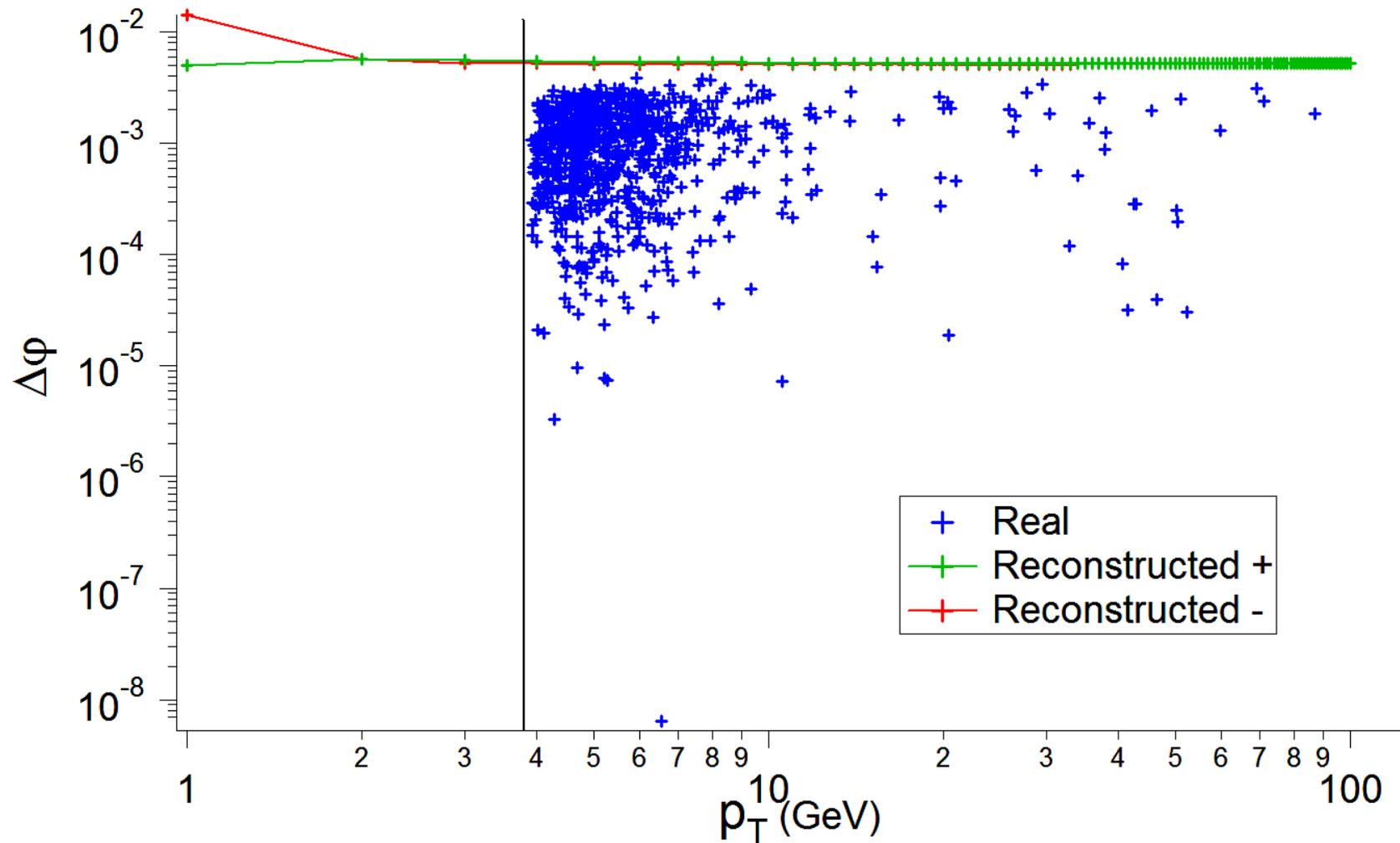


# DS $p_T$ Resolution (50x50 pixels)



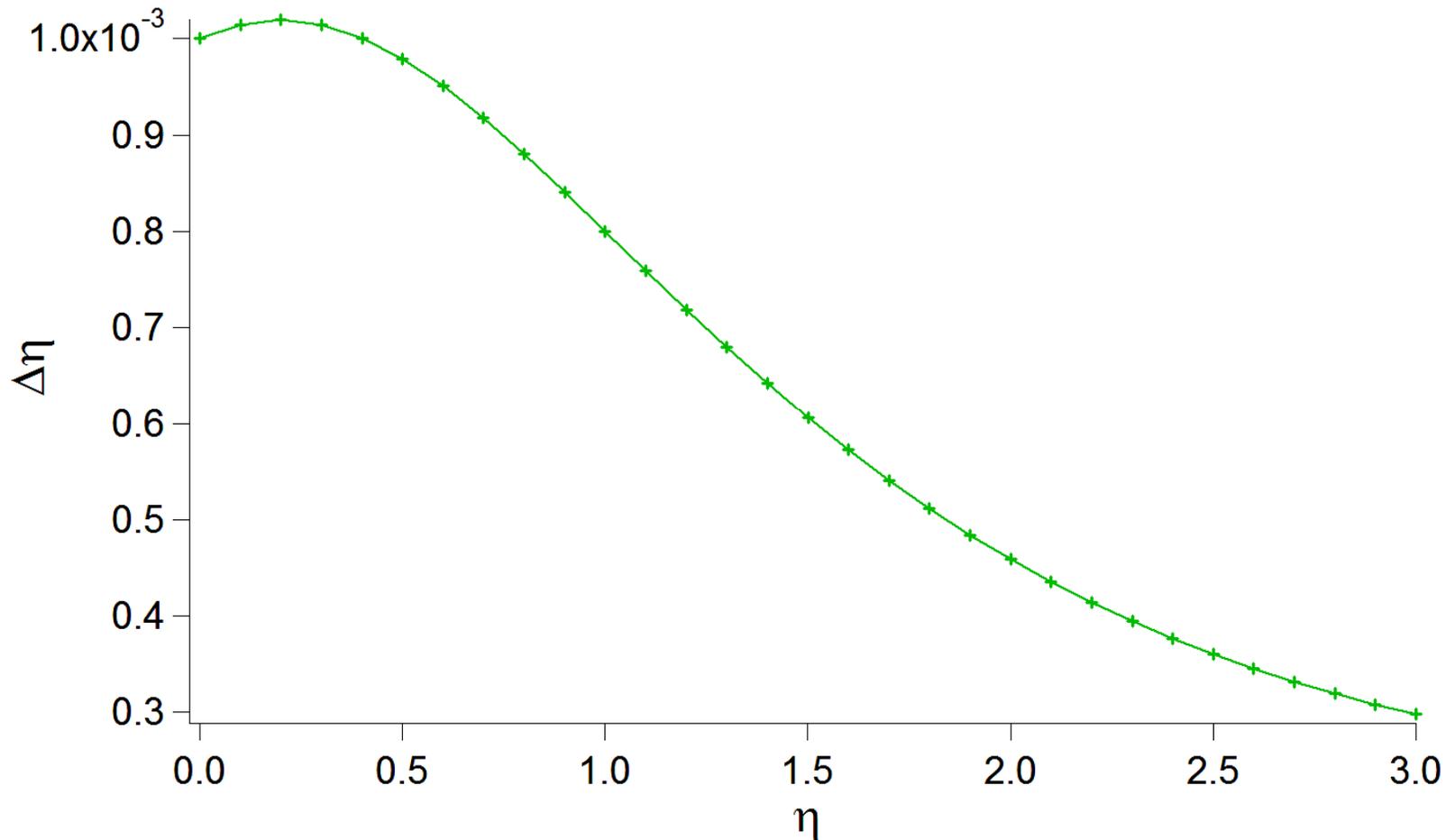
## DS Resolution in $\varphi$

- Reduced resolution at high  $p_T$  balanced by smaller curvature
- Resolution always better than 0.003 or  $\sim 4\text{mm}$  (c.f. 0.087)



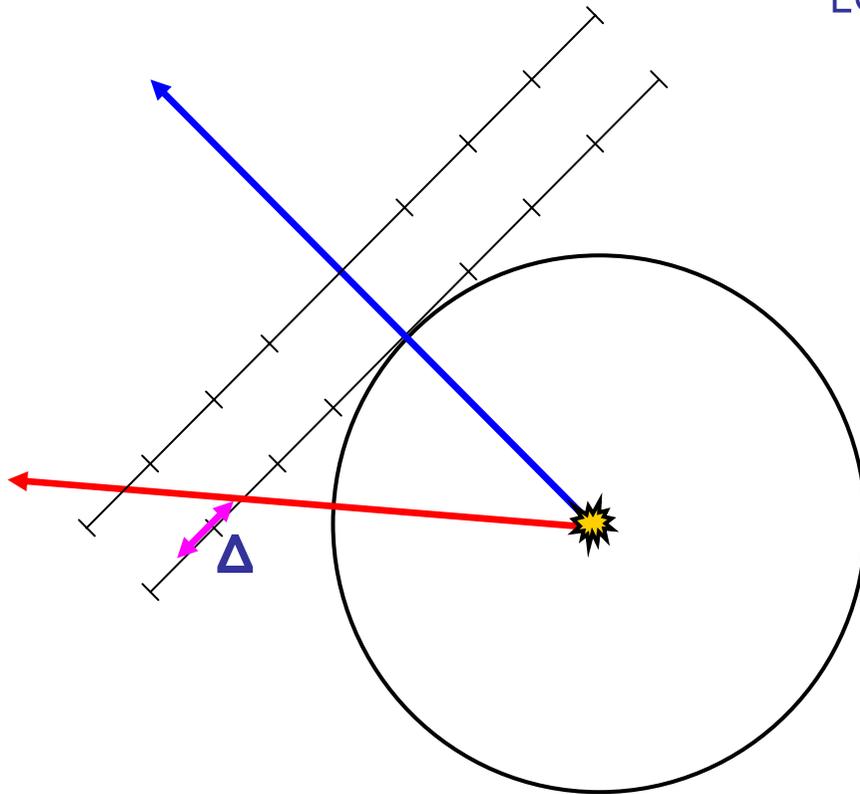
## DS Resolution in $\eta$ (50x50x50)

- Resolution of double stack far better than needed
- Trigger towers in ECAL are  $0.087 \times 0.087$  ( $\Delta\eta \times \Delta\phi$ )
- Worst case here is 0.001 – 1.3mm in middle of detector!



# Subtleties I – Pixel Flatness

- Pixels chips are really flat
  - Has impact on single stack reconstruction because of mismatch between normal to pixel sensor and straight track
  - $p_T$  cut becomes charge-dependent



Lateral shift / Stack separation =  
(Sensor width / 2) / Radial position

$$\Delta = 2\text{mm} \times (2\text{cm} / 2) / 10\text{cm}$$

$$\Rightarrow \underline{200\mu\text{m}}$$

Requires either reduced pixel pitch & layer separation or load calibration constants into correlator

## Subtleties II – Data Rate & Compression

- Track hits form clusters
  - Simulation includes this (~x2 rate increase)
  - Clusters can be calculated on-detector to reduce data rate
- Sensible data encoding can improve things too
  - Correlator guarantees pixel column difference < ~1 pixel
  - So only need to encode origin of outer stack and difference
  - Still need to encode full z pixel locations

Header	Outer Column Origin (8)	Inner Column Offset (8)	Outer Row Origin (8)	Inner Row Origin (8)
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**x2**

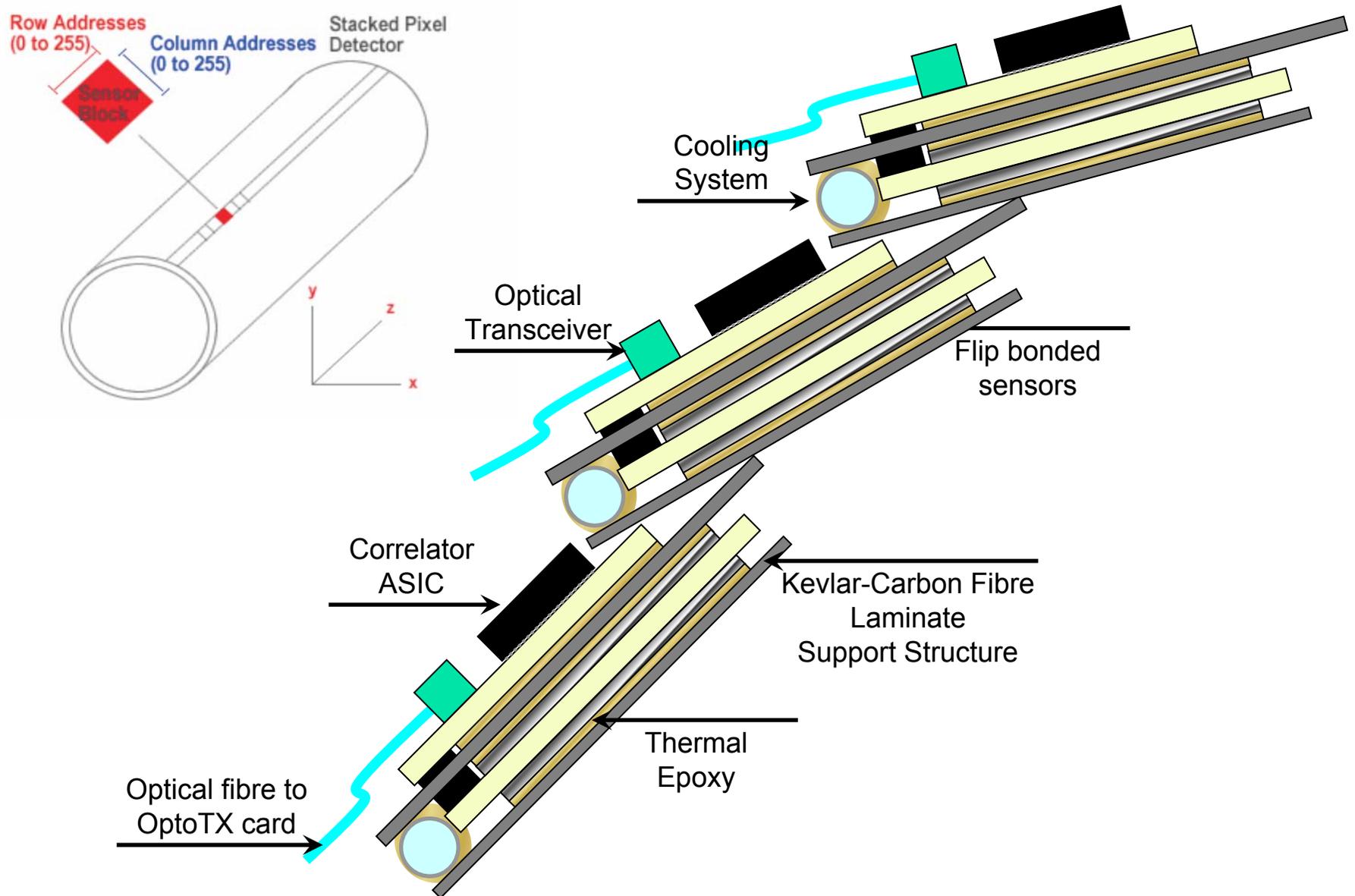
**vs.**

**= 64 bits**

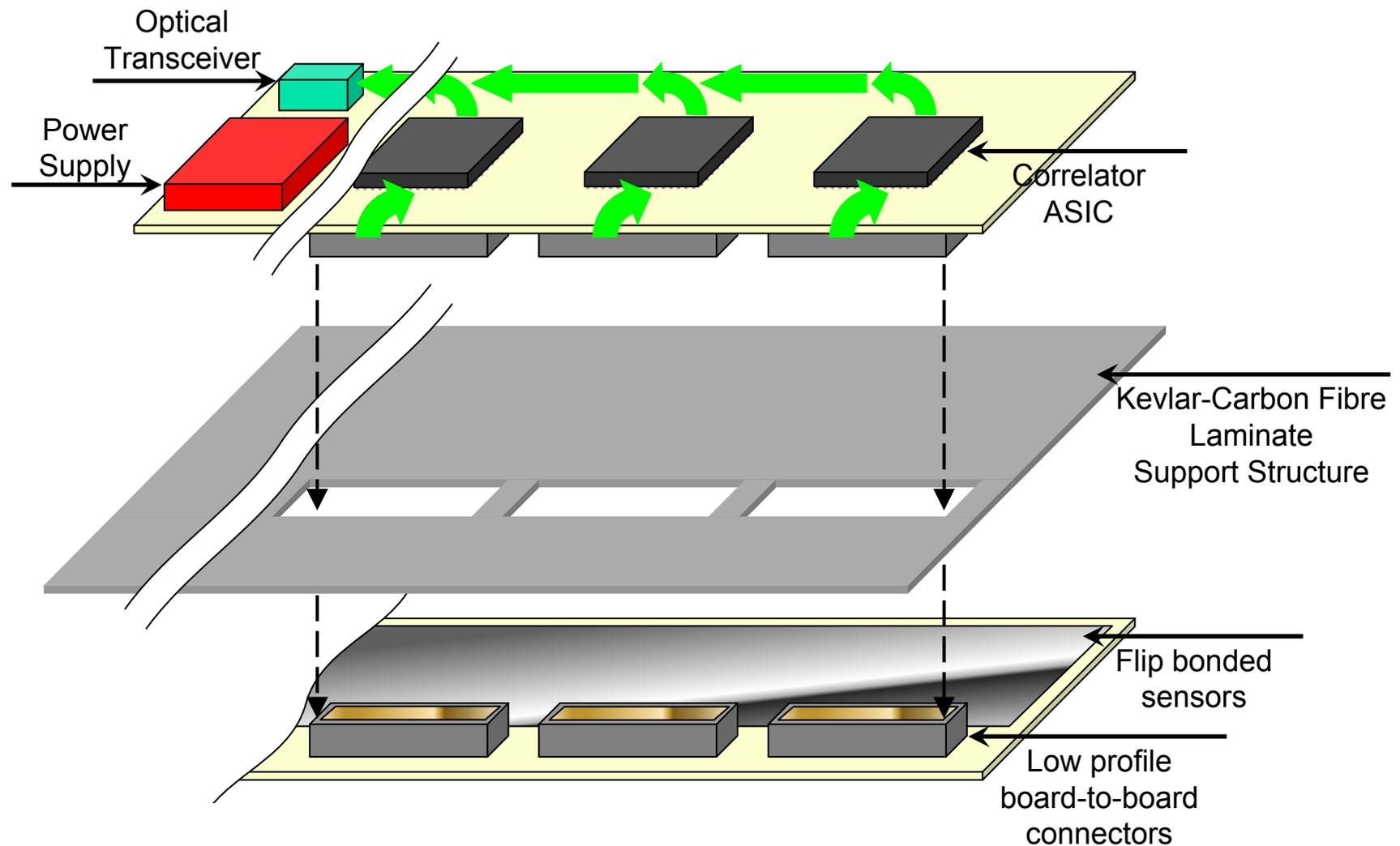
Header	Outer Column Origin (9)	Inner Column Offset (2)	Outer Row Origin (9)	Inner Row Origin (9)
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**= 29 bits (~45%)**

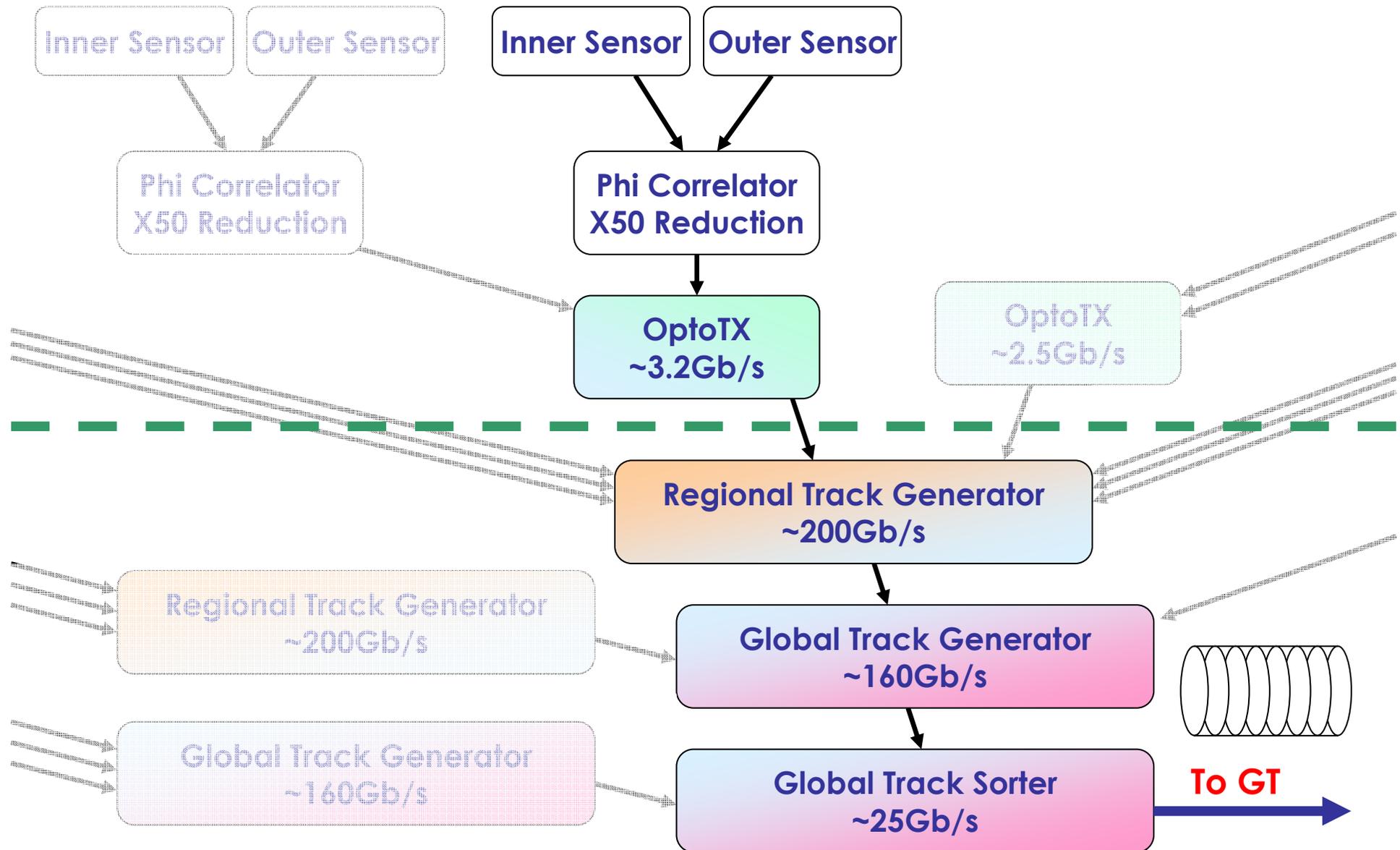
# Conceptual Design



# Correlator PCB



# Processing Architecture



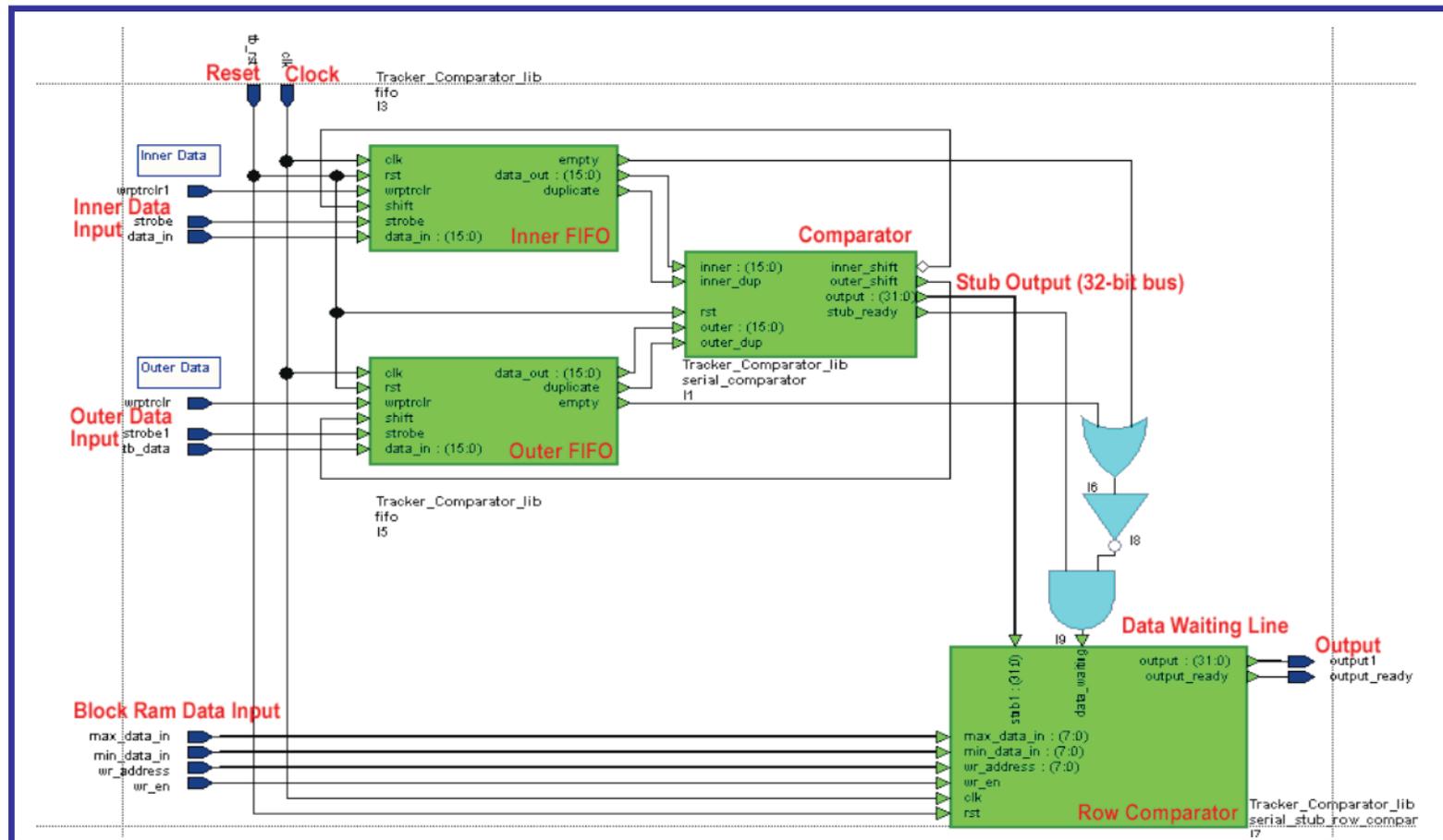
# Bandwidth Requirements

Component	Output bandwidth per unit	Rate Reduction	Number of units per upstream component	Total number of units	Aggregate output bandwidth
Sensor (20cm <sup>2</sup> )	10Gb/s/cm <sup>2</sup>	N/A	~0.4	~1600	~140Tb/s
Hit Correlator (5 per 20cm <sup>2</sup> stack)	~1.6Gb/s	X50	~2	~2000	~3Tb/s
Opto TX and SERDES	~3.2Gb/s	N/A	12	~1000	~3Tb/s
12xSFP to SNAP12 Cable	~40Gb/s	N/A	5	~90	~3Tb/s
Regional Track Generator	~50Gb/s	X4	~3	~18	~1Tb/s
Global Track Generator	~4Gb/s	X40	~6	~6	~25Gb/s
Global Track Sorter	~10-20Gb/s	X2?	N/A	1	~10-20Gb/s

# Regional Track Generator Architecture

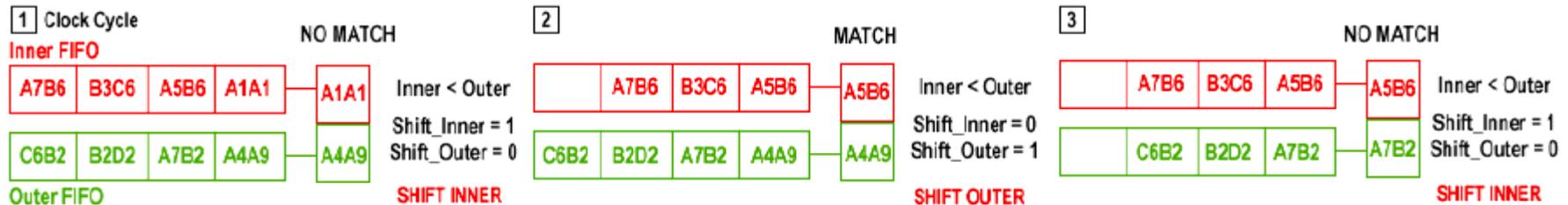
- Various architectures considered
  - But serial processing shown to be most efficient
- Data is column & row-ordered before processing
- Checks result from on-detector correlator & checks rows

B. Constance & K. Zhu



# RTG Performance

- Synthesised & implemented in Xilinx Virtex-II Pro 70 as benchmark
- Performance will improve in later generations of FPGAs

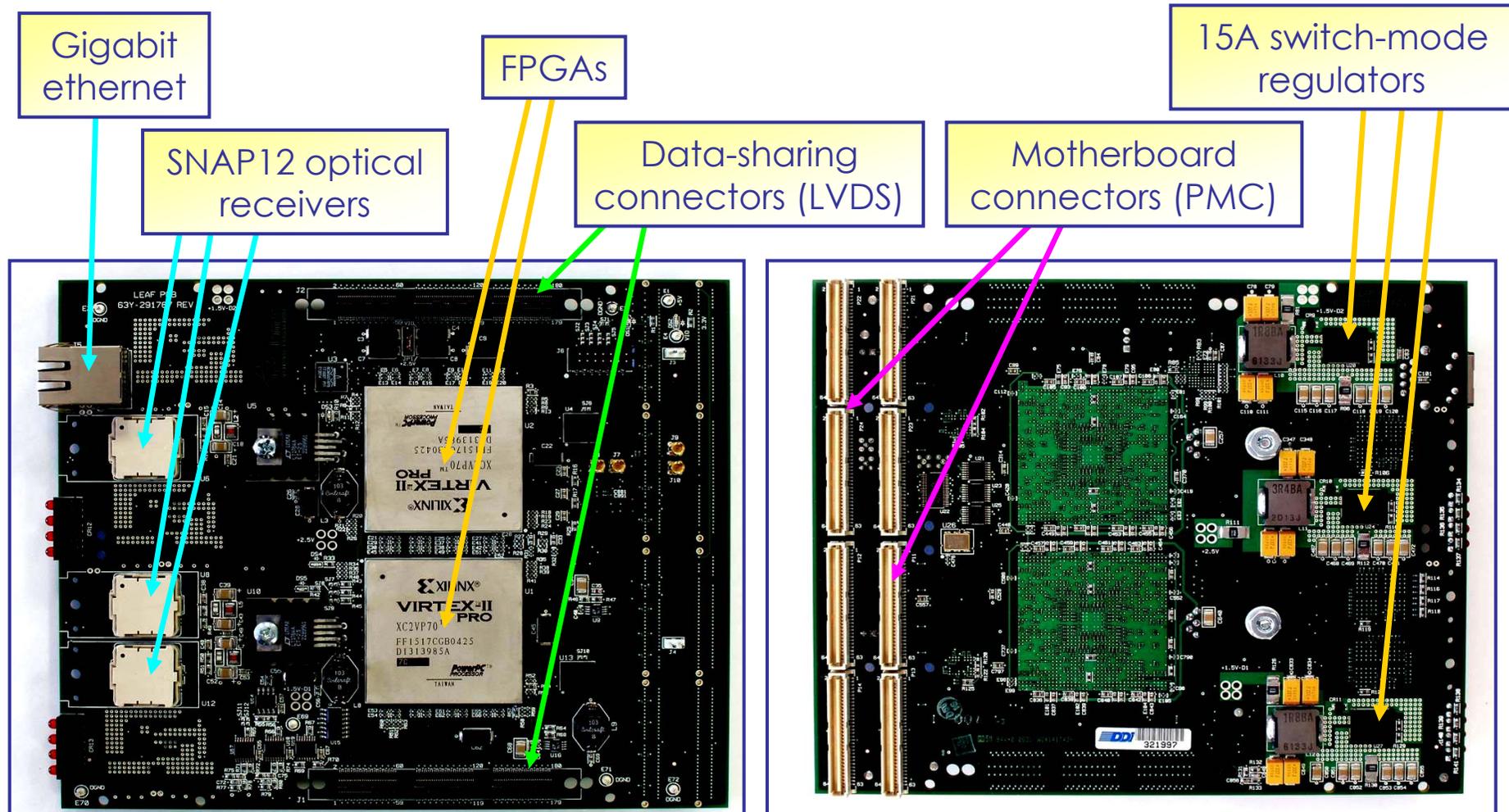


Resources	Used	Available	% Used
<b>5 Processor Units</b>			
External I/Os	365	996	36.65%
RAM 16s	10	328	3.05%
Slices	1456	33088	4.40%
BUFGMUXs	1	16	6.25%
<b>10 Processor Units</b>			
External I/Os	701	996	70.38%
RAM 16s	20	328	6.10%
Slices	2917	33088	8.82%
BUFGMUXs	1	16	6.25%
<b>12 Processor Units</b>			
External I/Os	835	996	83.84%
RAM 16s	24	328	7.32%
Slices	3500	33088	10.58%
BUFGMUXs	1	16	6.25%

**120MHz x 32bit =>  
~4Gb/s/module**

# CMS GCT Leaf Card – Prototype RTG?

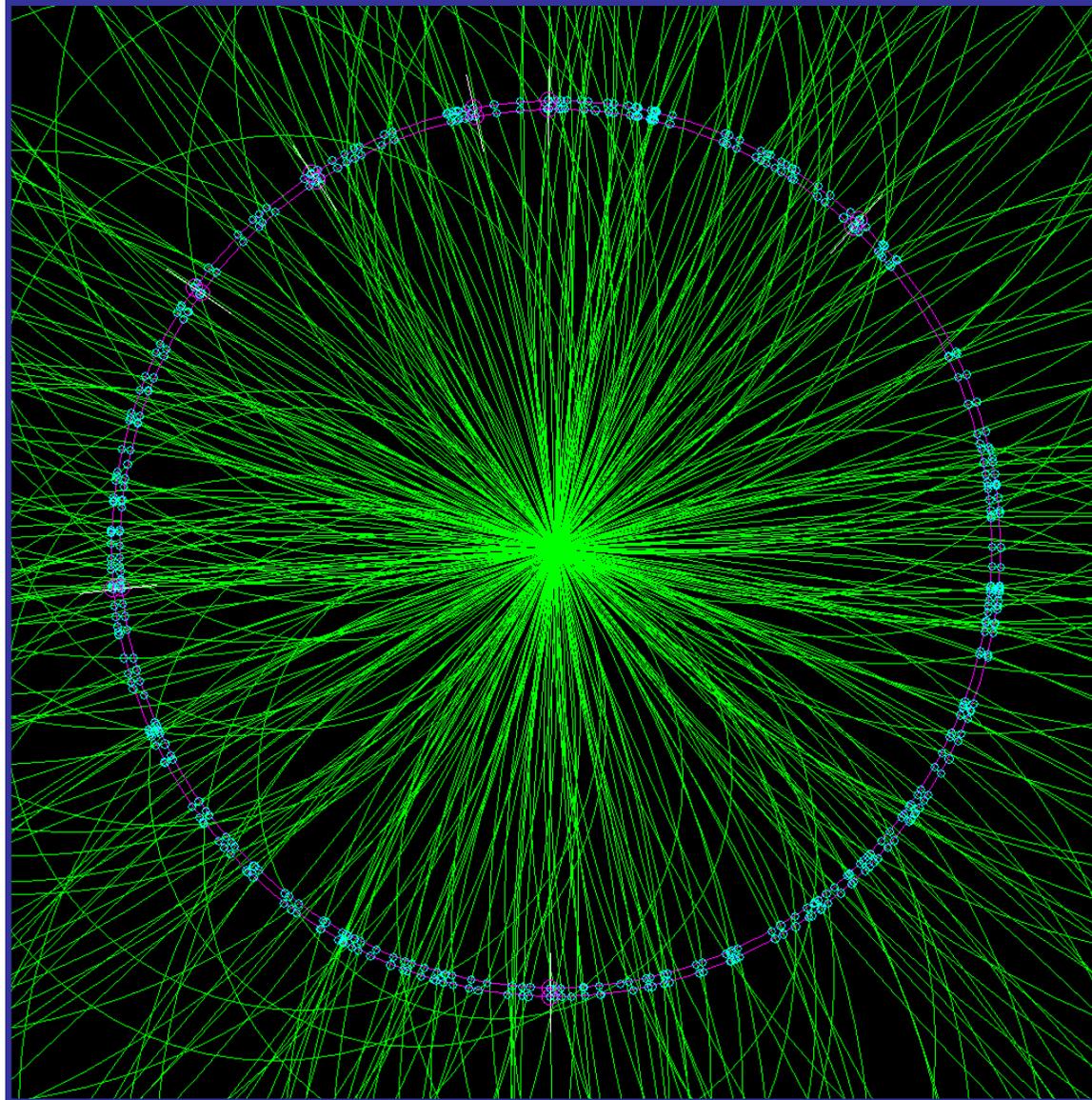
- 2xVirtex-II Pro 70 (-7) double PMC card
  - Fastest & biggest Xilinx FPGA with working multi-gigabit links
  - 32x2Gb/s optical receivers (upgradeable to 3Gb/s => **96Gb/s**)



# Summary

- FPGA reconstruction looks promising
  - Plenty to do, but feasible
- Further development on sensors needed
  - Technology should be readily available now if we're to be ready for upgrade
- Even with rate reduction, stacks etc..., rates are high
  - Need for modern optical links
  - Something faster than 1.6Gb/s would be preferable
- Double stack performance will give more margin in 'real world'
  - More tolerant to noise / bad pixels
  - Better to outperform requirements significantly in simulation
- **More than two stacks isn't necessary for a trigger**

## Additional Slides



# What About The Beam Spot?

- **Possibly** not a problem anymore...
  - Now we have four coordinates...
- Inner stack phi coordinate is useless for  $p_T$  measurement, **but...**
- Can use online data for real-time calibration?

## If beam spot drift ~ms

