Development and Test Results of a Readout Chip for the GERDA Experiment

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Abstract

This paper describes the F-CSA104 architecture and its measurement results. The F-CSA104 is for γ spectroscopy with Ge detectors. It is a low noise, fully integrated, four channel XFAB 0.6μm CMOS technology ASIC, that has been developed for the GERDA experiment. Each channel contains a charge sensitive preamplifier (CSA) followed by a 11.7MHz differential line driver. It has been particularly designed to operate in liquid argon (T = 87K/-186°C) and to have a measuring sensitivity of 660e^- with an ENC of 110e^-, after offline filtering with 10μs shaping, when connected to a 30pF load. Special techniques are used to improve the SNR such as a large input PMOS FET, an integrated 500MΩ CSA feedback resistor and a noise degeneration drain resistor.

I. INTRODUCTION

The GERmanium Dectector Array (GERDA) experiment [1] under construction at the Lab**Error! Reference source not found.**oratori Nazionali del Gran Sasso (LNGS) is searching for neutrinoless double beta (0νββ) decay of ^{76}Ge. Isotopically enriched Germanium diodes, suspended in a 70m^3 liquid argon (LAr) cryostat, serve as sources and detectors (330e^- per keV energy deposition). The LAr cryostat is immersed in a 630m^3 water tank that acts as a neutron moderator and Čerenkov medium. Since the detectors are operated in an unprecedented low background environment the analog amplifiers, which are operated close to the diodes in LAr, have to fulfill stringent requirements on low radioactivity, noise performance and be able to drive the signal off detector. The F-CSA104, alias Gulinbursti, has been designed by FBE ASIC Design & Consulting to fulfill these requirements by an appropriate technology choice and optimised architecture. The following sections outline the required detector electronic specifications and the F-CSA104 chip architecture, gives details of a few critical F-CSA104 circuit blocks, and presents measured performance results from the chip in both room and LAr temperatures.

II. DETECTOR ELECTRONIC SPECIFICATIONS

- Operating temperature 77K (- 196°C).
- Fully integrated system.
- Low power, no bubbling of the LAr. 50mW/channel.
- Differential voltage output to drive 10m of twisted pair cable.
- Total gain 277mV/MeV (5.1mV/fC).
- Measuring sensitivity 2keV (660e^-).
- Dynamic range 5keV - 10MeV.
- Amplifier output rise time < 30 ns.
- System linearity will fit to a 14-bit ADC.
- ENC 110e^- at 30pF load, cold.
- Approximately 300 channels in total.
- 0νββ event rate <10 per year.
- Background in the sub Hz range.
- Detector signal rise time in the order of 300ns.

III. F-CSA104 ARCHITECTURE

The F-CSA104[1] has been fabricated in the XFAB 0.6μm

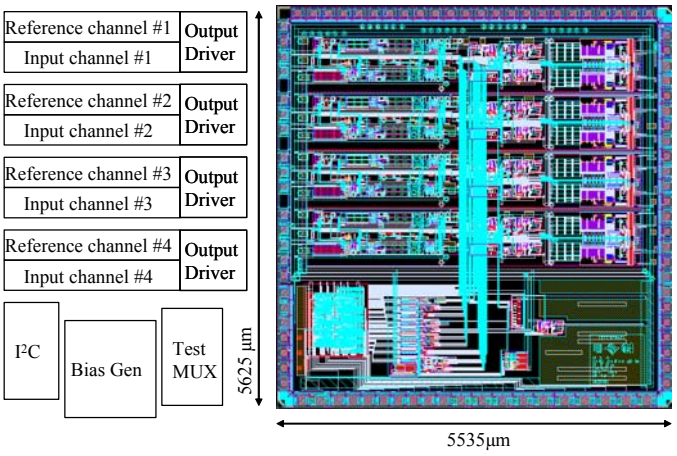

Figure 1: The F-CSA104 Floor plan & Layout.

5V CMOS process as it offers a large signal output voltage swing, substrate isolated NMOS and PMOS FET devices that

[1] The data sheet can be found at http://www.fbe-asic.com/solutions/assp/f-csa104.html

allow an improved noise immunity and, most importantly, do not exhibit bulk effect, which in combination with low temperatures causes prohibitory large changes in the threshold voltages. Figure 1 shows the F-CSA104 floor plan and layout. Each of the four input channels has, except for the scaled-down input FET and unity gain, an identical reference channel for DC subtraction.

Figure 2 shows the F-CSA104 block diagram. Charge delivered by a semiconductor detector is collected and amplified by the CSA. Its output voltage V_{out} is given by $V_{out} = q/C_{fb}$, where q is the charge delivered to the input and C_{fb} is the feedback capacitance (1pF after calibration).

A range of F-CSA104's parameters (all having room temperature start-up defaults pre-programmed), including offset and the CSA decay constant, can be programmed via I^2C commands for optimisation. Further to this, several options exist to select various reference points for sensitive nodes. An example of this would be the bulk node, labeled as BULK_EXT in Figure 2, of the input transistor which can be selected to the external bulk or the quiet ground point. The linearity and offset have been designed for use with 14 bit ADC systems. The high current differential line drivers allow for directly driving a 100Ω twisted pair cable over 10m.

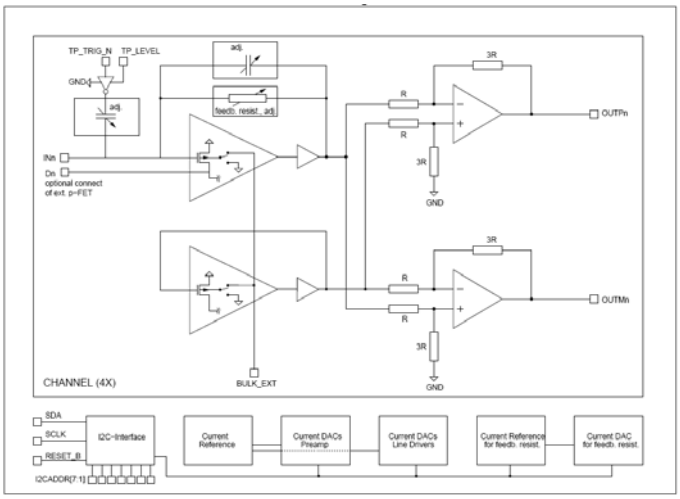

Figure 2: The F-CSA104 Block Diagram.

The internal current source has been designed to be insensitive to -200°C to +50°C temperature variations. Circuit biasing is achieved with 5-bit binary weighted current DACs utilising the current reference, followed by multiple current buffers for on-chip distribution. An internal test pulse circuit has been incorporated to allow functionality tests.

A. Integrated feed back resistor (Rfb)

A feedback resistor sets the DC operating point of the CSA, thus preventing it from going into saturation as a consequence of leakage current or high rate input pulses. For best noise performance, the feedback resistor should be as large as possible. However, this is limited by the need to avoid the CSA saturation just discussed. So as to cater for numerous input pulse rates, it is therefore desirable to untilise a wide-ranging-variable resistor for noise optimization.

It is advantageous to have a completely integrated circuit. Measurements have shown that the use of discrete components within the cryogenic vessel greatly reduce the radio-purity. For example, external components such as a carbon resistor for Rfb typically have in the order of 100 times more radioactive impurities than its integrated counterpart. However, integrating such a large resistor required the use of a substrate isolated NMOS (NMOSi) FET operating in the sub-threshold region. The resistance is adjustable from 1MΩ to 1.7GΩ.

Special electronic circuitry and layout has been used to allow the NMOSi FET resistor, labeled Rfb in Figure 3, to work in the sub-threshold region for both signal input polarities, selectable or autonomously, and to maintain a reasonably accurate and stable resistance. Sub-threshold FET operation is now briefly discussed.

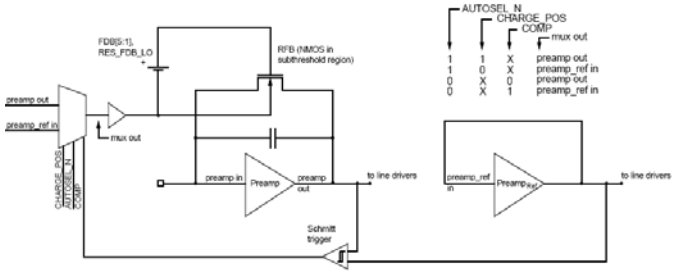

Figure 3: The NMOSi FET Feedback Resistor.

When $V_{GS} < V_{th}$, where V_{th} is the threshold voltage of the device, according to the threshold model, the transistor is turned off, and there is no conduction between drain and source. In reality, the Boltzmann distribution of electron energies allows some of the more energetic electrons at the source to enter the channel and flow to the drain, resulting in a sub-threshold current that is an exponential function of gate-source voltage and is given as [2]

$$I_d \alpha \exp\left(\frac{V_{GS}}{n.V_T}\right), \qquad Equ\ 1$$

where V_T is the temperature voltage derived from $V_T = (k.T/q)$, k is the Boltzmann constant, T the absolute temperature, and q the electron charge. The slope of the line is named 'sub-threshold slope' with the symbol n. From *Equ 1* it is clear that a stable V_{GS} is required. Furthermore, as the FET-channel conduction due to V_{GS} also has a dependency on the voltage between the source terminal and the bulk (V_{sb}), a stable and constant V_{sb} is also called for. How this is achieved in hardware is now described.

Referring to Figure 3, the very small value of V_{GS} needed to keep Rfb in the sub-threshold region is generated by a current mirror diode-connected configuration, which is a 10-times scaled version of Rfb. Both FET devices are within the same bulk area for better device matching. To maintain a fixed Rfb resistive value, tracking circuitry connected controlling the feedback MUX ensures that, in the case of positive input polarity operation, both NMOS bulk and gate voltage follow the negative going CSA output pulse, while N-tub has a fixed reference value. This ensures that V_{GS} and V_{sb} of Rfb remains a constant value. For negative input polarity, the N-tub tracks while the P-tub has the fixed reference.

B. Input transistor

The F-CSA104's noise performance has been optimized for use with detectors having a load capacitance of 0 - 100pF. Measurements have shown that the PMOS input transistor suffered less flicker noise than that of an NMOS **[3]**; Flicker noise being an important noise contributor at LAr temperatures. The total series voltage noise (e_n^2) for the input FET is **[4]**

$$e_n^2 = \frac{K_f}{C_{ox}^2 WLf} + \frac{8}{3}kT\frac{1}{g_m}, \qquad Equ\,2$$

where C_{ox} is the capacitance between the gate and the conduction channel, K_f is the flicker noise coefficient, WL are the FET width and length dimensions respectively, f is frequency in Hz, k is the Boltzmann constant, T is the temperature in Kelvin, and g_m is the transconductance given by $g_m = \sqrt{2k'(W/L)}.\sqrt{I_D}$, with k' being the process conduction parameter. The total parallel current noise source (i_n^2) representing shot noise is negligible for a FET device and is not discussed further. The first term in Equ 2 represents the flicker noise of the input transistor and the last term represents the input transistor channel thermal noise. It is clear that both flicker and thermal noise can be reduced by utilising a large width over length input FET. In this case a

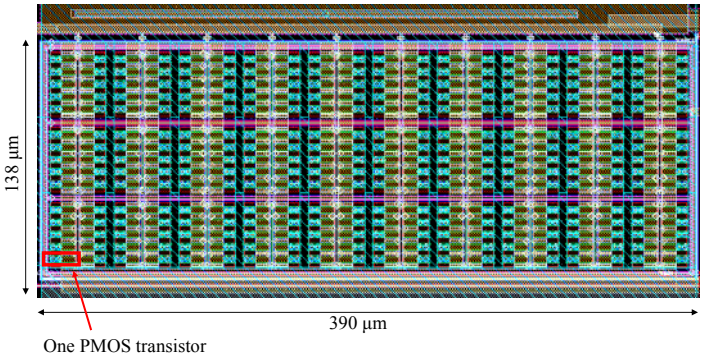

Figure 4: The NMOSi input FET.

PMOS input transistor channel of 9000/0.6 has been implemented using 600 parallel FET devices, see Figure 4. Special layout techniques have been used to reduce the stray capacitance and to screen the input line from bulk noise. So as the F-CSA104 may find use in other applications where the noise matching to higher capacitance detectors is vital, an external PMOS or a p-channel JFET may be connected to the IC and thus operates in place of the integrated input transistor, refer to the Dn input node of Figure 2.

C. Source degeneration resistor

Figure 5 shows a conceptual view of the input stage of the CSA. In principle it is of the folded cascade type, M1 being the large W/L input transistor just discussed in section B, M4 is operating as a constant current source, M3 is in a common gate configuration, M2 is the active load resistor of M3 and R1 is the degeneration resistor, the reason for its use is now given.

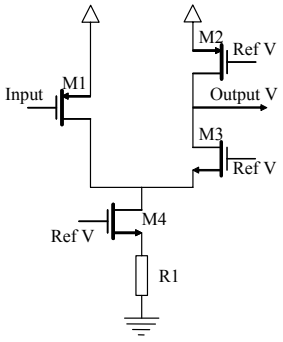

Figure 5: Conceptual view of the input stage.

In this configuration, neglecting other noise sources, the thermal channel noise current of M4 adds directly to M1 and can be written as **[5]**

$$i_n^2 = 4kT\gamma_1 g_{m1} + 4kT\gamma_4 g_{m4}, \qquad Equ\,3$$

where g_m is the transconductance and γ is a complex function of the basic transistor and bias conditions. In this case M4 carries the largest current, being the sum of both branches of the circuit, and its noise current can contribute a noticeable portion to the overall noise figure. One way to reduce its g_{m4} transconductance is to choose a small M4 W/L aspect ratio, but this is at the cost of a required increase in V_{GS}, which limits the dynamic range of the circuit. A better method is to 'degenerate' M4 by adding the resistor R1 in series with the source of M4. The thermal channel noise current of the M4 tail can now be written as **[5]**

$$i_{n(tail)}^2 = 4kT\frac{1}{R1} + \left(\frac{\frac{1}{g_{m4}}}{\frac{1}{g_{m4}} + R1}\right)^2 4kT\gamma_4 g_{m4}. \qquad Equ\,4$$

In the case of F-CSA104 the optimum R1 resistor value was found to be 200Ω giving, from simulation, in the order of a 20% reduction in the noise contribution. Care has to be taken of the R value selected to ensure that its own thermal noise does not significantly contribute.

D. Internal current source

A new compact, high precision, temperature-compensated, all-MOS current reference has been designed to allow the chip to work in both room and LAr temperatures. Its principle design and operation is given in the paper 'Compact temperature-compensated CMOS current reference' **[6]**. The paper discusses a second order temperature compensation obtained with a temperature-dependent current ratio using a MOS inverse Widlar current mirror. In this case the operating range is -30°C to +100°C. For the F-CSA104 the design has been enhanced to operate in the range of -200°C to +50°C with an expected mean temperature drift of 28 ppm/°C.

E. Offline filtering

The signal of the preamplifier will be digitized with a sampling rate of typically 100 MHz, enough to allow for detailed pulse shape analysis of the rising edge of signals from large germanium detectors, which have in the order of a 300ns rise time. A digital filter implementing a RC-$(CR)^n$ network with optimised shaping times of typically 10µs reduces the noise to the design value. The limitation of such a filter is to be able to cut off the low frequency noise while maintaining the broad spectrum range from the input pulse.

IV. Measured Performance Results

The F-CSA104's preliminary measured noise, signal output rise and fall times, linearity, gain and feedback resistor values are given for both room and LAr operating temperatures. Figure 6 shows a photograph of the test set-up. The F-CSA104 is mounted on, for LAr operation reasons, a flexible kapton PCB. The board has the option of supply filtering, which will ideally not be the case for the experiment. However, for laboratory testing it is a necessity. For test charge input, there exists a 15:1 resistor attenuation network that couples into a series capacitor, nominal value of 1.5pF. A surface mounted capacitor emulates the load capacitance of

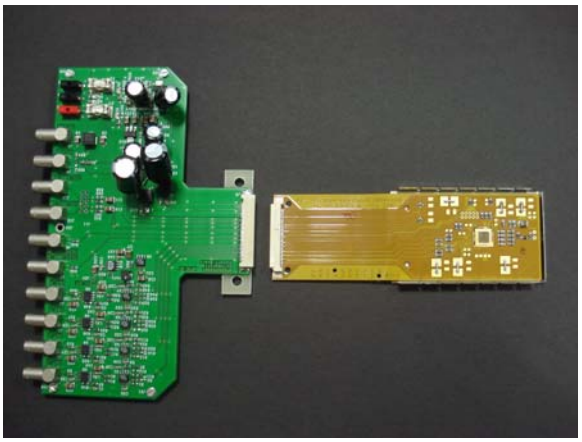

Figure 6: Photograph of the test set-up.

the diode detector. The flexible PCB can be connected to the receiver board, shown on the left side, either directly or via a 10m cable. The receiver board utilizes LM317EMP and LM317EMP voltage regulators, and 270MHz AD8130AR differential receiver amplifiers.

A. F-CSA104 resistor feedback

The measured value of the feedback resistor, discussed earlier in section II-A, has been extracted from the relationship between the amplifiers bandwidth and its feedback time constant using $R = \frac{T_{r(10-90)}}{2\pi 0.35.C}$, where C is the feedback capacitance of 1pF, after calibration. It should be noted that the amplifier's discharge slope is signal dependent and therefore only obeys a *RC* discharge curve for small input signals, but has a constant-rate discharge for larger signals. There are two modes of Rfb adjustment, the first is a fine-resolution step over the range of 10MΩ, and the second is a coarse-resolution step ranging 1.7GΩ. Figure 7 and 8, coarse and fine resolution step, respectively, are plots of *Rfb resistance vs. the resistor-select register*, for both simulation and hot/cold measurements. The input signal was ~500keV.

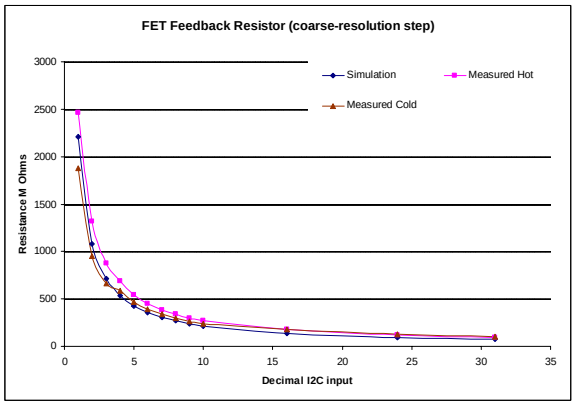

Figure 7: *R vs. coarse-resolution Rfb step settings.*

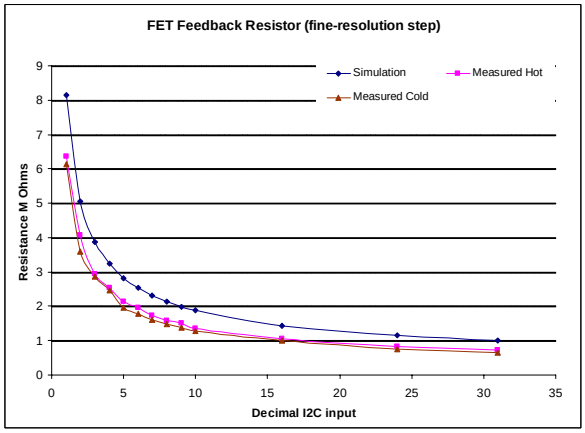

Figure 8: *R vs. fine-resolution Rfb step settings.*

As is clearly seen from these results the measured value of Rfb matches simulation well, and is only slightly effected by LAr temperature operation.

B. Noise measurements

For the preliminary noise measurements, the kapton flexible PCB had power supply filtering added, and the two boards shown in Figure 6 were directly coupled together. However, the differential receiver amplifiers were bypassed to eliminate their noise contribution. The output of each channel was shaped with a 20µs RC-$(CR)^4$ in-house-built filter and sampled by an 8-bit TDS784D oscilloscope. The oscilloscope took 5000 samples at 2.5Ms/s. To aid the removal of common mode noise, two of the channels were subtracted from each other and the single channel noise contribution was found from

$$\sigma = \frac{\sigma(Ch_A - Ch_B)}{\sqrt{2}}, \qquad Equ\,5$$

Where σ = *RMS* of scope voltage. The noise of the oscilloscope, approximately 20e^-, was also accounted for. The Equivalent Noise Charge (ENC) vs load capacitance is shown in Figure 9.

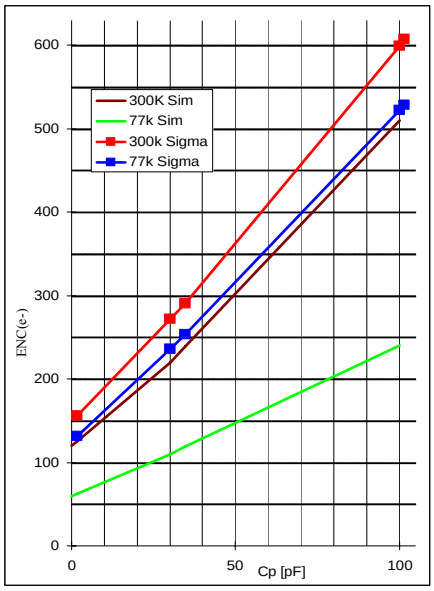

Figure 9: *ENC vs. load capacitance* noise plots.

The results for room temperature are in reasonable agreement with the simulation. However, there is evidence that this measurement is degraded due to a correlated source on the sensitive ground line. For the LAr operating temperature the result falls short of the GERDA requirements, but in this case it is plausible that the correlated source degrades the results more apparently then for the room temperature measurement. It is clear that the CMRR of the measuring circuit needs to be improved.

C. Output signal rise times

The output rise times for 10-90% have been measured with 33pF and 100pF, for both hot and cold conditions. The charge input was 22fC and Rfb set at ~100MΩ. The results are given in table 1.

Load capacitance fF	Rt_{cold} ns	Rt_{hot} ns
33	10	18
100	12	24

Table 1: Output rise time.

D. Linearity and gain

Figure 10 shows a plot of Non-Linearity (*NL*) *vs.* amplifier charge input. For the measurement of the extremely demanding linearity requirement of 0.006% a Total Harmonic Distortion + Noise (THD+N) method is utilised. THD of a signal is a measurement of the harmonic distortion present and is defined as the ratio of the sum of the powers of all harmonic components to the power of the fundamental. THD+N means THD plus noise. This is measured by inputting a sine wave and measuring both the input signal and output signal with a spectrum analyser; without shaping. In this way the proportion of *NL* relative to each output signal can be given. The circuitry resembles the IEEE standard **[7]**.

The red horizontal line in Figure 10 indicates the 0.006% requirement. The first measured point on the plot at q_{in}=0.6x10^{-18}C is the measured output without any input charge signal. The results show that the chips *NL* is less than the 0.006% limit for q_{in} above 5fC. Below this the noise

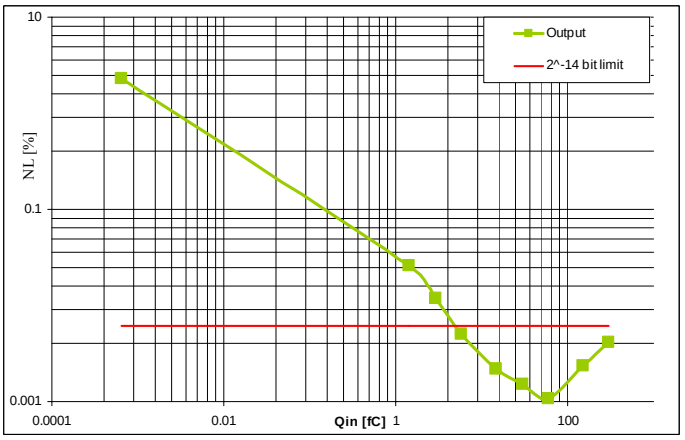

Figure 10: V_{out} *vs.* q_{in} linearity plot.

limits the measurement. One plausible explanation for the upward trend seen for input charge above 60fC is a *NL* contribution from the NMOSi feedback resistor Rfb. The measured gain is 4.75mV/fC.

V. Summary And Future Work

A four channel fully integrated low noise CSA for operation in the GERDA LAr cryogenic chamber, has been successfully designed, fabricated and tested. It is expected that the ENC noise figures will improve once the source of the correlated noise has been found and removed. The stability and dynamic resistive range of Rfb is better than the temperature limited simulation models predicted. Furthermore, its stability at very large resistor values, for both hot and cold operation, is testament to how well the constant current source behaves. The current source, full dynamic linearity, all bias nodes, the supply rejection ratio, along with all the other standard data-sheet measurements, will be fully evaluated in the near future.

VI. References

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