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Unified C/VHDL Model Generation of FPGA-based LHCb VELO algorithms

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We show an alternative design approach for signal processing algorithms implemented on FPGAs. Instead of writing VHDL code for implementation, and maintaining a C-model for algorithm evaluation, we derive both models from one common source allowing generation of synthesizeable VHDL and cycle- and bit-accurate C-Code.
We have tested our approach on the LHCb VELO pre-processing algorithms and demonstrate comparison of data processed both off-line and on-line using the two derived models.

Summary

The LHCb VELO uses silicon-strip sensors featuring 2048 strips per sensor. The analogue readout of each sensor is done using Beetle-chips. Digitisation and pre-processing at level-0 trigger (L0T) frequency of 1.1MHz is accomplished by the TELL1 board.
Different effects introduced throughout the analogue signal chain and the physical layout of the sensor do require a pre-processing prior to applying a cut to separate hits from background noise (zero suppression).
This pre-processing has been implemented in FPGAs located on the TELL1 allowing the usage of elaborate algorithms for efficient zero suppression yet guaranteeing the required throughput at L0T frequency. A Software (Vetra) written in C emulating the pre-processing allows off-line evaluation of algorithms using generated or recorded data.
As implementation or modification of algorithms for FPGAs (typically using VHDL) does require considerable more time and effort than the corresponding C-code we are concerned about the consistency between the two models rendering feedback from either model useless for the other.
To overcome this limitation, we have created a model description serving as a common source from which synthesizeable VHDL-code and cycle- and bit-accurate C-code can be derived. The language used for the common description is the Confluence hardware description language.

The most important prerequisite to make the suggested scheme work in practice are reliable interfaces, which guarantee that modified models can be immediately inserted into the respective environment (C or VHDL) without the need for further manual adaptations. If this can be achieved, turn-around times for model modifications shrink considerably. Therefore effects of modifications targeting a specific issue (algorithmic, hardware-resources ⋯) on other domains can be immediately evaluated. Iteration on hardware-implemented algorithms becomes feasible.

We will present data sets taken during the LHCb VELO Detector Commissioning Challenge (ACDC2, June 2006) and processed both off-line and on-line. Results and simulation times will be compared.

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