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An Error-Correcting Line Code for a HEP Rad-Hard Multi-GigaBit Optical Link

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This paper presents an ASIC implementing the line encoding scheme to be used in the GBT system, a multi-gigabit optical link designed for use in future luminosity improvements of the LHC. A general overview of issues specific to optical links placed in radiation environments is given, and the required properties of the line encoding discussed. A scheme that preserves the DC-balance of the line and allows forward error correction is proposed. It is implemented through the concatenation of scrambling, Reed-Solomon error-correction and addition of an 8-bit DC-balanced header. The proposed scheme has been implemented in a fully digital chip fabricated in a 0.13um CMOS technology. Implementation details and test and simulation results are given.

Summary

The Timing, Trigger and Control (TTC) system is an optical broadcast network used for fast timing and slow control distribution at the LHC. A possible upgrade of this system is under study for future luminosity improvements of the LHC. In the possible upgraded version the link will become bidirectional and the transceiver ASIC has been named GigaBit Transceiver (GBT). This new link will provide the system user with a 64-bit word every 25 ns, opposed to the 2 bits per 25 ns of the present TTC system.
In general, a line encoding scheme has to be built-in in the link in order to optimize the line data stream for the properties of the channel. E.g., a relatively high number of transitions on the bit stream has to be guaranteed in order to facilitate Clock and Data Recovery (CDR) and in particular for low clock jitter.
Additionally, the data stream has to be constituted, in the short term, of approximately the same number of zeros and ones for easy positioning of the decision threshold (property referred to in literature as the code being “DC-balanced”or “DC-free”). As in our application Single Event Upsets (SEUs)

on the photodiode are
likely to be the main source of errors, the line encoding
proposed here includes an
error correction scheme particularly targeted to this issue.
Commercially adopted
schemes have also been considered for our application,
even though none of them has
been found fully compliant with our needs, e.g. not
sufficiently efficient or
difficult to integrate with a sufficiently strong error correcting
scheme.
The proposed line encoding scheme addresses all the
previously summarized issues
through the concatenation of a parallel self-synchronizing
scrambler, a Reed-Solomon
error-correcting encoder/decoder and the addition of a DC
balanced 8-bit header used
for frame synchronization. Scrambling is a method of
randomizing the statistics of a
data stream which does not require an increase in
bandwidth. The Reed-Solomon blocks
add 16 redundancy bits to the 64-bit data packet, which
summed to the 8-bit header
lead to a total frame length of 88 bits. The total link speed is
about 3.5GHz and the
overall line code efficiency is about 73%. Low DC-wander
and high number of
transitions are guaranteed while being able to correct the
effects of at least one
SEU on the photodiode per 88-bit word.
A demonstrator ASIC implementing the encoding and
decoding functions has been
fabricated in a 0.13um CMOS technology. The whole encoder
block used about 1700 cells
and the decoder block counted about 5000, for a total area
of 1.3x1mm including the
36 pads. The ASIC has been successfully tested.

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