

## Development of a CMOS SOI pixel detector

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We are developing a monolithic radiation pixel detector using silicon on insulator (SOI) with a commercial 0.15um fully-depleted-SOI technology and a Czochralski high resistivity silicon substrate in place of a handle wafer.

Nine types of SOI TEG chips with a size of  $2.5 \times 2.5 \text{ mm}^2$  consisting of 20um pixels have been designed and manufactured.

The I-V measurement, a laser light detection test and a circuit test prove that the TEG chips function properly.

We present basic performance of the detector as well as the comparison with simulation results.

We also report the radiation effects on the TEG chips.

### Summary

One of the most important topics in the current particle physics is a search for Higgs particles and new physics beyond the standard model. In the interactions involving the new particles, bottom and charm quarks and a tau lepton play the essential role for the search.

A vertex detector placed near the beam colliding position enables us to detect and measure the decay positions of the heavy quarks and lepton precisely.

For example, LHC experiments employ a hybrid pixel detector (HPD) which is a position sensitive silicon detector, a size of about 1cm x 1cm, consisting of huge number of readout pixels of 0.1mm x 0.1mm, each is connected to a readout LSI via a bump bonding.

For future collider experiments such as ILC, super LHC, super B factory, further improvements of the spatial resolution and radiation hardness are required, however.

The harsh requirements demand a novel vertex detector that is able to overcome the difficulty in decreasing the pixel size and thickness, and the bump bonding.

One of the candidates is a pixel detector making use of the silicon on insulator (SOI) technology.

The ionizing radiation SOI detector consists of a high resistivity monolithic Si layer in place of a handle wafer, a thickness of about 100um, overlaid by a 0.2um insulating SiO<sub>2</sub> layer (Buried Oxide, BOX), and a thin Si film (device layer) over the BOX, in which a readout LSI is formed.

The handle wafer is used for a radiation sensor with a matrix of fully depleted diodes directly connected to the LSI through a hole in the BOX.

We are developing the SOI detector with a commercial 0.15um fully-depleted SOI technology and a Czochralski high resistivity silicon substrate.

Nine types of SOI TEG chips with a size of 2.5mm x 2.5mm have been designed and manufactured.

The I-V measurements, a laser light detection test and a circuit test prove that the TEG chips function properly.

We report the basic performance of the detector as well as the comparison with simulation results.

For the application of an SOI detector to high luminosity

collider experiments in future, we need understand its radiation effects. Some of the TEG chips are irradiated by gamma rays and proton beams, and total-dose and single-event effects on the chips are examined. We also present the irradiation test results in terms of the threshold voltage shift, mobility degradation, 1/f noise, sensor response on the laser light and beta rays, and the single-event-upset.

**Primary author:** ISHINO, Hirokazu (Tokyo Institute of Technology)

**Co-authors:** Dr MARTIN, Elena (University of Hawaii); Prof. VARNER, Gary (University of Hawaii); Prof. TAJIMA, Hiro (Stanford Linear Accelerator Center); Prof. IKEDA, Hirokazu (Japan Aerospace Exploration Agency); Prof. HARA, Kazuhiko (University of Tsukuba); Prof. TAJIMA, Osamu (High Energy Accelerator Research Organization (KEK)); Prof. TERADA, Susumu (High Energy Accelerator Research Organization (KEK)); Prof. KAWASAKI, Takeo (Niigata University); Prof. TSUBOYAMA, Toru (High Energy Accelerator Research Organization (KEK)); Prof. ARAI, Yasuo (High Energy Accelerator Research Organization (KEK)); Prof. IKEGAMI, Yoichi (High Energy Accelerator Research Organization (KEK)); Prof. USHIRODA, Yutaka (High Energy Accelerator Research Organization (KEK)); Prof. UNNO, yoshinobu (High Energy Accelerator Research Organization (KEK))

**Presenter:** ISHINO, Hirokazu (Tokyo Institute of Technology)

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