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The Level 0 Pixel Trigger System for the ALICE Silicon Pixel Detector

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The ALICE Silicon Pixel Detector contains 1200 readout chips. Fast-OR signals indicate the presence of at least one hit in the 8192 pixel matrix of each chip. The 1200 bits are transmitted together with data on 120 optical links using the G-Link protocol. The Level 0 Pixel Trigger System extracts and processes them to deliver an input signal to the Level 0 trigger processor within a latency of 800 ns. The system is modular and based on FPGA devices. The architecture allows the user to define and implement various trigger algorithms.

Summary

The ALICE [1] Silicon Pixel Detector [2] data stream includes 1200 Fast-OR signals indicating the presence of at least one pixel hit in each of the detector readout chips [3]. This information is used in the ALICE Level 0 trigger decision to improve background rejection in pp interactions and event selection in heavy ions runs [4].

A Pixel Trigger System has been designed to extract the Fast-OR signals from the optical data lines and process them to provide an input signal for the Level 0 trigger decision in the ALICE Central Trigger Processor. The modular electronic system satisfying the requirements is described in this paper.

The input to the Central Trigger Processor is to be provided in about 800 ns from the interaction time. This latency budget is largely used for the Fast-OR generation, the serialization-deserialization of the data and the optical transmission from the detector to the trigger system. Only a small fraction of the latency is available for the extraction and processing of the signals. A careful choice of the degree of the parallelism of the data flow is required to comply with the short latency budget while maintaining a reasonably limited number of data lines.

The Pixel Trigger System does not affect the Silicon Pixel Detector readout system. The detector data stream is divided into two optical readout lines by passive optical splitters. One output is sent to the data readout modules in the counting room. The other one is connected to the optical inputs of the Pixel Trigger System, located in the vicinity of the Central Trigger Processor.

Ten optical input boards extract the Fast-OR signals, each one receiving 120 Fast-OR bits from twelve detector modules every 100 ns. The input boards are based on optical receivers, dedicated G-Link ASIC decoders and one FPGA. Prototype G-Link receivers using only FPGAs containing on chip decoders have also been realized and tested. They did not satisfy the latency constraint.

The 1200 extracted signals are transferred to a processing board by time division multiplexing on 600 dedicated lines. Optional high speed serial output links are provided on the optical input boards. The Fast-OR signals are processed in a FPGA with a large number of input-output pins. The output of the processing unit is then transmitted to the Central Trigger Processor.

The system architecture is independent of the processing algorithm. A set of different algorithms for the generation of the input to the Level 0 trigger is foreseen. They are based on the topology of the event or on the occupancy. The system allows remote configuration of the processing FPGA to enable the definition and implementation of the algorithms by the user.

Remote control, monitoring and configuration of the system are provided by a dedicated processor on the processing board. Communication with the control room is via an Ethernet link.

References

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