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A high level modelling approach to design and manage 18 electronics configurations used for the ECAL's endcaps hardware design

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The ECAL sub detector of the CMS experiment is composed of one barrel and two endcaps. The crystals of the endcaps are arranged on an X-Y grid. Mapping signal clusters on to the eta-phi coordinate system required for the trigger therefore presents a problem. The 48 channels Trigger Concentrator Card (TCC48) is designed to compute the trigger primitives of the different parts of each endcap sector. Each card has to support 18 electronics configurations. Based on FPGA devices, an architecture supporting all possible configurations in one design will be presented. An automated approach to extract all configurations for each trigger tower will be described in this contribution. It will also be shown how a high level model based on SystemC language is used to cover all modelling and simulation aspects.

Summary

For each crystal inside the ECAL sub detector, the very front end electronics board (VFE) provides a digital version of the output signals form. Because of the endcaps geometry, the deposited energy is not summed over 25 crystals like in the barrel, but over 5 sets (pseudo strips) of 5 crystals. The results are sent by 5 high-speed links to the off detector TCC48 board. As a consequence of the eta-phi geometry of the trigger tower, the trigger tower signals are defined using a different association list (18) of pseudo strip signals depending on the phi sector. Moreover each endcap phi sector is split into an inner and an outer part. The full architecture requires 72 cards for the endcaps detectors.
- For each trigger tower of each inner and outer part of each phi sector, the pseudo strips association list is extracted from a database. From this information, a software algorithm is applied to define the right effective hardware structure. Without any manual intervention, it allows specific parameters association into a predefined generic hardware model. In addition, with this approach, a unique type of electronics card and its associated firmware can be used to cover all the configurations providing an easy maintainability of the system.
- Modelling and simulating a design that has to take into account a large set of parameters is a real problem. An approach is to use a high level modelling language like SystemC. With the NEPSYS tool from PROSILOG, we use SystemC to model efficiently and simulate our design. A close collaboration with PROSILOG to help us and include our requests in their products has been a key point to achieve our goals. The specific aspects of this design are supported by NEPSYS.

This presentation will describe a solution for an efficient modelling and simulation of a complex electronics card that must respond to many different configurations. Automated parameters extraction, hardware structure fitting and the high level modelling, experimented in this design will be presented.

Primary authors: VAUMORIN, Emmanuel (PROSILOG); ROMANTEAU, Thierry (LLR Polytechnique)

Co-authors: Mr DECOTIGNY, David (LLR Polytechnique); Mr DOBRZYNSKI, Ludwik (LLR Polytechnique); Mr BUSSON, Philippe (LLR Polytechnique)

Presenters: VAUMORIN, Emmanuel (PROSILOG); ROMANTEAU, Thierry (LLR Polytechnique)

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