The Level-0 muon trigger for the LHCb experiment

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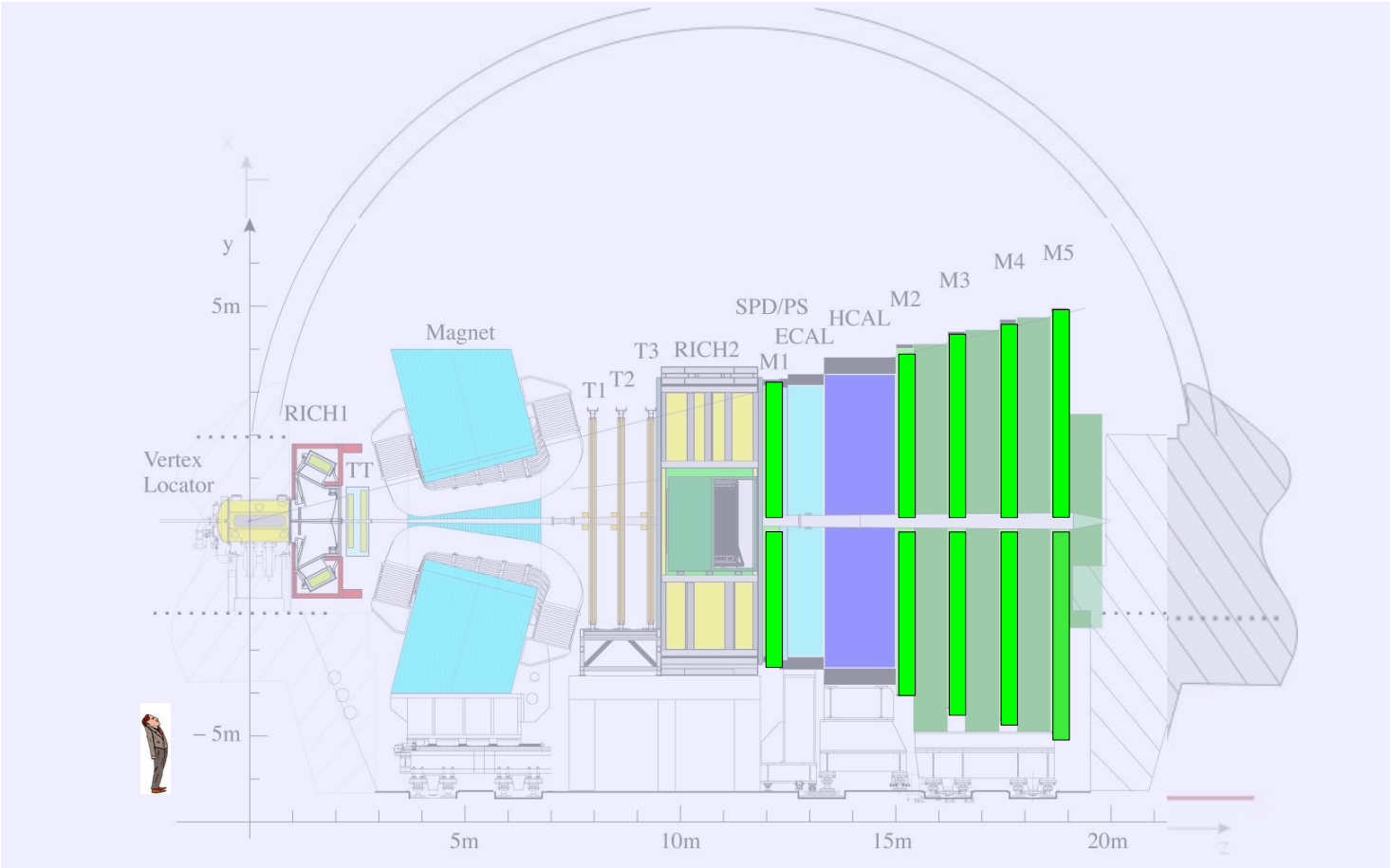

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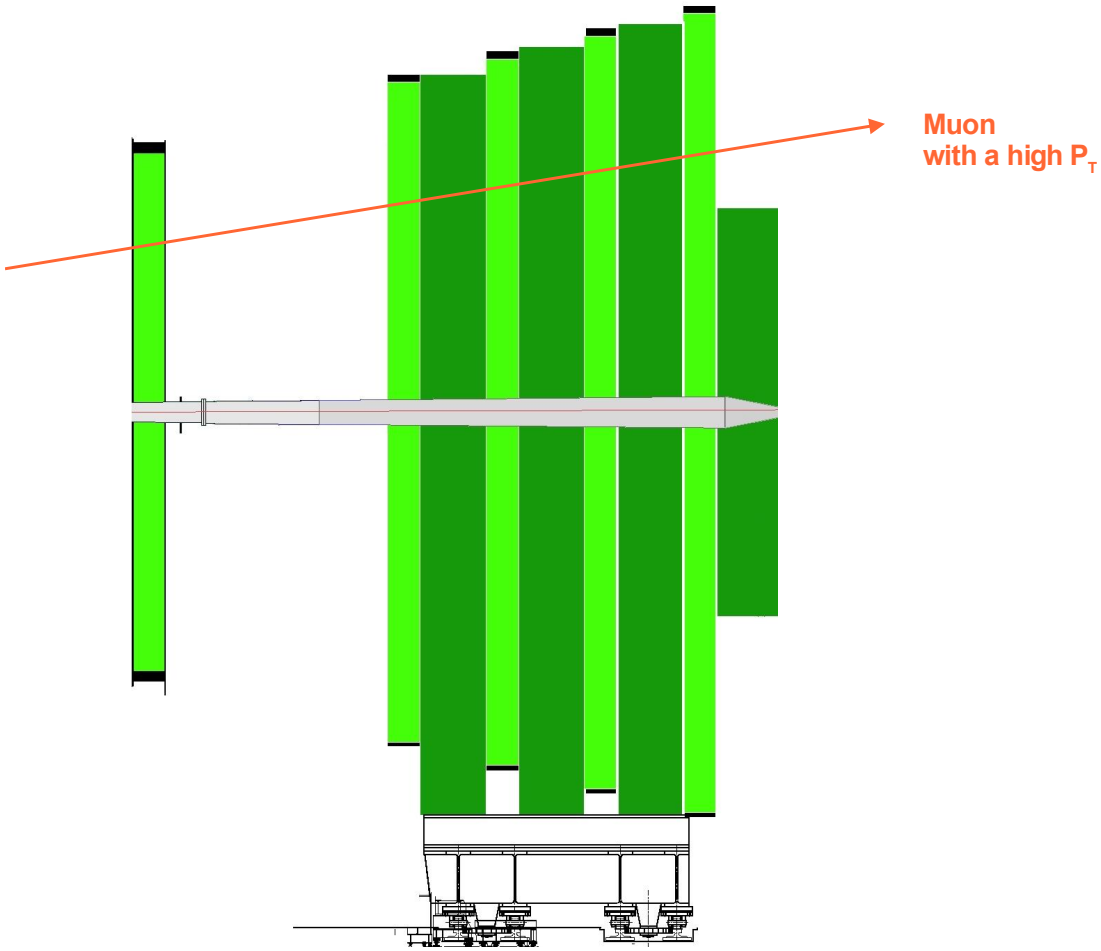
Outline

- Requirements
- Architecture
- Implementation
- Debugging and verification tools
- Conclusion

Requirements

Level-0 muon trigger overview



Goal:

- Identify B Meson decay by finding a muon with a high PT

Processing:

- Find muon tracks in the muon chambers;
- Transverse momentum calculation

Real time computation :

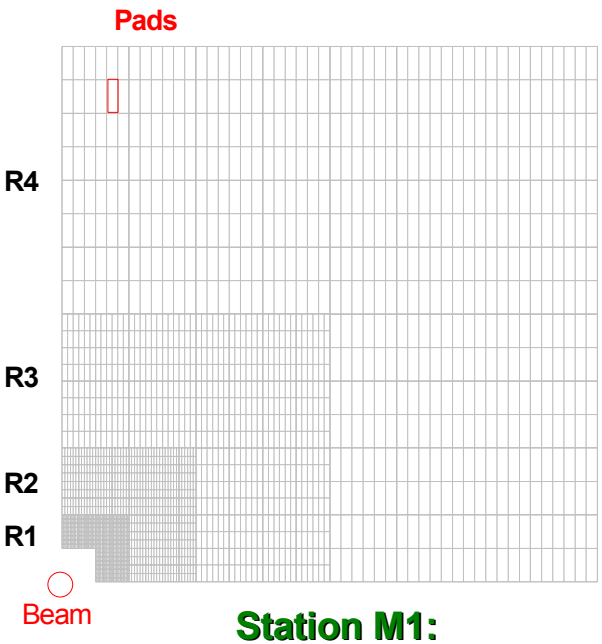
- 25920 channels sampled every 25 ns;
- Processing of 130 GigaBytes/s
- Compute a decision every bunch crossing (25 ns)
- Max processing time 1.2 µs

Detector geometry

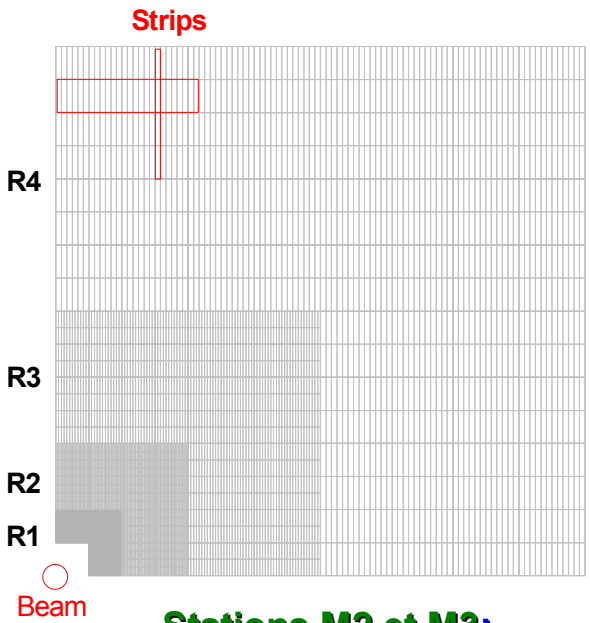
5 stations M1 to M5 :

- Channels are projective
- Granularity changes between M1, M2/M3 and M4/M5

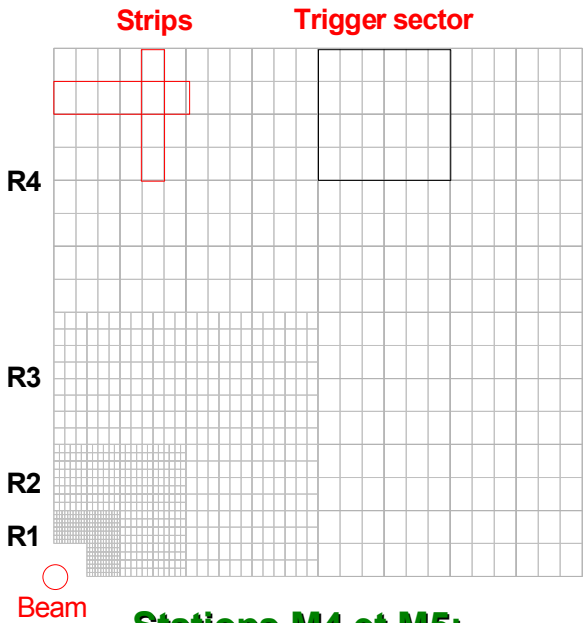
4 regions per station



Station M1:
Pads only

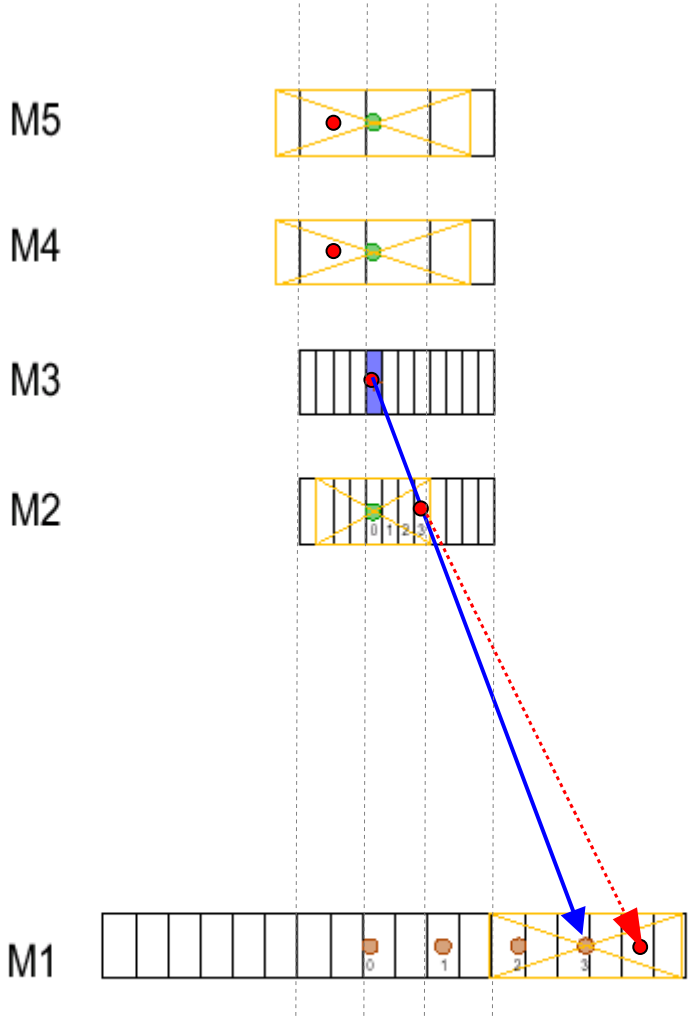


Stations M2 et M3:
Strips only
Density double wrt M1



Stations M4 et M5:
Pads and strips
Density half wrt M1

Search Algorithm

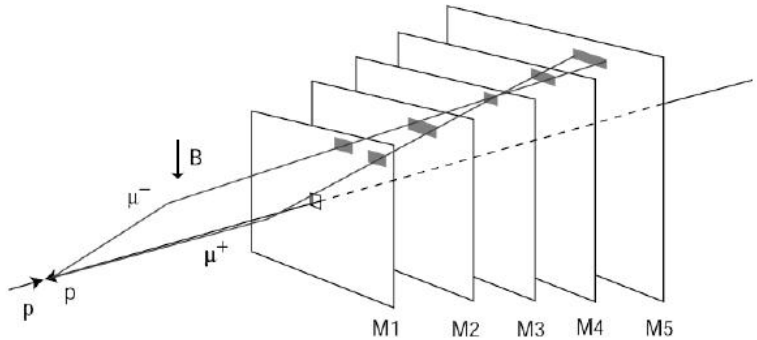


Algorithm:

- Search of hits in M2, M4 et M5 in a window centred on initial position in M3
- Search window in M1 centred on direction given by M3/M2 hits
- Search for hits in M1
- Transverse momentum is computed from the M2/M1 addresses

Projective tower structure

- **Algorithm requires only logical operations**



A complex system

A huge number of channels distributed in a large volume

Heterogeneous

- Granularity changes between regions and between stations
- Mixture of pads ans strips
- Elementary trigger processing area matches the sectors except in R1 M2/M3

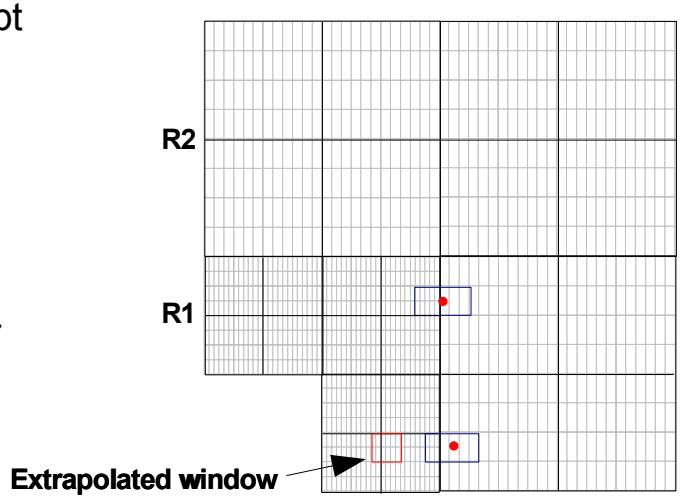
Topology of data exchanges between processing elements is complex and depend on the location

- Heterogeneity
- Horizontal exchanges for M1 to M5 and vertical exchanges for M4/M5

Processing time is short

- one result every 25 ns
- total processing time allowed 1.2 µs

Design a generic system, simple and easy to debug and to maintain



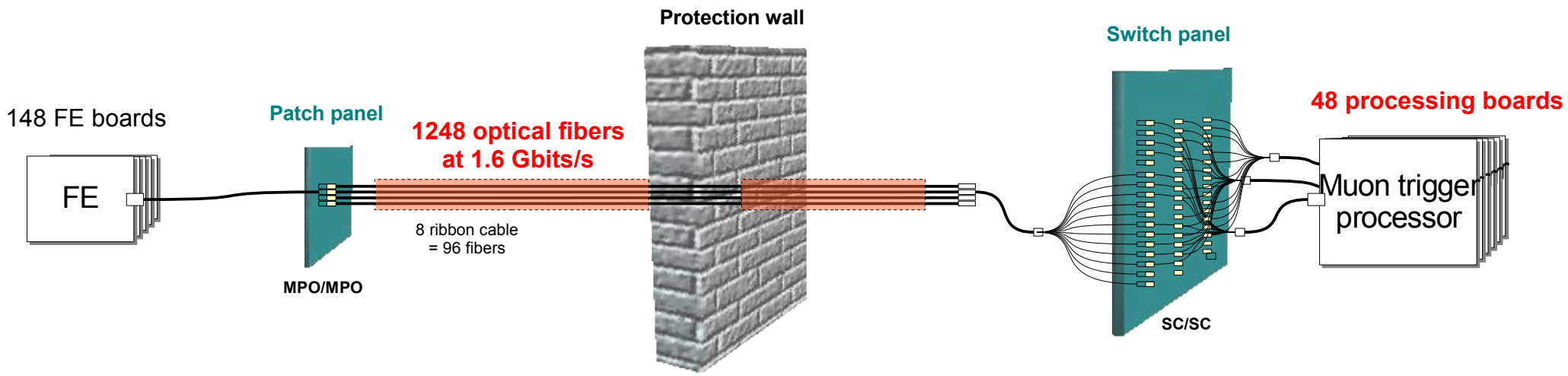
Example of hits requiring data exchanges

Architecture

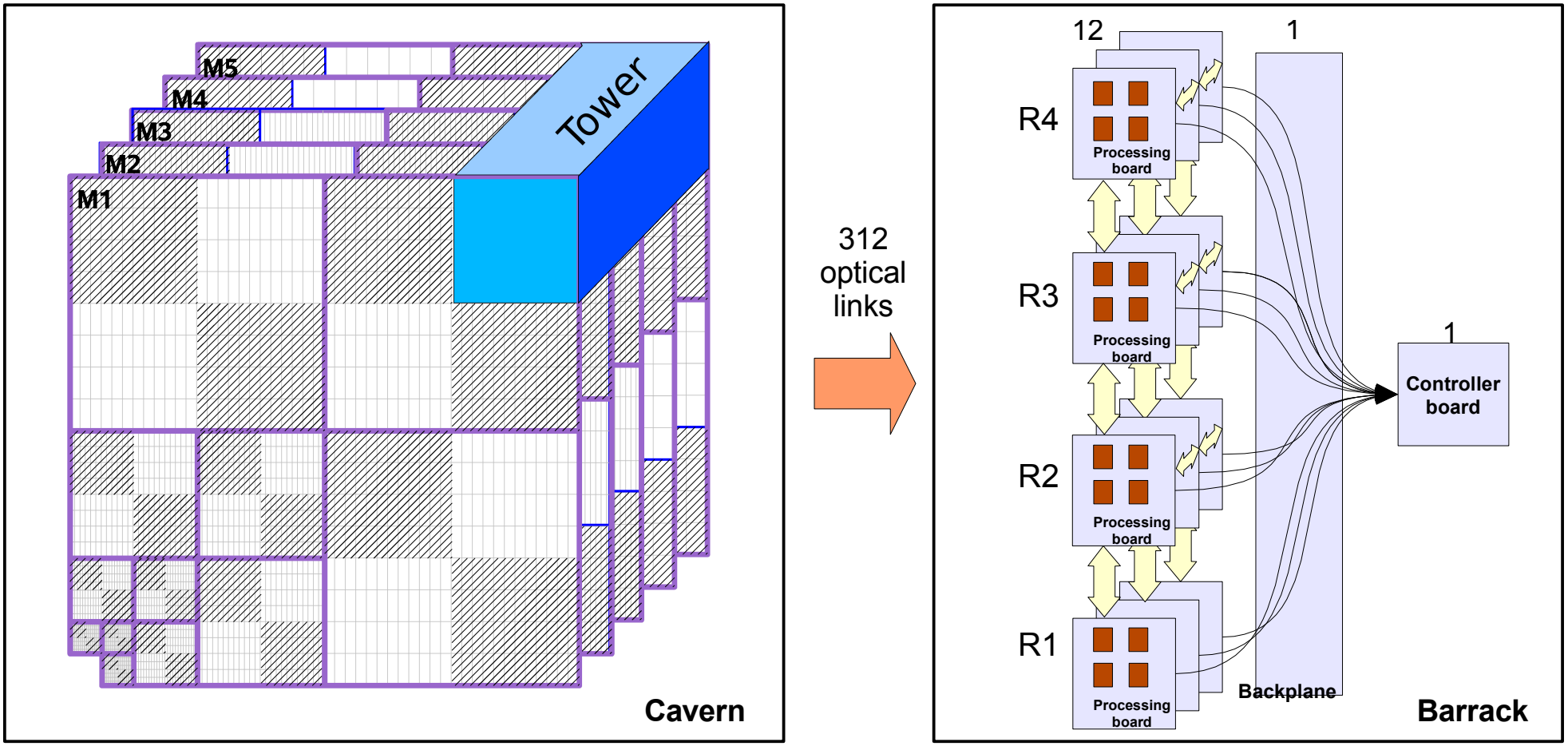
Front End ⇨ Trigger connectivity

Connection between FE and trigger designed to ease the processing

- **1248 optical links at 1.6 Gbits/s** between FE and trigger processor
- **Switch pannel** to group the sectors of the 5 stations (tower) to a single processing entity

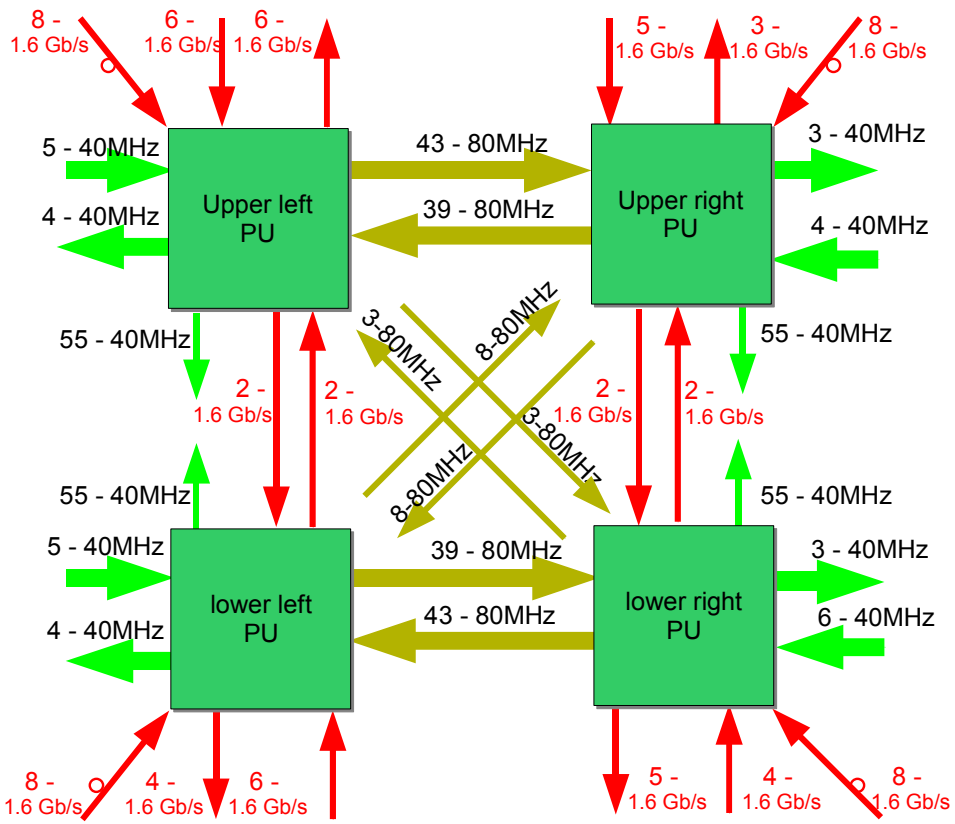


Muon trigger architecture



Architecture for a quarter of detector

Interconnections within a processing board



Legend:

- 1.6Gbps serial link
- 80MHz parallel link
- 40MHz parallel link

Processing boards

- Computes the information of towers
  - One FPGA per tower
  - Hits on a border require exchanging neighbour information
- One board executes 384 search algorithms simultaneously
- 12 processing boards for a quarter of detector

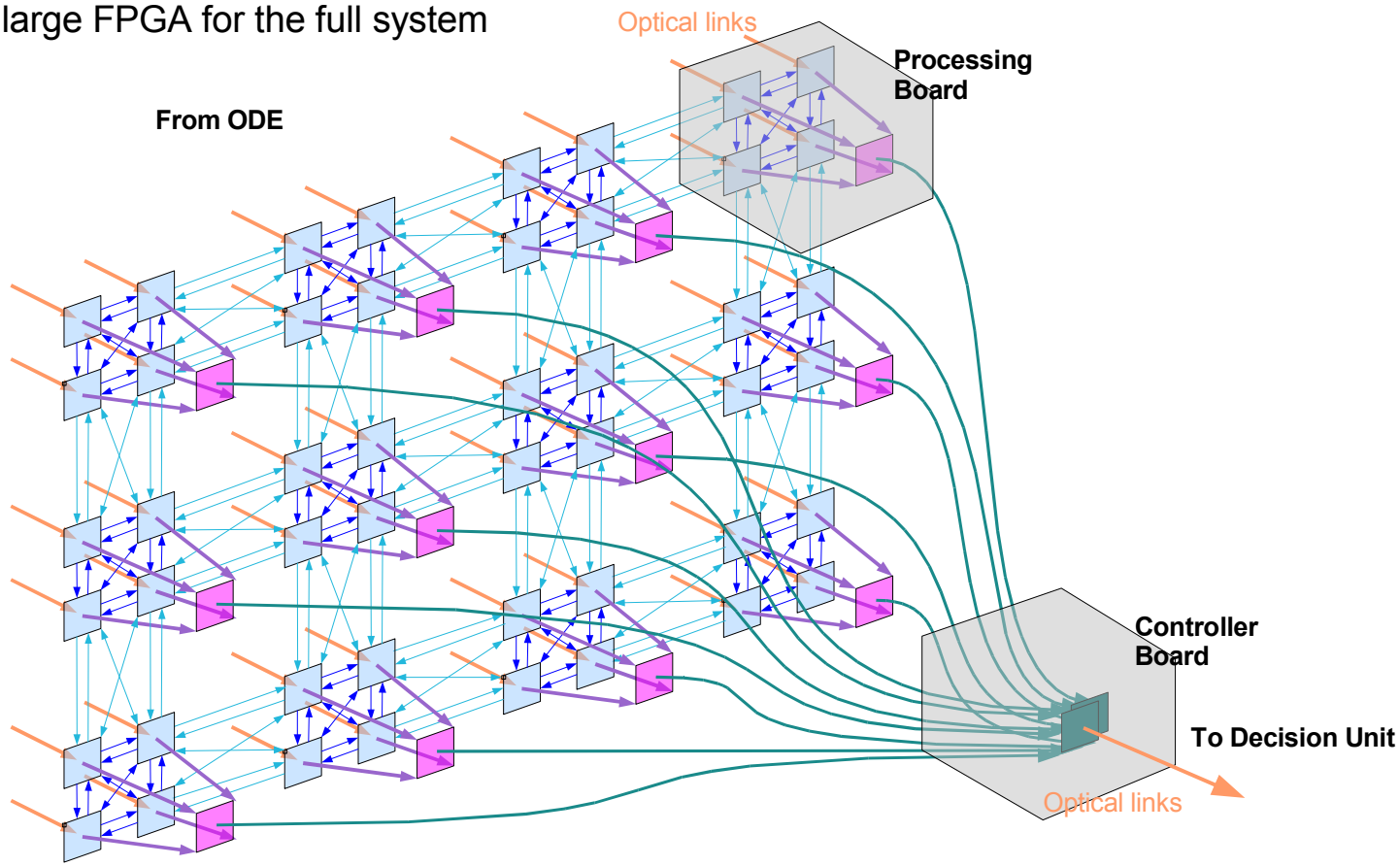
Generic architecture

- All the processing boards are identical
- FPGAs programmed according to location of the board
  - 48 configurations

Data flow within a processor

62 large FPGAs interconnected together for a quarter of detector

- 248 large FPGA for the full system

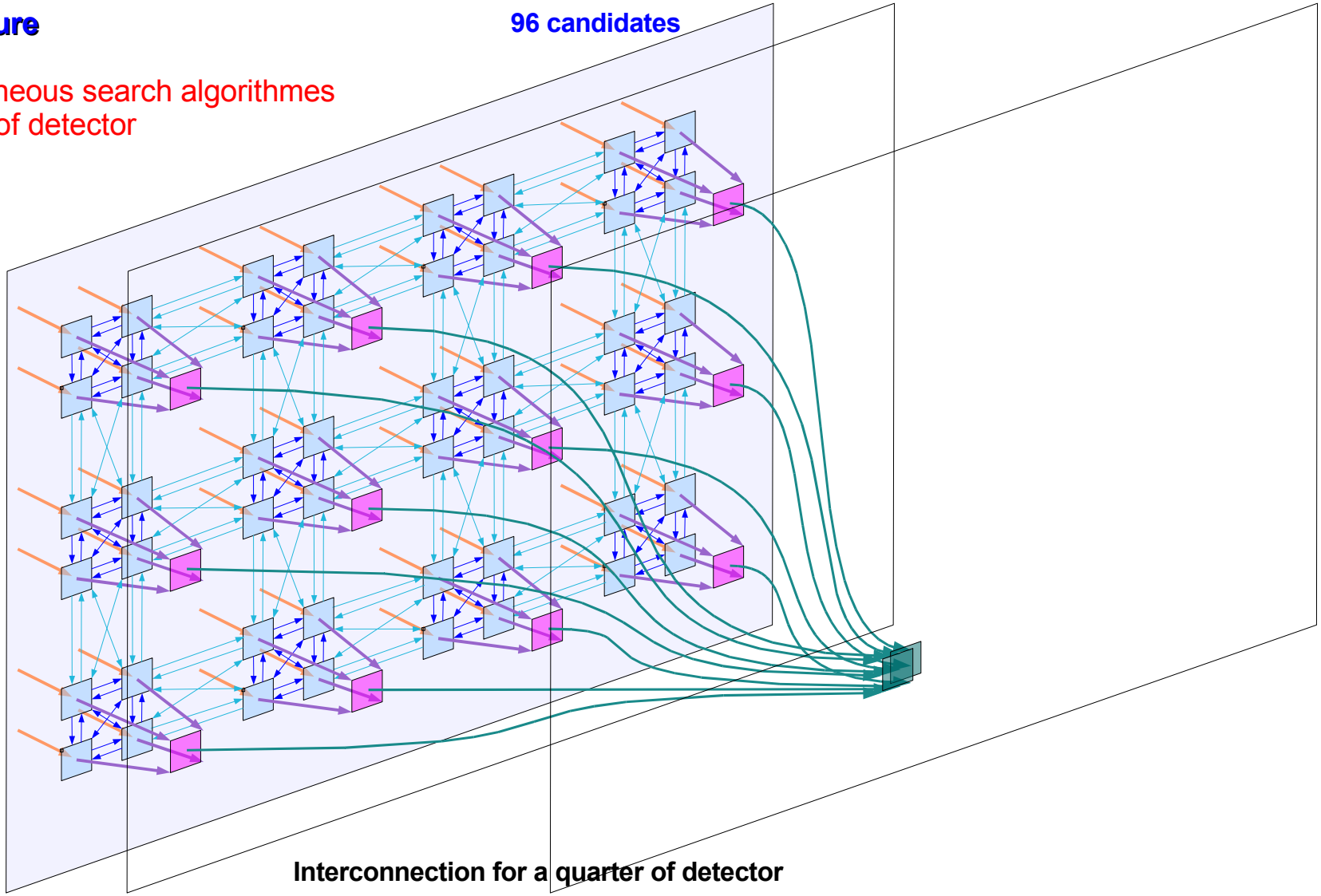


Interconnection for a quarter of detector

Data flow

Pipeline architecture

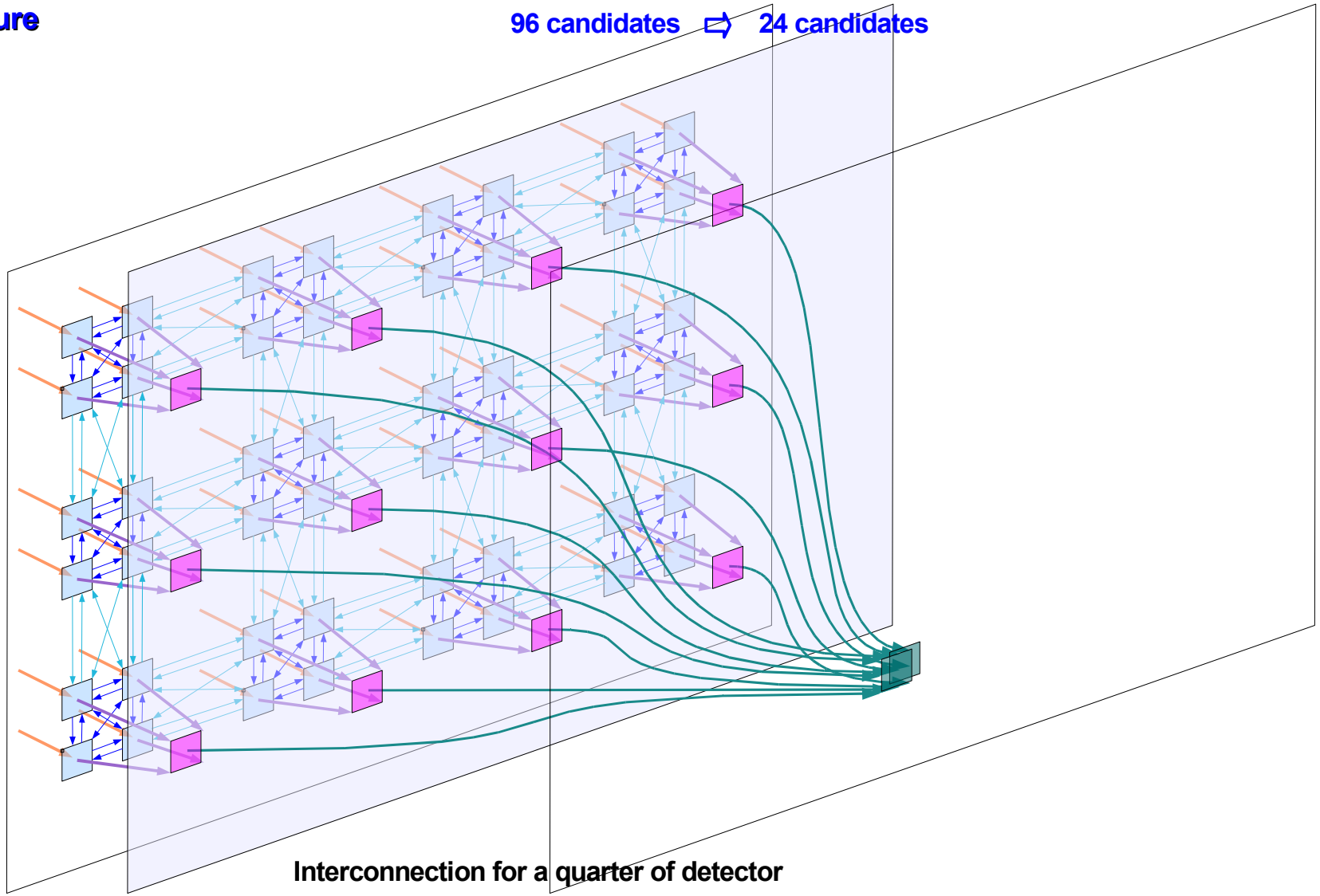
4608 simultaneous search algorithmes
for a quarter of detector



Data flow within a processor

Pipeline architecture

96 candidates ⇨ 24 candidates

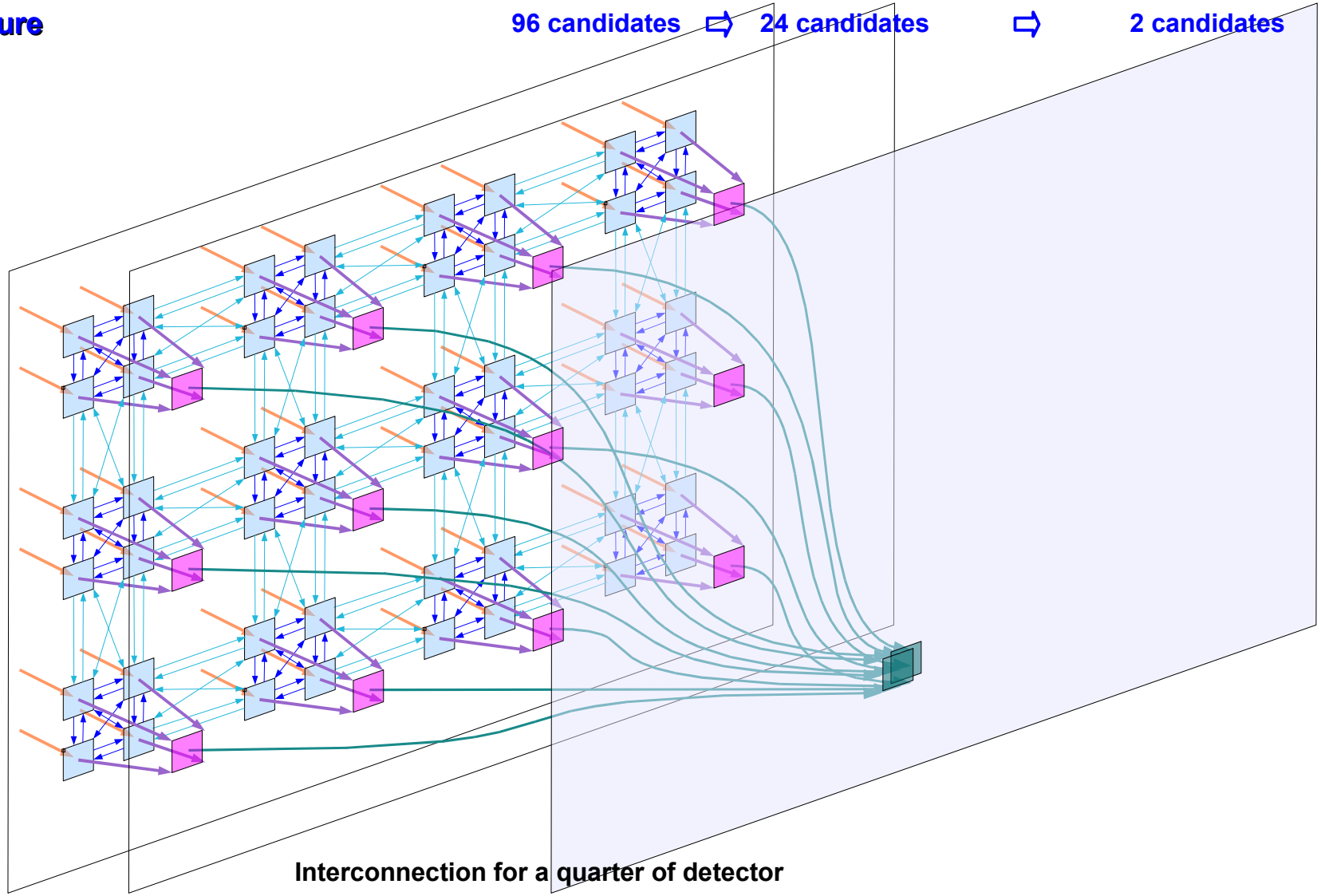


Interconnection for a quarter of detector

Data flow within a processor

Pipeline architecture

96 candidates ⇨ 24 candidates ⇨ 2 candidates



Interconnection for a quarter of detector

Implementation

Massive use of serial links

Serial data at 1.6 Gbits/s

- Divides the number of connections by a factor 16

Optical communications

- 1248 optical inputs from the ODE boards @ 1.6Gbps
- 104 optical outputs to Tell1 and to L0DU @1.6Gbps

Neighbour exchanges within the L0 Muon Trigger Processor are made on high speed serial copper links

- 90 copper links on a single board processing @ 1.6Gbps
- 110 copper links trough a backplane @ 1.6Gbps

Technical choice

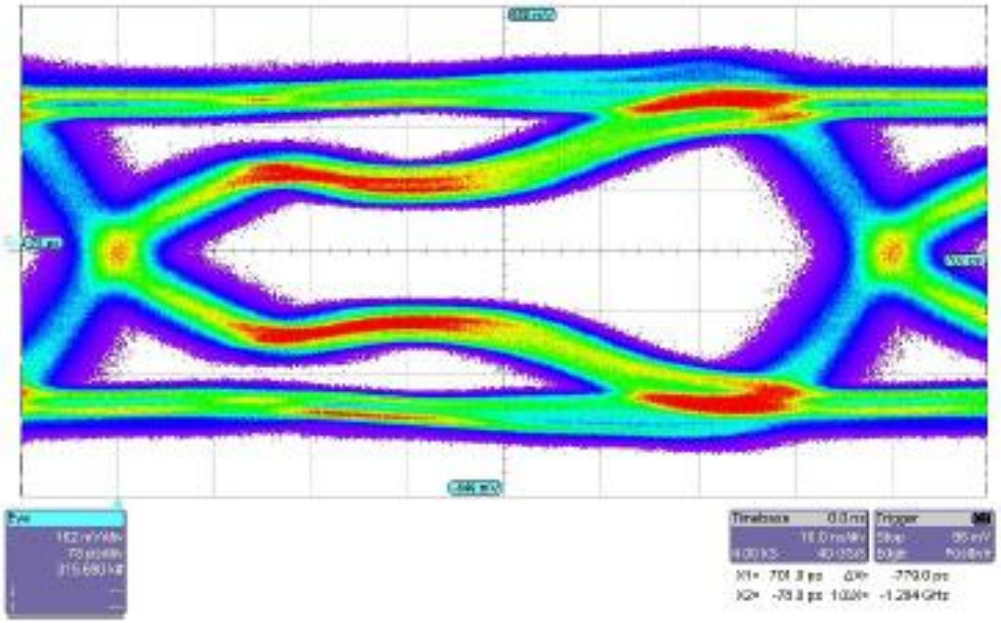
StratixGX FPGA from Altera

BGA 1020 pins
16 bidirectional SERDES at up to 3.125 Gbits/s

Performances

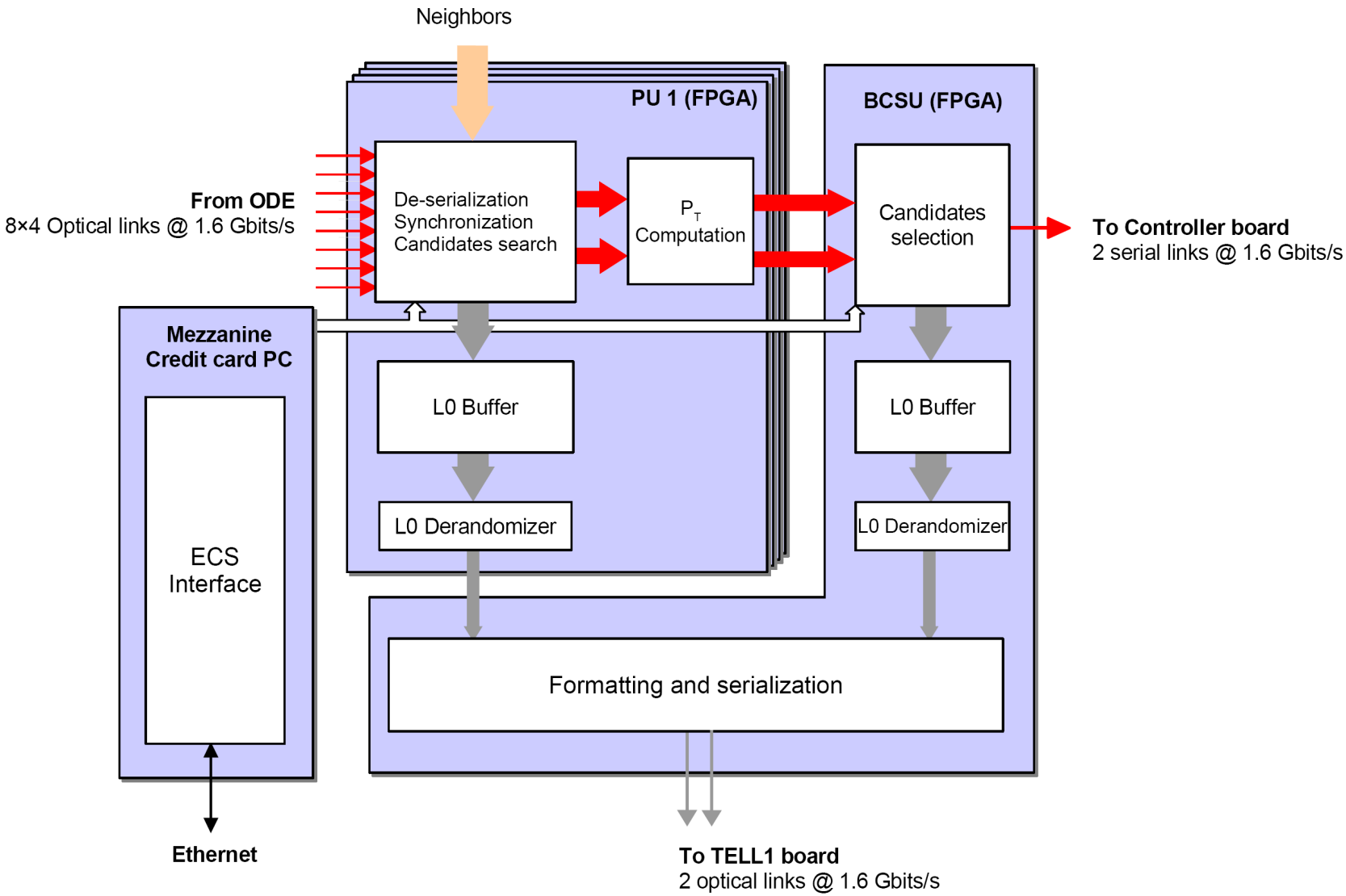
Measured bit error rate below 10^{-16}

Hundreds of links run without error for weeks

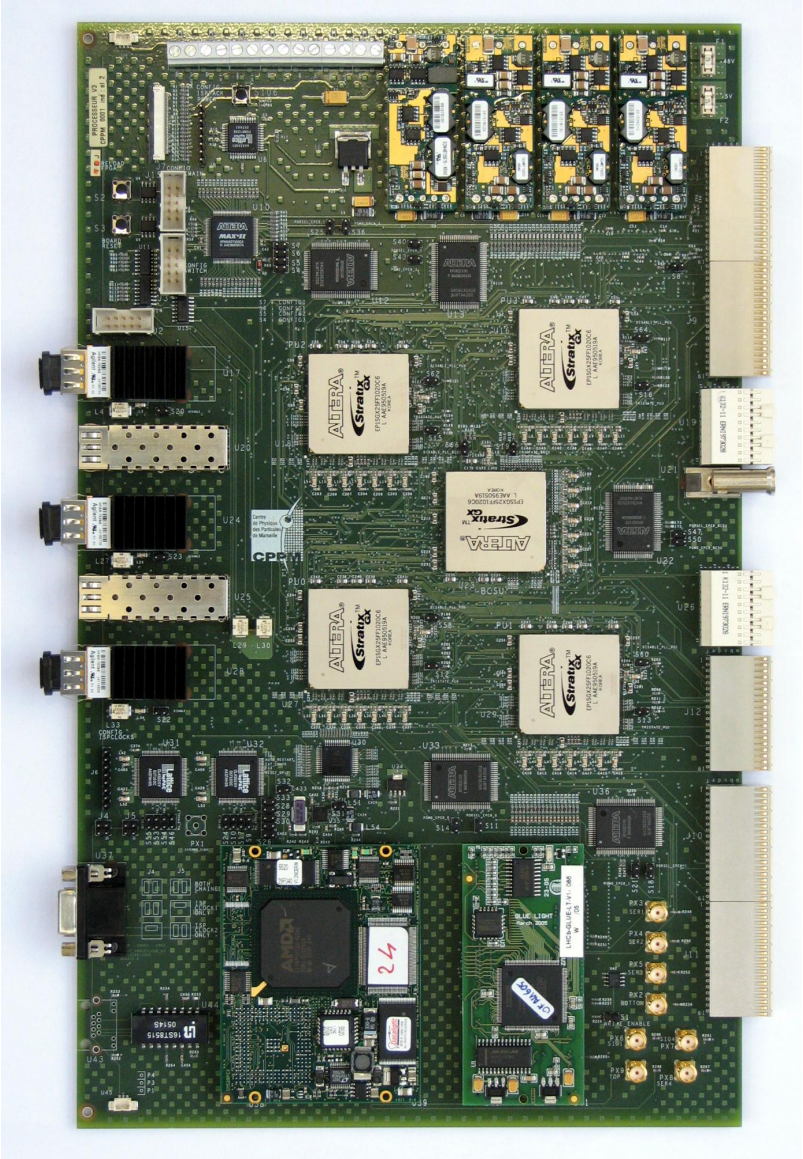


Eye diagram of a backplane serial link at 1.6 Gbits/s

Processing board

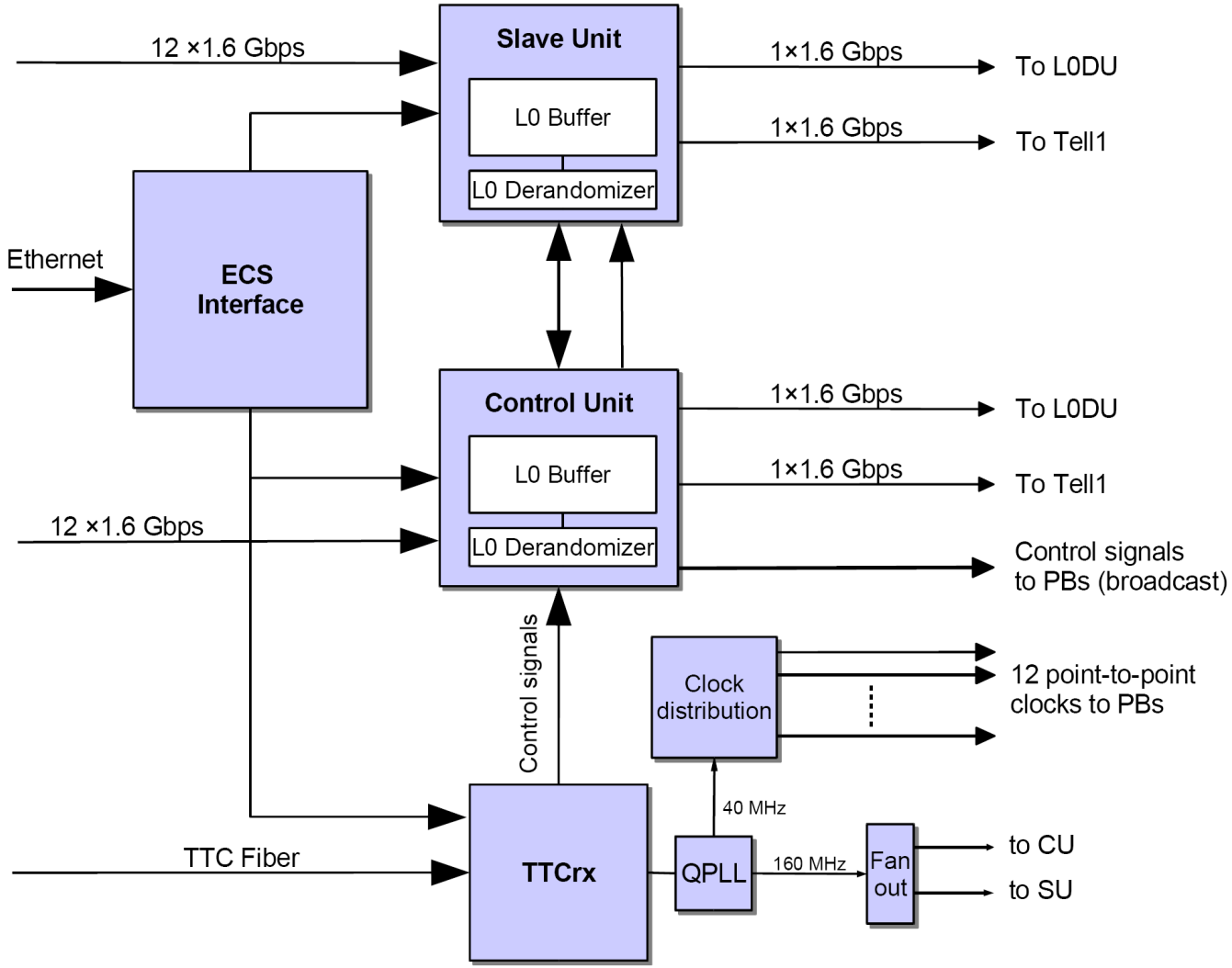


Processing board characteristics

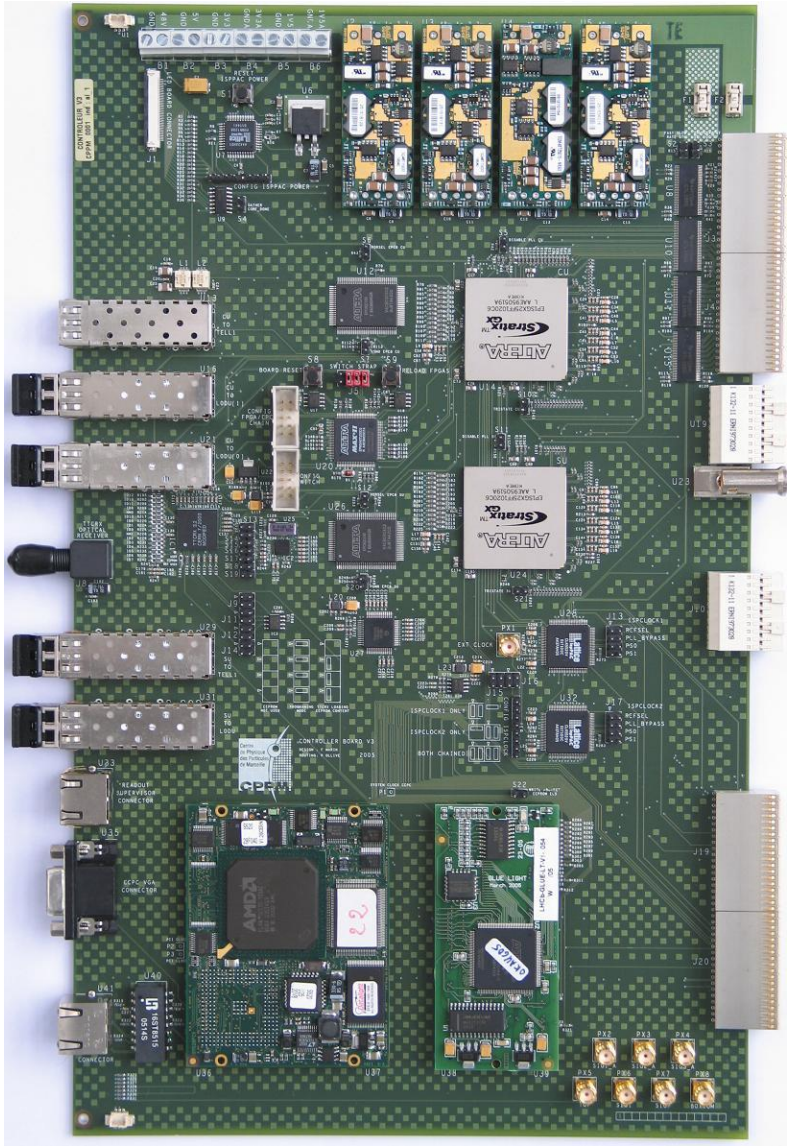


- 9U board (366.7mm x 220mm)
- 18 layers
- 90 differential signals @1.6Gbps
- 5 StratixGX EP1SGX25FF1020-C6
- 1512 components
- Consumption < 60W

Controller board

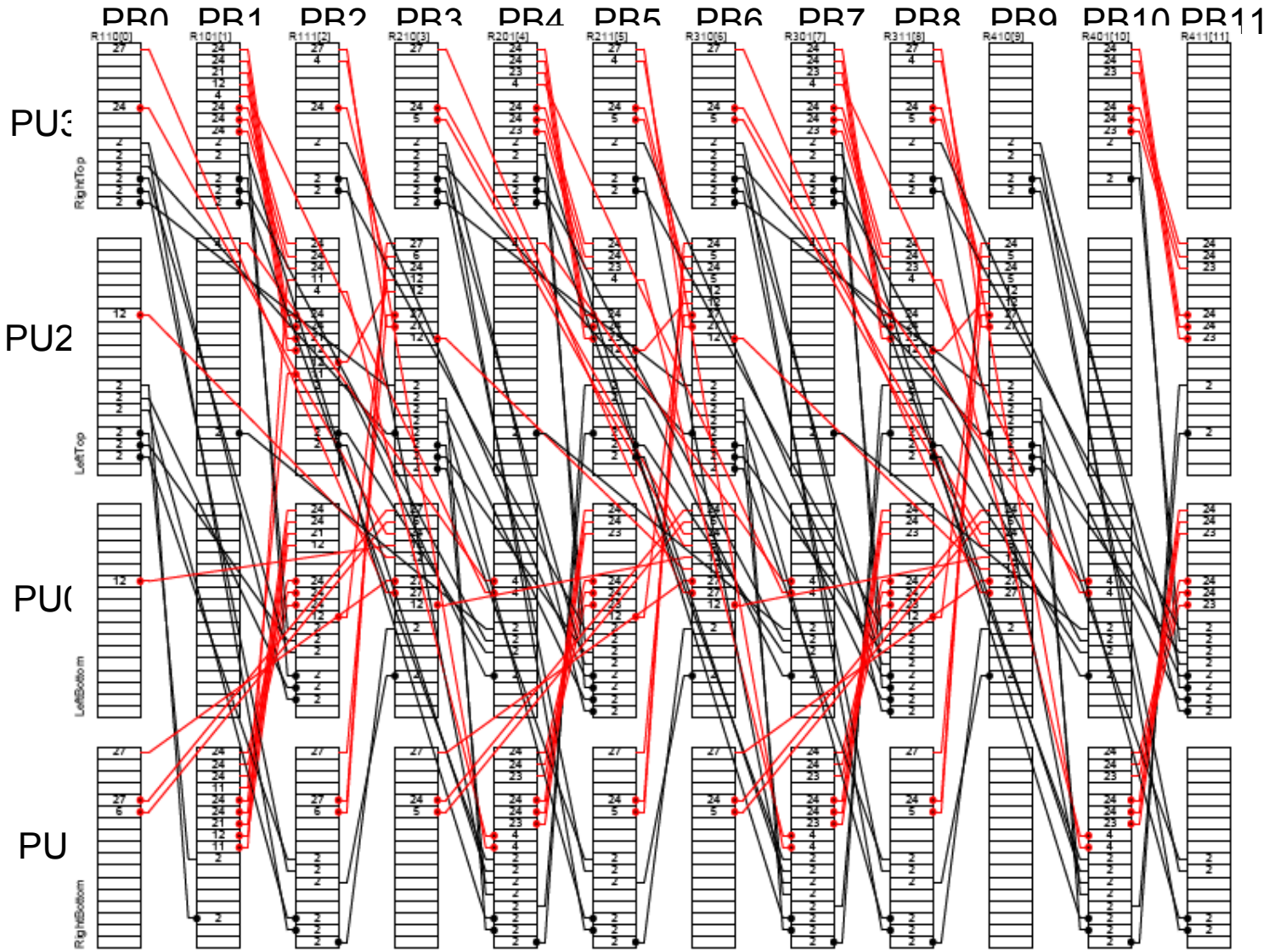


Controler board characteristics



- 9U board (366.7mm x 220mm)
- 14 layers
- 36 differential signals @ 1.6Gbps
- 2 StratixGX EP1SGX25FF1020-C6
- 948 components
- Consumption ≤ 50W

Backplane : PU interconnection matrix



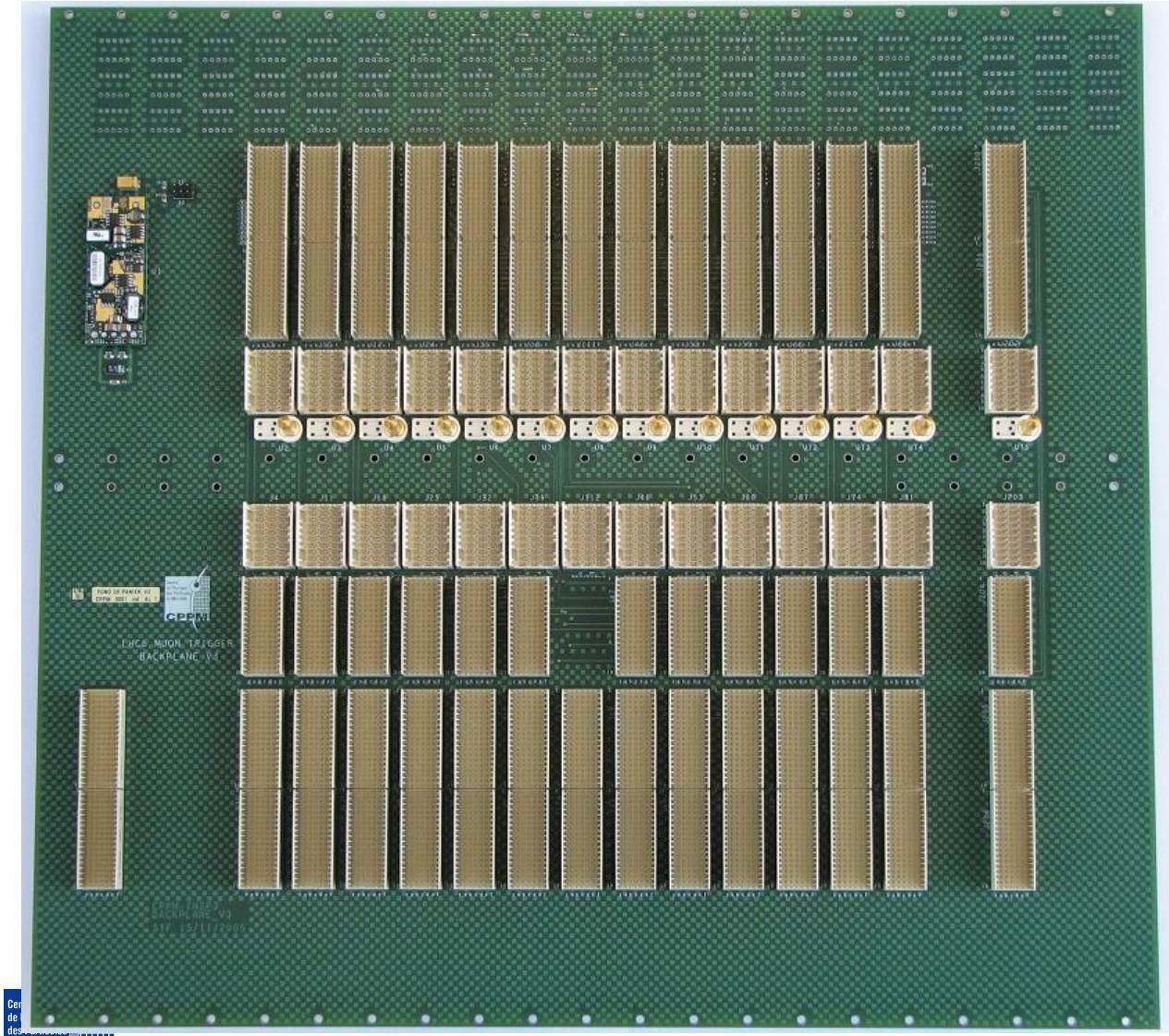
- 110 serial links
- 288 parallel links

Legend:

Parallel link to

Serial link to

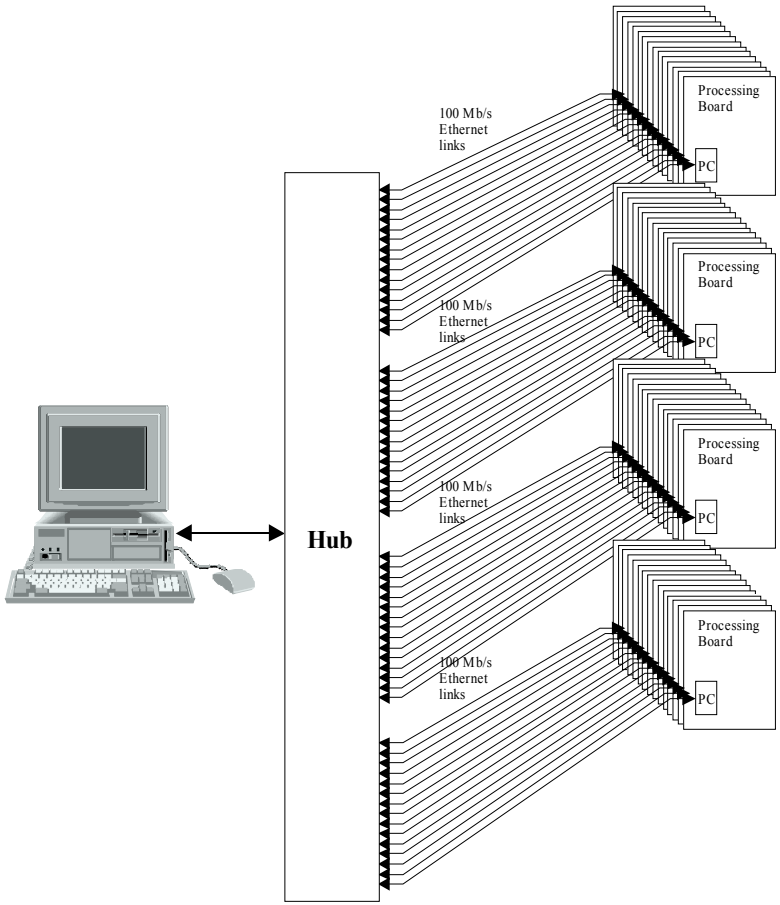
Backplane characteristics



- Size: 395.4mm x 426.72mm
- 18 layers
- 110 differential signals @ 1.6Gbps

Debugging and verification tools

Slow control



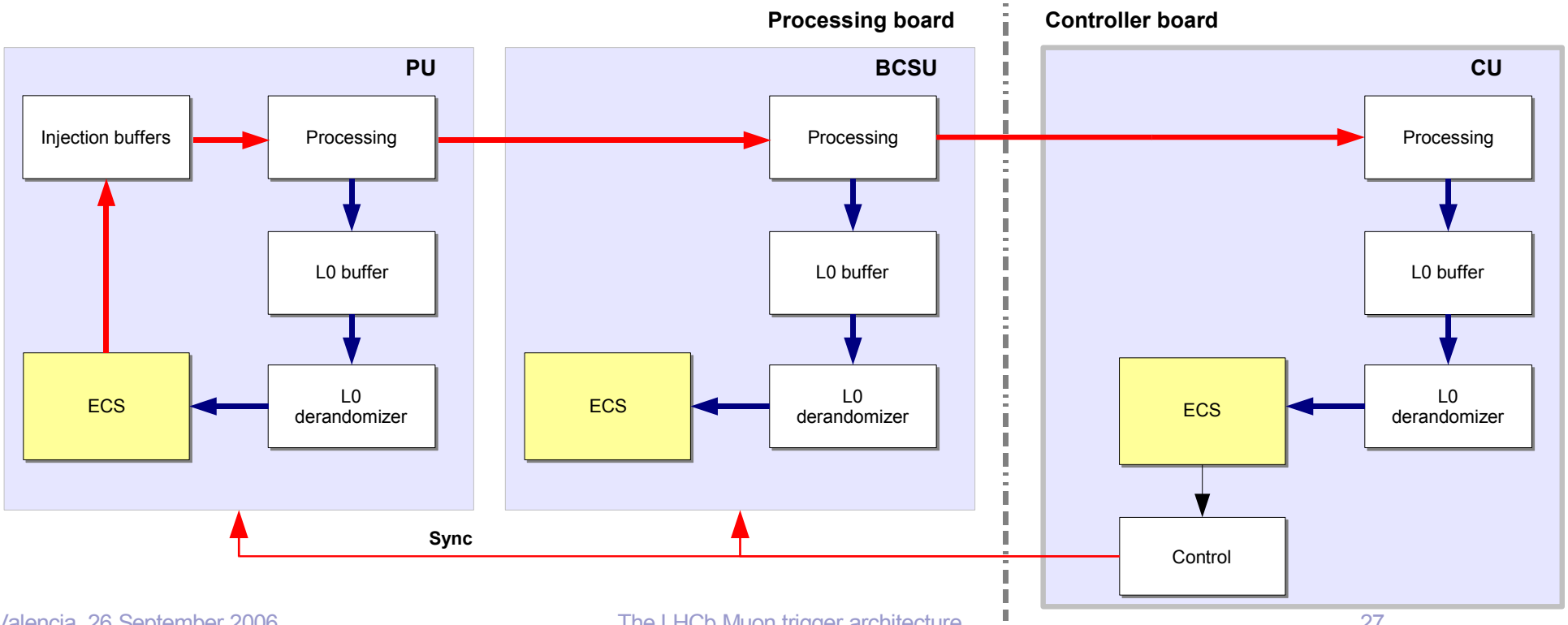
System control

- Embedded « Credit card PC » on each board
- Runs Scientific Linux
- Connected to control system through an Ethernet link
  - **Key component for debug**

Testability

Possibility to inject simulated data and read back

- Data are fed at the PU stage
- They can be read back at several places:
  - **Gives a complete visibility on all stages of the dataflow**



Verification

Very complicate system

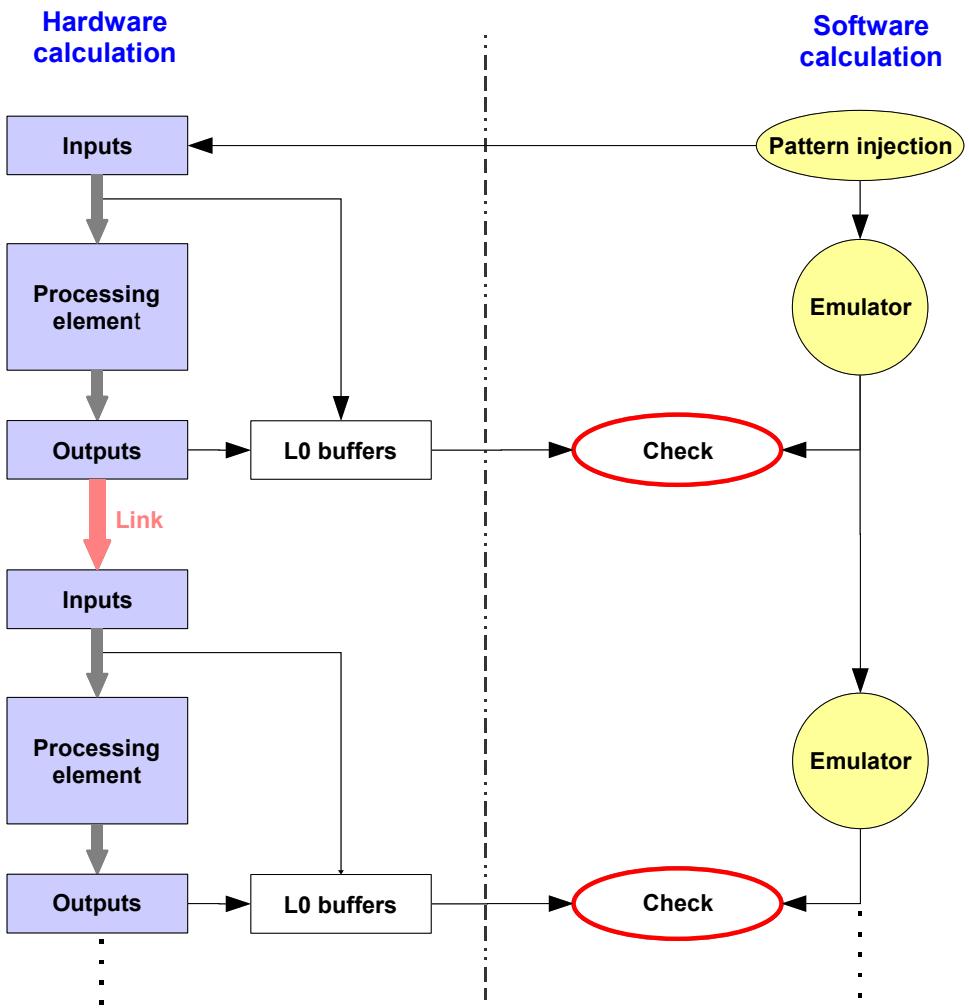
- need to understand what happens

Human check nearly impossible:

- at PU level: ~ 512 bits per event
- at board level: ~ 2300 bits per event
- at crate level: ~ 30000 bits per event

Software emulation of the processing allows a bit to bit comparison

- **Hardware/software crosscheck of the algorithms**
- **Can be run in background during data taking**



Conclusion

The muon trigger is a very complex system

- A challenging architecture has been developped
  - **2272 high speed serial links at 1.6 Gbits/s** for the full trigger
    among which 920 component-to-component or board-to-board copper links
- All tests demonstrate that **the hardware is fonctional**:
  - data path integrity exhaustively checked
  - **multigigabit serial links prove to be very reliable**
- We have developped tools that should help us facing the complexity

Production is on-going

The muon trigger will be installed in the experiment first quarter 2007