Contribution ID: **64** Type: **Oral**

The Level-0 muon trigger for the LHCb experiment

Tuesday, September 26, 2006 2:40 PM (25 minutes)

The Level-0 muon trigger looks for straight tracks crossing the five muon stations of the muon detector and measures their transverse momentum. The tracking uses a road algorithm relying on the projectivity of the muon detector. The Level-0 muon trigger analyzes every LHC bunch crossing. It handles about 130 GBytes per second. It finds muon tracks for a bunch crossing in about one microsecond. The architecture is pipeline and massively parallel. The processor is based on high speed optical and copper links, custom backplane as well as on the Stratix GX family of FPGA.

Summary

The Level-0 trigger is an important part of the LHCb trigger reducing the bunch crossing rate from 40 MHz down to 1 MHz in less than four microseconds. It is composed of three sub-triggers: the Level-0 calorimeters trigger, the Level-0 muon trigger and the pileup system.

The muon detector is composed of five tracking stations equipped with 1368 Multi-Wire-Proportional-Chambers and 24 triple-GEM chambers. Each station is divided into four regions, with increasing distance from the beam axis. The chamber topology is complex depending on the station and on the region occupied. In addition, chambers are equipped with pads or strips. The layout of the channel is projective to ease the Level-0 muon trigger processing. The latter receives 25,920 bits every 25 nanoseconds.

The muon detector is divided in four quadrants. Each quadrant is connected to a Level-0 muon processor. These four processors are identical. They are composed of twelve processing boards, a controller board and a custom backplane. A processing board houses four processing elements, a best candidates selection unit and a credit card PC. A processing element analyzes the data coming from a "muon tower" corresponding to 1/48 of a quadrant. It is connected to the five muon stations through eight high speed optical links running at 1.6 Gbps. A processing element is embedded in an FPGA from the Stratix GX family. Processing elements have to exchange a huge number of logical channels to avoid inefficiency on the border of a tower. Copper serial links running at 1.6 Gbps are used between processing elements and on a custom backplane.

All boards are in production now. A processing board, the key element of a processor, is a 9U board with a width of 220 mm. It contains five Stratix GX, about 1500 components and seven pressfit connectors. The printed circuit is made of 18 layers. The minimal size of the track and the minimal distance between two tracks is 120 microns. The total number of links running at 1.6 Gbps is close to 100. The impedance of these tracks is controlled within 10%. High speed serializers and de-seriliazers are those embedded in FPGAs.

Dedicated software tools have been developed to handle the complexity of the data flow. Dedicated tests have been prepared to validate boards during production and to validate a processor in our institute before its installation at CERN.

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Session Classification: Parallel Session B2-Trigger session 2