New RPC Front-End Electronics for HADES

A. Gil [a], D. Belver [b], P. Cabanelas [b], J. Díaz [a], J.A. Garzón [b], D. González-Díaz [b], W. Koenig [c], J.S. Lange [c], J. Marín [d], N. Montes [b], P. Skott [c], M. Traxler [c]

[a] Instituto de Física Corpuscular, centro mixto (UV-CSIC), Valencia, 46071, Spain.
[b] LabCAF, Dpto. de Física de Partículas, Universidade de Santiago de Compostela, Santiago de Compostela, 15782, Spain.
[c] GSI, Gesellschaft für Schwerionenforschung, Darmstadt, 64291, Germany.
[d] CIEMAT, Centro de Investigaciones Energéticas, Medioambientales y Tecnológicas , Madrid, 28040, Spain.

alejandro.gil@ific.uv.es

Abstract

Time-of-flight (TOF) detectors are mainly used for both particle identification and triggering. Resistive Plate Chamber (RPC) detectors are becoming widely used because of their excellent TOF capabilities and reduced cost. The new ESTRELA* RPC wall, which is being installed in the HADES detector at Darmstadt GSI, will contain 1024 RPC modules, covering an active area of around 7 m^2. It has excellent TOF and good charge resolutions. Its Front-End electronics is based on a 8-layer Mother-Board providing impedance matched paths for the output signals of each of the eight 4-channel Daughter-Boards to the TDC.

I. INTRODUCTION

HADES is a High Acceptance DiElectron Spectrometer currently installed at the SIS accelerator of GSI Darmstadt (Germany), which has as main goal the detection of electron pairs produced in relativistic hadron-nucleus and nucleus-nucleus collisions, with high acceptance and invariant-mass resolution, to obtain information about the modification of the properties of vector mesons in nuclear matter, both normal and hot and compressed. HADES consists of several detectors providing triggering, particle identification and momentum reconstruction capabilities. Among these sub-detectors there is a TOF system, built of plastic scintillator rods read by photo-multiplier tubes at large angles and of Resistive Plate Chamber (RPC) detectors at low angles, where the particle rate is low enough. This new low angle ESTRELA detector, which has recently been approved, covers a polar angle between 18º and 45º with 2π azimuthal acceptance, and consists of a RPC wall containing 1024 double-sided readout detectors (2048 channels) distributed in 6 sectors, covering an active area around 7 m^2.

Detector cells have 4 gaps of 0.3 mm width inserted inside aluminium profiles [1]. With this design, the crosstalk between neighbour channels is kept below a negligible level. Plates are made alternatively of aluminium and float-glass their widths ranging between 2.2 cm and 5 cm and the lengths between 12 cm and 52 cm. The HV is applied to the inner aluminium plate and the induced signal is read in all the electrodes. Typical applied voltages with respect to the grounded Al electrode placed in the middle of the cell are of the order of 6kV. As ionizing gas, the 'standard mixture' (85% of Freon, 10% of SF6 and 5% of isobutane) was chosen. The narrow electronic peak of a typical signal has a rise time of about 500 ps and a width of 5 ns.

* Electrically Shielded Timing RPCs Ensemble for Low Angles

II. FRONT-END ELECTRONICS

The Front-End electronics consists of 2 different boards: the 4-channel Daughter-board (DB) and the Mother-board (MB), which serves 8 DB (figure 1). Thus, every MB provides an interface for 32 channels from the DB to the TDC readout-board (TRB). The TRB consists on a custom multi-purpose 128-channel Time-to-Digital Converter electronics based on the HPTDC chip [2] with on-board DAQ functionality, needing 1 channel for timing. Further information about the TRB can be found in [3].

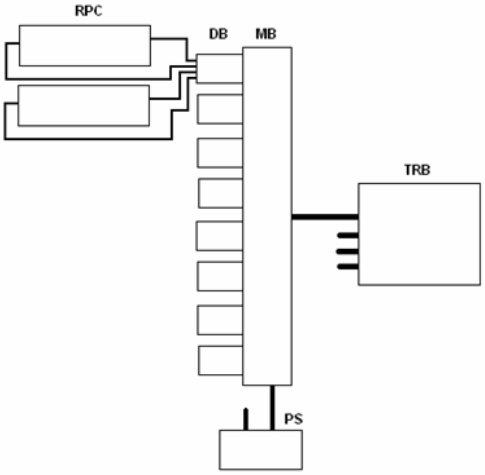

Figure 1: Full chain diagram block.

The DB is the part of the front-end electronics that generates digital signals to be used for TOF and charge measurement. These digital signals are transmitted to the TRB through the MB, which also provides stable supply voltage and thresholds to the DB.

Main requirements of the Front-End electronics for the HADES RPC wall are the following:

- Large bandwidth to deal with very narrow RPC pulses (500 ps rise time).

- Low noise levels (crosstalk < 1%).
- Precise time (electronic jitter < 50 ps) and charge measurements. The overall time resolution (RPC+FEE) should be less than 100 ps, to obtain time resolutions better than 75 ps after slewing correction.
- Low Voltage Differential Signal (LVDS) output signals.
- Output signal for the trigger logic of HADES.
- Stability, reliability, and compact design (max. 4.5 *x* 5 cm for 4 channels).
- Moderate power consumption (about 0.5 W per channel), to reduce heating.

The small space available for the front-end electronics on the detector makes size an important restriction for the DB. Since the DB has been built with discrete, commercially available components, an important requirement for the design of the electronics is the use of the minimum quantity of components, forcing the schematics to be as simple as possible. Other important requirement is the need of low power consumption, to minimize heating.

There are also restrictions in size for the MB, limiting its width to 6 cm to avoid the interaction of the board with the active area of the detector. The MB is a 8-layer PCB, and has a size of 40 *x* 6 cm^2. DB and MB are connected geometrically forming an angle of 90º. Thus, the end of the FEE on the front-side and the back-side of the RPC gas-box will form a channel for air cooling.

III. THE DAUGHTERBOARD

The 6-layer DB provides a digital LVDS output signal containing accurate time and charge information in a compact design, which employs a reduced number of commercially available and inexpensive components.

TOF measurement is performed through a fast discriminator, while the charge measurement is obtained by the Time Over Threshold method (TOT), which gives the charge information as the width of the output pulse.

Since the RPC output signal has frequency components extending up to the GHz range, the preamplifier used in the DB features a 2 GHz bandwidth, with 18 dB power gain and 2.8 dB noise figure. After the amplification, the signal is processed in two parallel ways (figure 2): on one hand, a leading edge discriminator implemented with a fast PECL comparator produces the rising edge of the output signal for time measurement. On the other hand, an integrator, based on a OPA690 voltage operational amplifier, shapes the signal used to measure the charge information. A second leading edge comparator, acting over the shaped signal, determines the width of the output signal, thus encoding information about the charge. In the actual scheme, when the TOF comparator is activated, the output gets locked through the latch enable input. The unlocking of the output is produced by the activation of the TOT comparator. A minimum dead time of 20 ns between the activation of both comparators avoids hang-ups in the digital signal. Further information about the DB can be found in [4].

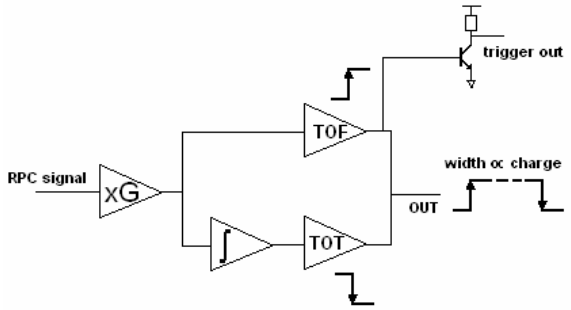

Figure 2: DB diagram block.

In practice, both discriminators are implemented on the MB by the MAX9601 chip, which integrates 2 PECL comparators with latch and 500 ps delay in the same chip. Before transmission to the Motherboard, the output signal is converted into LVDS by the differential translator/repeater SN65LVDS100.

IV. THE MOTHERBOARD

The Motherboard interfaces the very front-end electronics (DB) with the data acquisition system (TRB). Main tasks concerning the MB are to provide:

- Stable and programmable threshold voltages (for TOF and TOT) via DAC.
- Interface for DAC control.
- PCB paths for the readout of all the detector signals.
- Test input signals paths.
- Stable and low ripple power supply voltage and ground.
- Output for low level trigger purposes.

Threshold voltages have been implemented by the LTC2620 DAC. This DAC features 12 bit resolution, low power consumption and very low output noise. To minimize the influence of the noise picked-up along the signal path, every DAC output signal is scaled down through a resistor divider on the DB side, thus, reducing the noise levels by the same factor. The 8 DAC installed in every MB are daisy-chained (figure 3), and can be programmed using the same control lines by Serial Peripheral Interface (SPI).

For signal delivery from/to the MB, the LVDS Standard has been considered as the optimal standard transmission choice [5]. This interface allows communicating data using a very low voltage swing, requiring very low power consumption. This differential signalling technology allows data transmission at hundreds of Megabits per second (Mbps), fitting the requirements of the application.

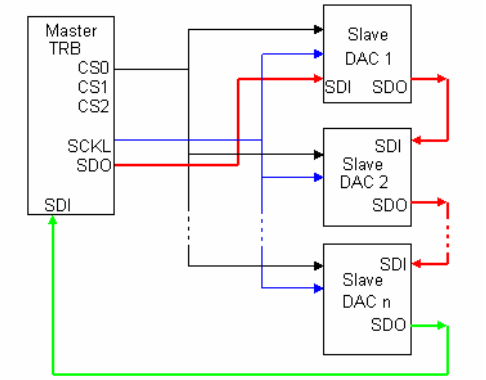

Figure 3: Daisy-chain implementation of the DACs on the Motherboard.

The LVDS interface is used to transmit the control and programming data to the DAC, which are converted to TTL on the MB through a translator. The same differential interface standard is used for the signals coming out from the DB which provide information about the TOF and charge. The main advantage of the differential approach is that noise is coupled to the two wires in common mode (the noise appears on both lines equally) and is thus rejected by the receivers which look at only the difference between the two signals. The differential signals also tend to radiate less noise than single-ended signals due to the cancellation of magnetic fields. In addition, the current mode driver is not prone to switching spikes, and as differential transmission is practically immune to power supply fluctuations there is a further reduction of noise [6]. This is especially important, because switching power supplies are expected to be used to feed the whole system.

Signal paths on MB are completely impedance matched to 100 Ω, terminated on receptor side, to reduce reflections and distortions. Strip-lines (matched traces in the inner layers) between ground and power planes have been implemented [7] instead of micro-strips to increase noise immunity levels. For strip-line, the impedance Z_{DIFF} is given by [8]:

$$Z_{DIFF} = 2 \cdot Z_o \cdot (1 - 0.374 \exp(-0.29 \frac{S}{h}))\Omega \qquad (1)$$

With

$$Z_o = \frac{60}{\sqrt{\varepsilon_r}} \cdot \ln\left(\frac{4h}{0.67\pi(0.8W + t)}\right)\Omega \qquad (2)$$

Where S denotes the distance between traces, h denotes the thickness of the board, W denotes the trace width, t denotes the trace thickness, and ε_r is the dielectric constant of the medium.

The DB is connected to the MB through a SAMTEC QSS connector with 16 differential pin pairs of 0.635 mm pitch. The connector is specified for a crosstalk less than 3.6 % and an impedance matching of 100 Ω, with a mismatch less than 10 % up to frequencies of 2 GHz.

As mentioned before, the MB provides appropriate paths to deliver test signals from the TRB to the DB. The DB provides additional test inputs separated from the RPC signal inputs. The goal of the test signals is only to check if a certain channel is working properly. The use of test signals for calibration is not foreseen. For the reasons already exposed, the test signals are also transmitted as LVDS signals. On the DB, test signals pass through a passive RC derivator circuit placed behind a TTL receiver with the purpose of converting them into narrow pulses, similar to RPC signals. Thus, an external test pulse generates a narrow RPC-like test signal of a few nanoseconds width. Test signals are generated on the TRB, where a LVDS driver delivers the signals through a flat-ribbon cable to a connector placed in the centre of the MB. A 4-port LVDS receiver on the MB allows distributing the test signal to the desired output through a dip-switch. The end of every signal path is terminated with a 100 Ω resistor.

The MB supplies three voltages to the DB; +5V, +3.3V and -5 V, managing a current of 80 mA, 40 mA and 35 mA respectively per channel (including MB consumption). Since the MB is feed by a switching power supply, special care was taken in the design of a power ripple filtering scheme.

Switching power supply output produces a relatively low-frequency ripple at the switching regulator clock frequency (typically 100 kHz to 3 MHz) and high-frequency "spikes" associated with power-switch transition times. The switching regulator pulsed energy delivery creates the ripple. Tantalum high capacitance low ESR capacitors were placed at the power input on the MB. These bulk capacitors smooth but do not eliminate the ac content. For this reason, a local ferrite filter in a π configuration was implemented for every DB and each supply voltage. This filter contains very low ESR multilayer ceramic capacitors (MLCC), of different decades (from 1nF to 1μF), together with special 100 nF feed-through filter capacitors placed before and after the ferrite bead. The ferrite used is the BLM18PG121, from Murata, which has very low DC impedance (only 0.05 Ω). Its impedance-frequency characteristic is shown in figure 4.

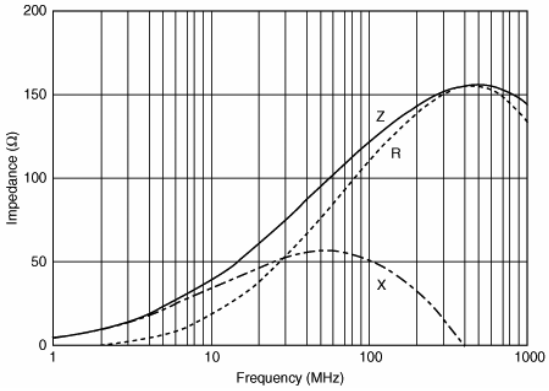

Figure 4: Impedance-frequency characteristics of BLM18PG121 ferrite, from Murata.

The technique of plugged vias was used to achieve short paths from filter capacitors to ground and power, thus reducing the ESL and ESR associated to the layout.

The trigger system (figure 5) provides information about the number of channels fired for a given event. In the MB, the output information of every DB channel is collected and processed to provide an output that is used for low level trigger purposes. This is implemented by a 2-stage circuit with operational amplifiers. Four summing-difference amplifiers and a summing amplifier work in cascade to produce a contribution of -100 mV per fired channel at the output of the trigger. As the number of channels that generate this trigger signal is 32, the output voltage with all channels fired is -3.2V, which is the dynamical range required by the TRB. If there is no channel fired, the output vanishes. The operational amplifier used is the OPA690, mainly because of its high slew rate (1800 V/μs) and high output swing (±4 V).

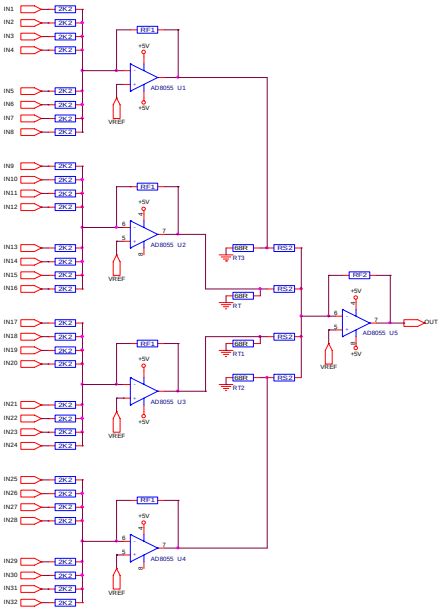

Figure 5: Schematics of the multiplicity trigger signal on the MB.

For simplicity and to reduce the number of pins needed to connect the DB to the MB, multiplicity signals (4 per DB) are transmitted from DB to MB without being converted to LVDS.

V. RESULTS

The Front-End Electronics was tested by pulse generator signals [4], a ^{60}Co radioactive source and a 1 GeV ^{12}C beam delivered by the GSI SIS accelerator.

Measurements performed on the present version of the Front-End Electronics with electronic pulses sources show about 15 ps TOF resolutions (for pulses above 100 fC). Studies of data with several channels firing simultaneously show a cross-talk level below 1% for a threshold of 25 fC, and a worsening of the time resolution of at most 10 ps.

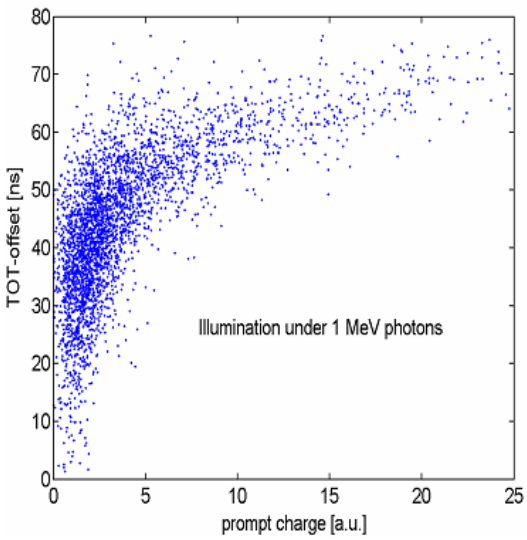

Figure 6: TOT vs charge characteristic for illumination under ^{60}Co photons.

Figure 6 shows the correlation between TOT and prompt charge under gamma illumination, using a ^{60}Co source. The TOT has an offset due to the dead time of the discriminator which was subtracted. Saturation effects are visible in the streamer region. The correlation observed proved to be reasonably good for performing the RPC slewing correction over the time of flight measured. Measurements performed under gamma illumination give an estimation of the TOF resolution of σ=40±5 ps when base-line fluctuations due to cross-talk are included.

Recent data for cosmic rays and secondary particles from 1 GeV C-C collisions show efficiencies of 98-99% (for cosmic rays) [9], and time resolutions around 70 ps (including the detector response) for C-C collisions, as shown in figures 8 and 9.

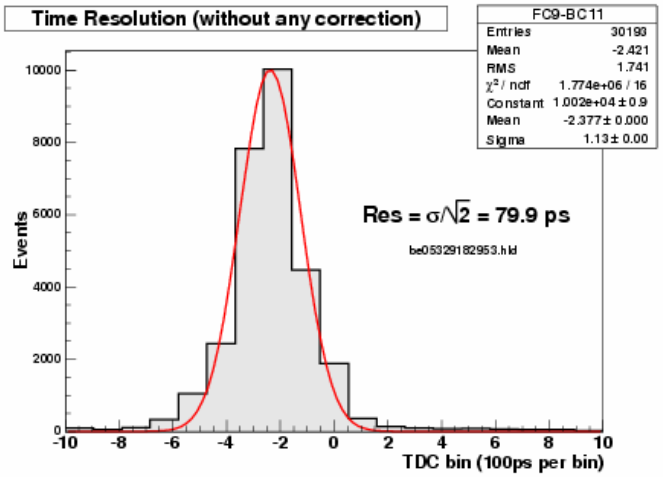

Figure 7: Time resolution for the present Front-End electronics without any correction under 1GeV C-C collisions.

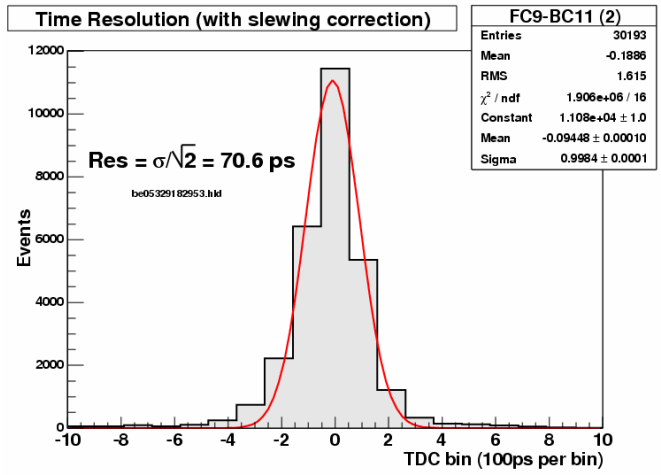

Figure 8: Time resolution for the actual Front-End electronics with slewing correction under 1GeV C-C collisions.

VI. FUTURE WORK

Despite of the good results obtained with the actual version of the FEE, some important improvements are being performed on both, MB and DB boards.

The upgrade of the DB will simplify the charge measurement scheme by using only one of the two comparators. Thus, there will be a double integration with sliding reference threshold, being the integrated signal itself and not the charge comparator the one determining the trailing edge of the output signal (which provides the charge information). This change will improve the resolution of charge measurement and will reduce the power consumption per channel around 30%, which in the actual version is nearly 0.5 W (including MB consumption).

Concerning the MB, the ripple filtering scheme of the power supply voltage will be improved, to increase the power supply rejection ratio, reducing the influence of the switching power supply that feeds the MB. Low drop-out voltage regulators will be included to reduce ripple. A read-back capability will be added to the DAC to check that they are programmed correctly. The manual switch for the test signals will be removed, and a temperature sensing will be added.

VII. CONCLUSIONS

Dealing with the very short rise time RPC signals requires the use of very high speed components and high frequency rules in the PCB design. Differential impedance matched paths with termination resistors were implemented for the transmission of LVDSwhich was considered the optimal interface for the transmission of the digitalized signals.

Special care was taken in noise reduction techniques, thus, multi-layer PCBs with power and ground planes together with many filter capacitors were used in the design of both, DB and MB. For this reason, a local ferrite filter in a π configuration was implemented for every DB and each supply voltage.

Results reveal that the Front-End electronics for the ESTRELA RPC wall of HADES provides very good performances under electronic pulses and gamma ray sources. Tests with ^{12}C beam performed feature an overall time resolution that satisfies the requirements of the project.

VIII. ACKNOWLEDGMENTS

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