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for LHC and future experiments
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Optical Pattern Generator
for Level 0 Trigger Decision Unit of the LHCb experiments
- *The GPL board* -

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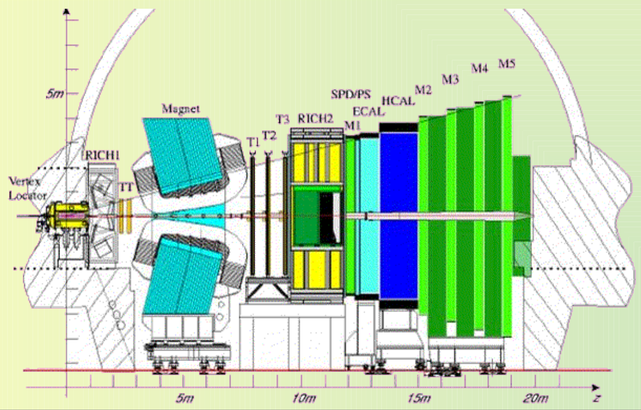
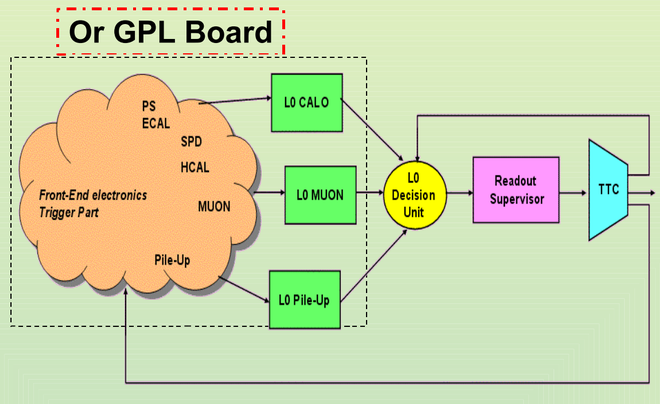
PRESENTATION





LHCb L0 Trigger
- First data processing level (hardware)
- Reduces the data flow to 1MHz
- Fully synchronous pipeline architecture

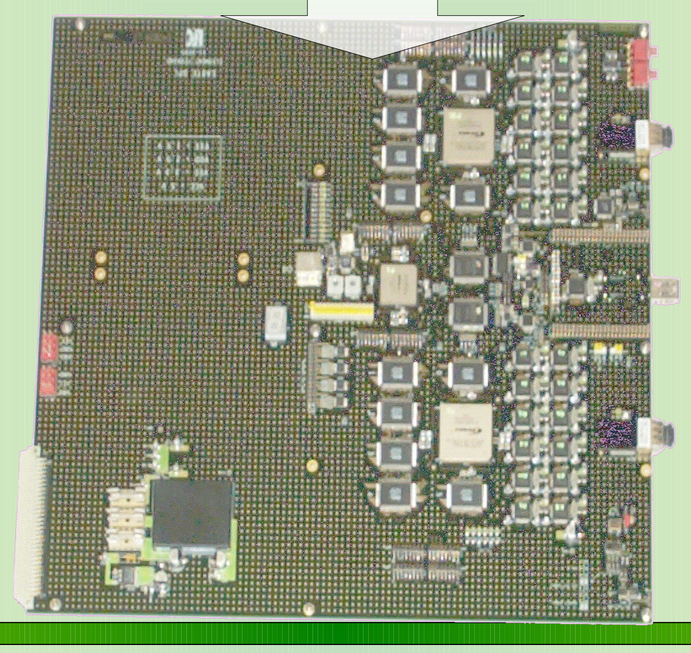
Level 0 Decision Unit (L0DU)
- Receives an event summary for every collision: 764 bits@40 MHz (30 Gb/s)
- Time alignment of the incoming data
- Computes a decision every 25 ns

A specific test bench is needed: *The GPL board*

BOARD PROPERTIES

GPL Test bench for L0DU
- Generates L0DU pattern up to 18 LHC cycles
- Simulates L0 sub-trigger outputs : CALO, MUON and PileUp systems
- Simulates specific event : experimental problems, erroneous data, transmission errors…
- Compares result of L0DU algorithms and data outputs of L0DU

Characterize the links:
Allows to characterize optical links
with L0DU
in stand alone
Allows to test the copper link
32 bits LVDS 40MHz



Board Properties
- PCB : 16 layers
High frequency signals / High wire density
Board Size : VME 9U

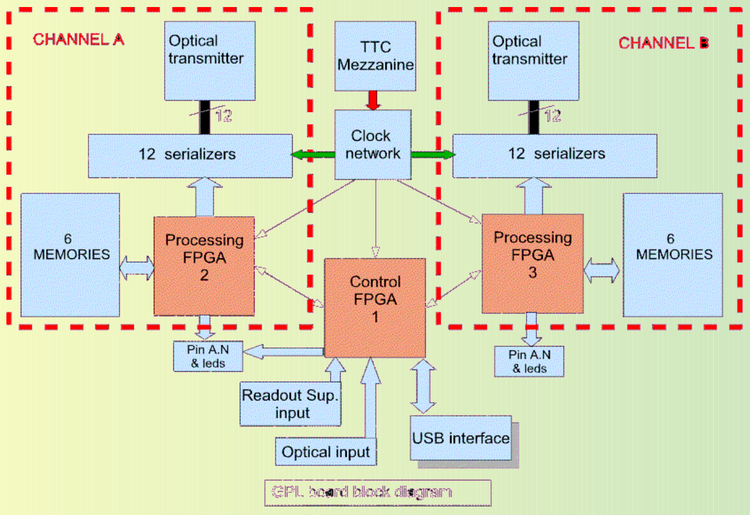
Outputs
24 independent optical outputs at 1.6 Gb/s

Inputs
1 optical input
1 copper input: 32 bits LVDS @ 40MHz from L0DU

TTC mezzanine

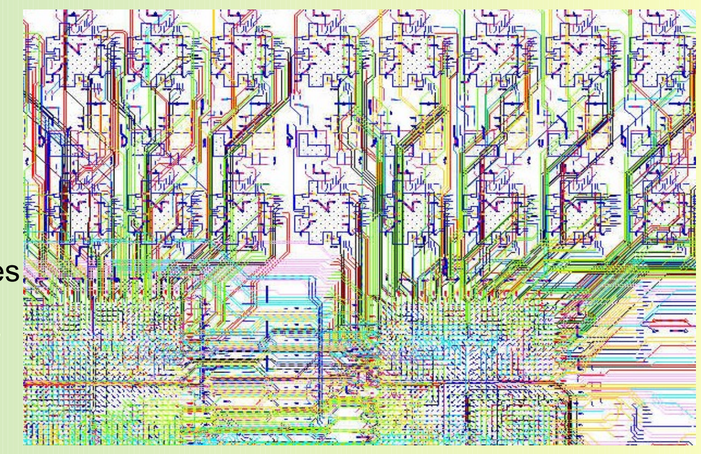
2 Clock networks: one for delay phases alignment

BOARD DESIGN



Board control
- interface from L0DU
- USB from a PC (debug mode)
- JTAG for FPGA programming

Data flow
- 2 processing FPGA
- 128k pattern storage in 12 external RAM, 18 LHC cycles
- 24 serializers TLK2501
24 *18bits @80MHz copper → 24 x 1,6 Gb/s copper
- 2 optical transceivers HFBR772
24x1.6Gb/s copper→ 24 x1.6Gb/s optical



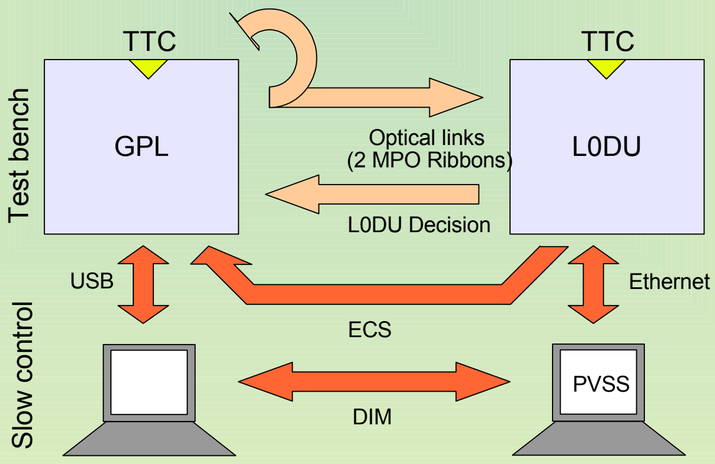
High wires density and high frequency signal

TEST MODES

On each 16 bits input
(Optical input and L0DU decision)
- Stores the incoming data in a RAM (32k)
- Compares the incoming counter with a local one
16-bit error counter / 48-bit word counter

Start signal for sending data or data acquisition
- Software / Push button
- Bunch Count Reset (Synchronisation with L0DU)

Software
- Easy to use PVSS interface
- Fully integrated with the L0DU software
- Configures the board
- Loads the RAM
- Reads the test results



GPL output pattern type:
- An identification word
- A counter
- The RAM content (128k / output)

- Adds special characters between each cycle to synchronize the links (TLK specification)
- Adds latency between each outputs
- Changes the clock phases between the 2 channels