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Optical pattern generator board

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The GPL board is an optical pattern generator for the L0 Decision Unit (L0DU). Its design is based on three FPGAs in BGA package which can send 24*16bits @ 80 MHz via 24 optical fiber link running at 1.6 Gb/s. One FPGA is used for the control of the board, via USB or through L0DU, and two processing FPGAs are used to control the optical channel. Each processing FPGA controls twelve deserializers which send the data to an optical transceiver. The GPL board is a 16 layer custom board.

Summary

The GPL board is an optical pattern generator used for the external test bench of the Level0 Decision Unit. Its design is based on three FPGAs in BGA package which can send 24*16 bits @ 80 MHz via 24 optical fiber link running at 1.6 Gb/s.
One FPGA is used for the control of the board and two processing FPGAs are used to control the optical channel. Each processing FPGA controls twelve deserializers which send the data to an optical transceiver. For stand alone test purpose, an additional single optical channel transceiver is implemented. The GPL board is synchronized by the Timing and Trigger Control which delivers, through the TTC mezzanine and the QPLL, the clock reference with low jitter required by the deserializers. A 32 bit LVDS input is implemented in order to receive the Readout Supervisor word from the L0DU. The acquired data is saved and compared to the expected results to elaborate the diagnostic of test. The GPL board allows to emulate the full L0DU environment at laboratory and will be the same rack of the L0DU for the commissioning test.
Two tests mode are foreseen. The first one consists in sending a 16 bits counter one every optical fiber link in order to qualify the bit error rate of each optical fiber link. The second test, the content of FPGA's internal memory or external memory is sent to the L0DU to check the behaviour of the L0DU. This mode allows testing the L0DU algorithms with realistic data generated from a sample of simulated physics events, and check the behaviour of the L0DU when erroneous data or optical transfer errors are introduced in the data flow.
To control the board, two interfaces are provided. The first one is an USB interface based on a commercial device, which allows to connect the board directly to a PC to configure the board. The second one is done through the L0DU and the CC-PC of the TELL1 board. In this configuration, the GPL board is seen as a part of the L0DU and can be controlled and configured by the Experimental Control System (ECS).
The same software interface is used to configure both boards. It allows to easily set up the internal register and the pattern RAM with graphical panels and to analyse the test results. The L0DU environment in the LHCb experiment could be emulated by the GPL board which is a 16 layer custom board.
It is the central part of the external test bench of the L0DU. It allows to qualify the bit error rate of each optical fiber link on the receiver side and to emulate the L0DU input informations which are sent by the L0 sub-triggers.

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