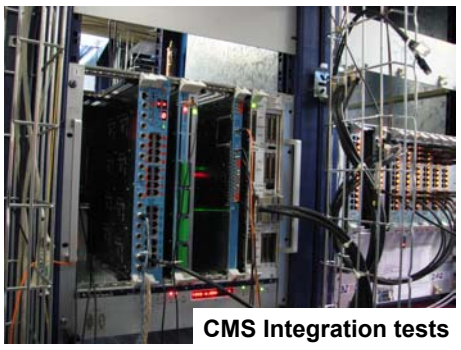
The Level-1 Global Trigger for the CMS Experiment at LHC

M.Jeitler, A. Taurok

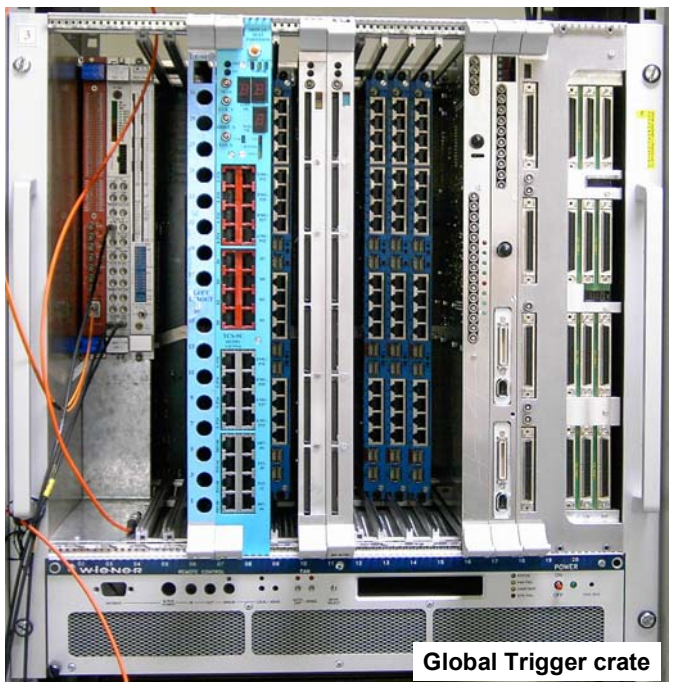
H. Bergauer, C. Deldicque, J.Erö, M. Ghete, P. Glaser, K. Kastner, I. Mikulec, T. Nöbauer, B. Neuherz, M. Padrta, H. Rohringer, T. Schreiner, J. Strauss, C.-E. Wulz

Institut für Hochenergiephysik der Österreichischen Akademie der Wissenschaften,

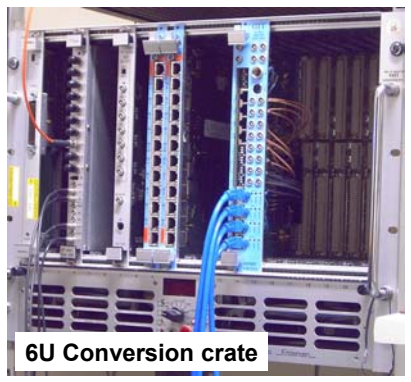
Nikolsdorfergasse 18, A-1050 Vienna , Austria



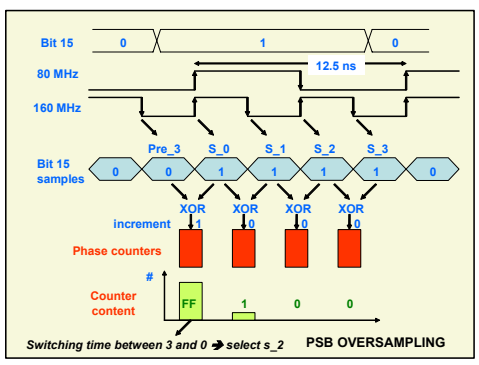
CMS Integration tests



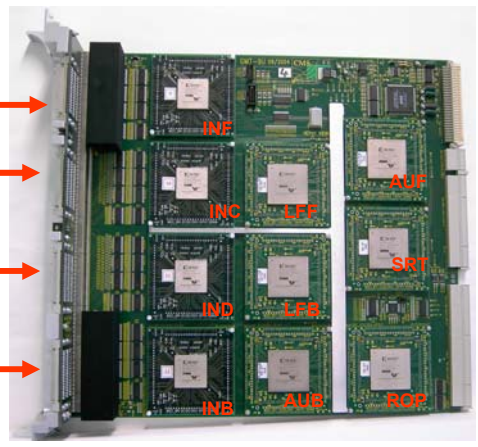
Global Trigger crate



6U Conversion crate



Muons:
4 fRPC
4 CSC
4 DT
4 bRPC



LVDS

3 PSB

MIP, Q bits

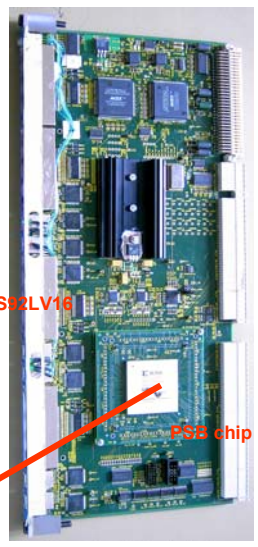
4 Muons

GTL+

TOTEM Trigger

Global Calorimeter Trigger

LVDS seriell

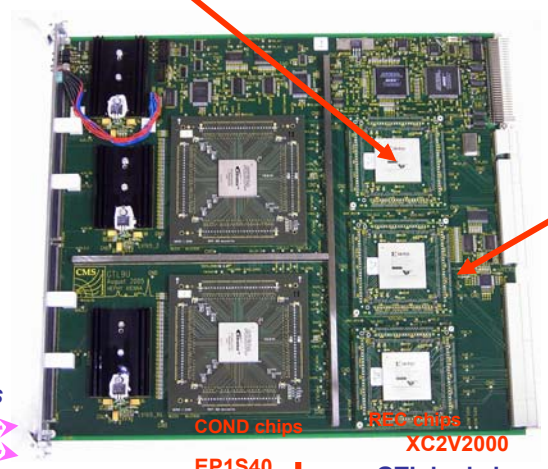


3 PSB input & synchronization boards

- 8 Serial Receivers
  - DS92LV16: 1.2 Gbps ➔ 80MHz/16bits
- LVDS Receiver: 64 bits / 40 MHz
- PHASE synchronization:
  - ➔ oversampling of input signals
- BC-synchronization:
  - ➔ delay circuits for trigger data
- Synchronization to LHC orbit:
  - ➔ SIM/SPY memories for each channel
- DAQ:
  - ➔ Ringbuffer + FIFO + ROP(state machine)

Global Muon Trigger GMT

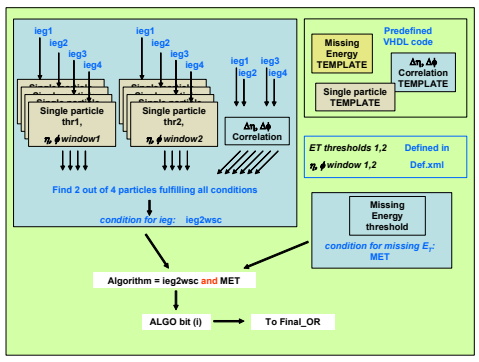
IN chips: LVDS Receiver: 512 bits / 40 MHz
PHASE + BC synchronization
Spy mem, Ringbuffers + FIFOs
LFF/LFB: find matching muons, cancel out logic
order by rank, 1st-sorter stage
AUF/AUB: assign MIP+ISO bits
SRT: Final Sorter, Ringbuffers + FIFOs
ROP: VME decoding, Readout processor



GTL+

Calorimeter objects:
4e/g, 4ie/g, 4cjet, 4fjet, 4tau
E_T, E_T_miss, jet#

Algorithm Logic (example)

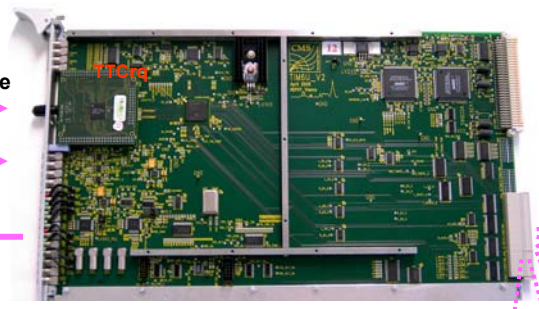


TTC: L1A,.....

fibre

CLK, orbit (ECL)

clk



LVDS

TIM broadcasts Clock, BCRes, L1A signals

- TTCrq module: clk, bcres, l1a, bgo-cmds
- ECL signals: clk, orbit, l1a
- Internal BCRes generation
- BC-table: generates L1A, Bgo-cmds for tests
- programmable delays for each board
- common BCRes delay

128 Algo bits

GTL logic board

- 3 Receiver chips
  - SIM/SPY memories
- 2 Condition chips EP1S40
  - Algorithm Logic for 128 Algo-bits
  - SIM/SPY memory

FDL makes FinOR signals

- 128 Algorithms + 64 Technical Triggers
- Rate Counters
- Prescalers
- Masks, Veto-mask for TechTrig's
- DAQ: Ringbuffer + FIFO + ROP
- SIM/SPY memories

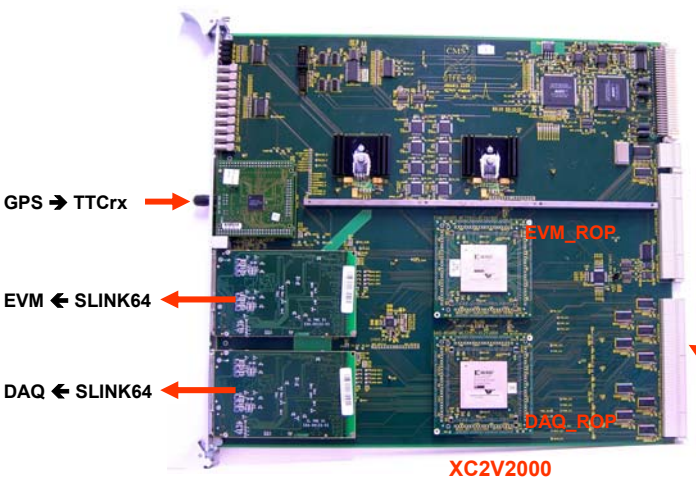
GTL+

64 TTRIG bits

64 Technical Triggers

LVDS

PSB for Technical Triggers



Event records via *Channel Links*

GTFE readout ➔ DAQ, Event Manager

- Event records via Channel Links from GMT, PSBs, FDL, TCS
- TTCrq receives GPS time
- SLINK64 ➔ DAQ
- SLINK64 ➔ Event Manager
- Record Formatting:
  - Special FIFO: 16 bits in ➔ 64 bits out, sync. reset
  - Crate_ROP: state machine
- SIM/SPY memory

8 Fin_OR

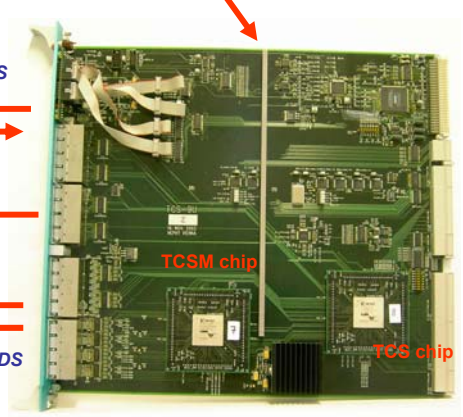
LVDS

4 Tracker Emulators

LVDS

8 DAQ aTTS

LVDS



32 TTCci

TCS Central Trigger Control

- 8 FinOR ➔ 8 L1A
- 8 Partition Controller ➔ 8 DAQ Partitions
- Throttle Logic
- STATUS Signals from FMM
- IO ➔ Tracker Emulator
- Counters: deadtime.....