Beam Phase and Intensity Monitor (BPIM) for the LHCb Experiment

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Abstract

The LHC bunch clock is transmitted over kilometres of fibre to the experiments where it is distributed to thousands of front-end electronics boards. In order to ensure that the detector signals are sampled properly, its long-term stability with respect to the bunch arrival times must be monitored with a precision of <100ps. In addition it is important to monitor the trigger conditions by measuring the intensity of each bunch locally in the experiment.

For this purpose a beam phase and intensity acquisition board (BPIM) has been developed for the Button Electrode Beam Pick-ups which will be installed on both sides of the LHCb interaction point. The board measures the two quantities per bunch, and processes the information in an onboard FPGA. The information is read-out by the Experiment Control System and is directly fed to the LHCb Timing and Fast Control (TFC) [1]. In the TFC system the information is included in an event data bank but may also be used as a bunch crossing trigger or gate.

I. Introduction

The LHC bunch frequency of 40 MHz is transmitted to the experiments via a network of optical fibres which is mostly based on non-phase-stabilized fibres located at a depth of about a metre. In the case of the LHCb experiment the total distance is about 14km. In LHCb the bunch clock is locally distributed by the Timing and Fast Control (TFC) system to all the detector front-end electronics where it is used to sample the detector signals which typically have plateaus of the order of a nanosecond. Thus it is of extreme importance that the phase of the LHC clock remains stable with respect to the bunch arrival times. However, several effects such as temperature variations influence the phase. Measurements show that the time drift on the transmission fibres could be as large as 200ps over a period of 24 hours, and up to 8ns have been observed over a period of a year (Figure 1[2]). Clearly the phase must be monitored and regular timing alignments must be performed. The TFC system provides several means of making a complete timing alignment at the level of 50ps.

In order to monitor the bunch arrival times with respect to the bunch clock a Button Electrode beam pickup (BPTX) [3] has been installed 146m away from the LHCb interaction point on each side for exclusive use by LHCb. In order to be largely independent of the position of the beam, the pulses of the four buttons of each pick-up is summed. As a result the current of the individual bunches may also be measured. This is of high interest since it allows monitoring the LHC bunch structure to detect possible ghost or displaced bunches, and will be of great help in the coarse timing alignment of the experiment. This also is of particular interest in LHCb since the interaction point is off the nominal interaction point by 7.5m and will therefore have single bunch crossings also.

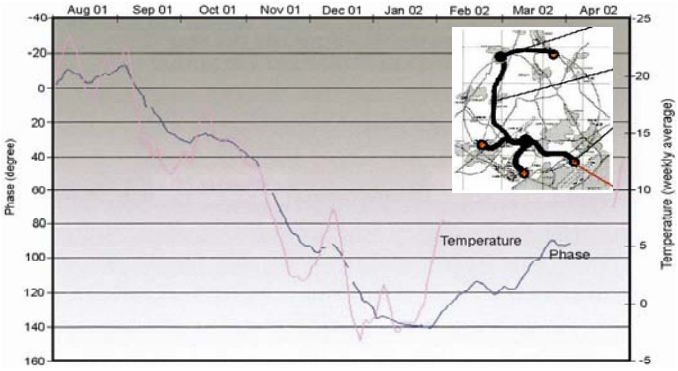

Figure 1: Effect of temperature variations on the clock distribution fibres [2].

The individual intensity measurement also allows checking the bunch intensities against the actual physics triggers and therefore allows verifying that the trigger and the detector front-ends are correctly synchronized. Directly interfaced to the Timing and Fast Control system of LHCb the information may also be used to produce a bunch crossing trigger or a gate for special running modes.

II. Beam Pick-Up and Signal Transmission

Out of the 1158 beam pick-ups of the Button Electrode type around the LHC, two have been installed per experiment for local beam monitoring (Figure 2). The pulses from the four buttons are summed giving the total amplitudes presented in Table 1 for three different beam scenarios. The pulses are bipolar with a typical length of 2ns (Figure 3 and 4).

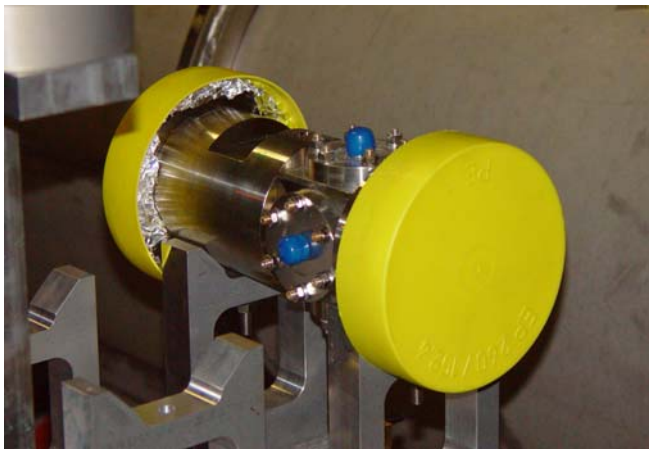

Figure 2: Picture of one of the two Button Electrode beam pick-ups at LHCb

Table 1: Expected total signal levels in three different beam scenarios at injection (450 GeV) and in physics mode (7 TeV).

Beam intensity (ppb)	BPTX [V]		200 m CMA50 [V]	
	450 GeV	7 TeV	450 GeV	7 TeV
Pilot ($5*10^9$)	-1.3 / 2.2	-1.7 / 3.7	-0.6 / 1.2	-1.2 / 2.4
Year 1($4*10^{10}$)	10 / 18	-14 / 30	-4.4 / 9.6	-10 / 19
Nom($1.15*10^{11}$)	-29 / 51	-39 / 85	-12 / 28	-30 / 55

The pick-up signals from the two BPTXs around LHCb (BPTX.5L8.B1 and BPTX.5R8.B2) are transmitted to the counting houses in LHCb by means of a ~200m Nexan ½" CMA50 coaxial cable with a nominal attenuation of 3.3dB/100m at 160 MHz and 5.9dB/100m at 450MHz. Table 1 gives the expected total signal amplitudes before and after the cable for three different beam scenarios. The bunch length is assumed to be σ_{beam} = 375 ps at 450 GeV (injection) and σ_{beam} = 250 ps at 7 TeV (physics beams) and the shape Gaussian.

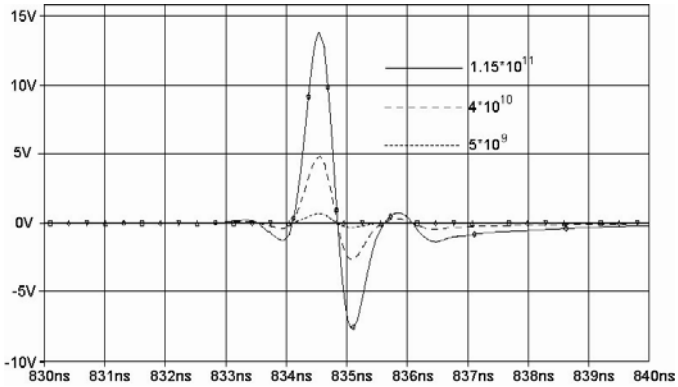

Figure 3: Expected signal for single button after 200m of the transmission cable in the three beam scenarios at 7 TeV.

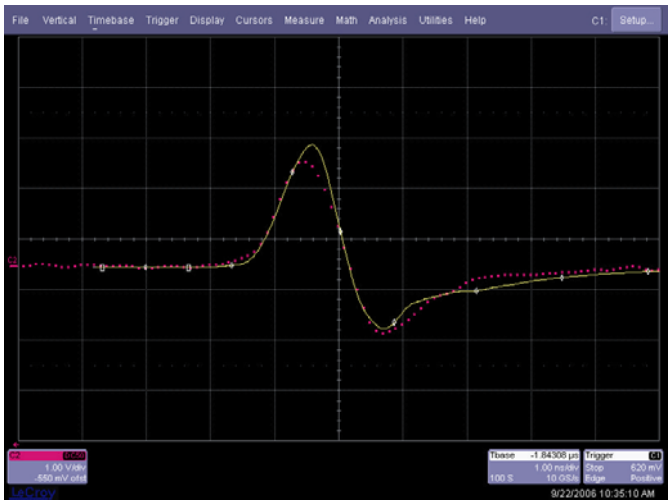

Figure 4: Pspice simulation of the signal pulse from a single Button Electrode including cable compared to a real pulse from a provisory pick-up at the CERN-SPS.

III. Acquisition Board

The acquisition board consist of a custom-made 6U VME board, currently one board per beam. The block diagram is shown in Figure 5. The analogue unit of the board consists of a separate circuit for the phase measurement and the intensity measurement. The board performs the intensity and the phase measurement continuously at 40 MHz and outputs the intensity information on the front-panel. Accumulation of data for all bunches of a full LHC turn (3564) may be triggered via the controls interface and synchronizes on the following LHC orbit pulse. The information may then be read-out via the control interfaced, processed, and used in the monitoring of the experiment.

Logically the device may be divided into the following blocks:

- clock adjustment and distribution,
- input pulse normalizer and buffer,
- intensity measurement circuitry,
- phase measurement circuitry,
- digital processing and data accumulation,
- I/O interfaces,
- and board control

A. Clock Distribution

The logic of the entire board is solely driven with the LHC bunch clock and the orbit signal. The LHC orbit signal serves as a reference for the accumulation of data for one full LHC turn. The bunch clock is AC-coupled and properly reshaped at the input. Since the analogue signal from the beam pick-up and the bunch clock are tightly coupled in the time domain, the relative phase of the two signals at the inputs has to be carefully adjusted once and for all. In order to start out with a maximum available range for a negative/positive phase shift, the best location for the beam pick-up pulse is in the middle of the clock period.

The clock adjustment is accomplished by means of three cascaded active delay lines (ONSEMI 100EP196). Together they cover the entire clock period and the delay is completely programmable via the control interface.

The delayed clock train is distributed by means of a clock fan-out to all the crucial nodes of the module:

- ADC sampling clock
- TDC reference clock
- TDC start clock (bunch clock divided by eight)
- Main and Auxiliary (VME interface) FPGA base clocks
- Intensity FIFO write clock
- Phase FIFO write clock
- Local Bus clock (bunch clock divided by two)

The distribution is entirely based on differential LVPECL. The discharge circuit of the integrator is driven by the bunch clock as well on a separate output of the fan-out.

B. Analogue Signal Input Stage

Due to the very large range of amplitudes in the different beam scenarios, the intensity measurement circuit contains an attenuator at the input of the pick-up signal with two different attenuations, one for pilot and the first year of beam, and the second for the nominal beam. The attenuator stage is meant to

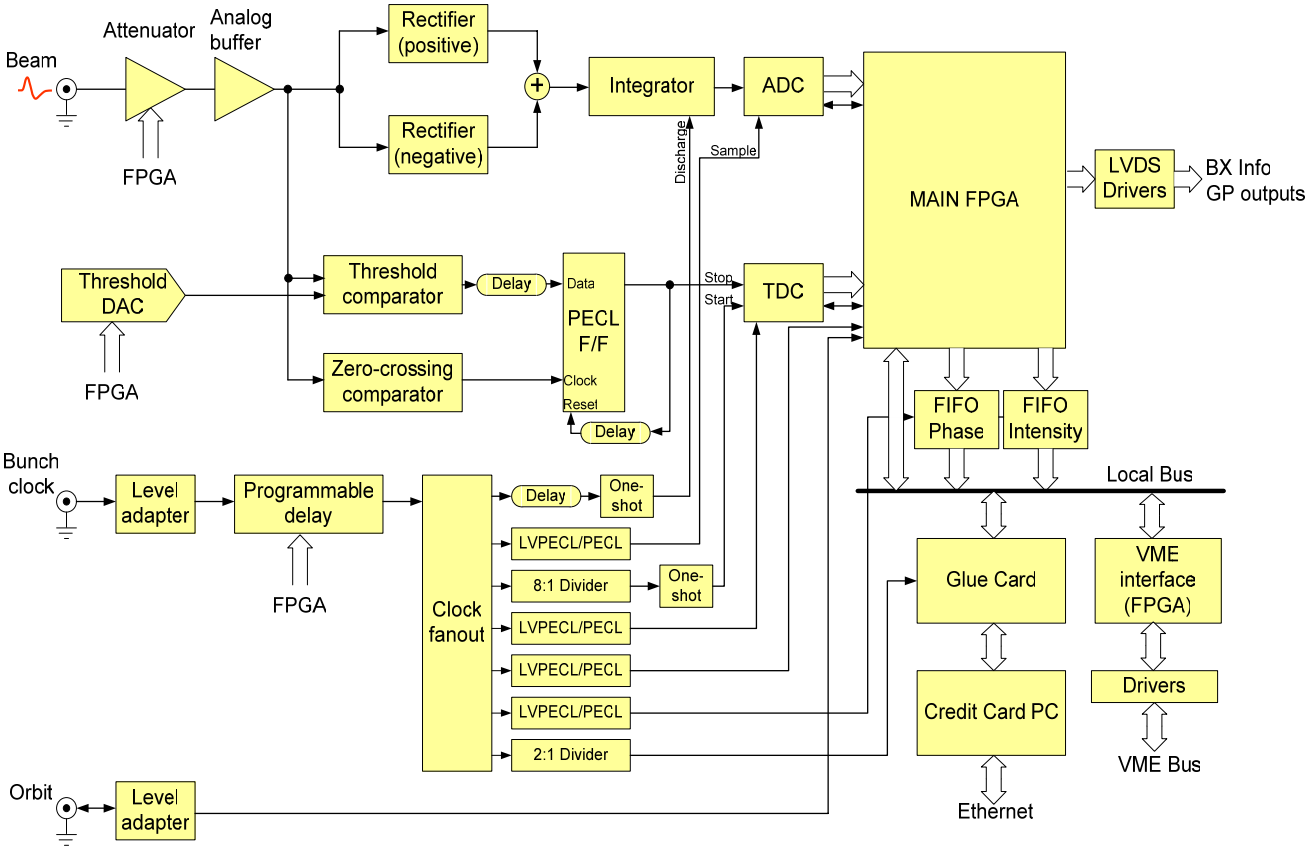

Figure 5: Complete block diagram of the Beam Phase and Intensity Monitor.

normalize the incoming analogue pulse to an amplitude of approximately +5V. The two different ranges of amplitude normalization may be changed by means of changing a resistor if needed. The ranges are switched via the control interface with the help of special RF relay from Omron. The output from the attenuator stage (THS3201 Operation Amplifier) is buffered by an ultra-fast unity gain device (LMH6559).

C. *Intensity Measurement*

In order to measure the intensity of the individual bunch crossings the entire area of incoming bipolar pulse is integrated. Thus the output from the unity gain buffer is passed through a full-wave rectifier. To achieve symmetry, both halves of the pick-up pulse are rectified by identical but individual active circuits, one of which acts on an inverted primary pulse. The outputs signal from the two rectifiers are summed and passed to an active integrator.

The accumulated charge is constantly sampled by a 12-bit A/D Converter (AD9432) preceded by an ADC Driver (AD8138) which makes the data acquisition mode differential. The converter is equipped with an ultra fast on-chip track-and-hold circuit. The amplitude from the integrator is sampled by the ADC on the rising edge of the *Sample* pulse which is a replica of the bunch clock. The ADC pipelines the samples meaning that, on every sample edge, the ADC outputs the data of the sample taken ten clock periods earlier. The output data is immediately read by the FPGA.

Two nanosecond after the rising edge of the bunch clock, the integrator is discharged with a 2.5 ns resetting pulse which closes an RF MOSFET transistor.

A simulation of the intensity measurement circuit is shown in Figure 6.

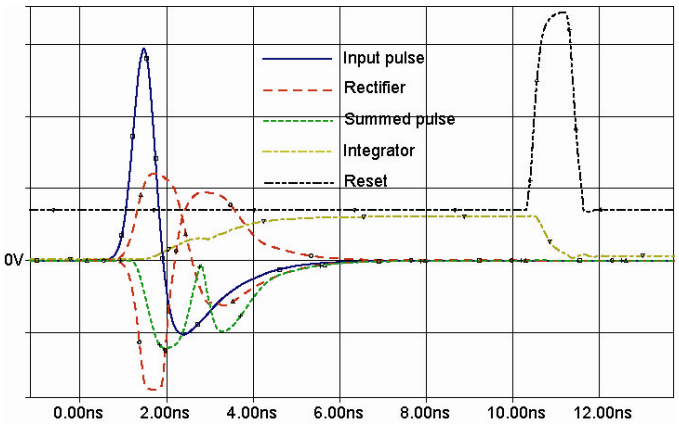

Figure 6: Pspice simulation of the intensity measurement circuit.

D. *Phase Measurement*

The heart of the phase measurement circuitry is an ultra-high performance 8-channel Time-to-Digital Converter from Acam (TDC-GPX). The current design uses the “R” operational mode in which the TDC may operate in a multi-hit mode at 40 MHz with a resolution of 27 ps over a period of 10 µs. The TDC works in a retriggered manner in which the start signal is supplied every eight bunch clocks at its rising edge. The stop pulse is formed by a zero-crossing discrimination of the attenuated analogue pick-up signal. Low amplitude parasitic pulses are eliminated with the help of a programmable threshold provided by a DAC. A simulation of the phase measurement circuit is shown in Figure 7.

Although it is known that the zero-crossing point is not fully suitable for a high precision reference of the bunch passage, this method was chosen for the first version. The zero-crossing point varies slightly with bunch length and shape and may vary up to 100ps between injection and start-of-physics.

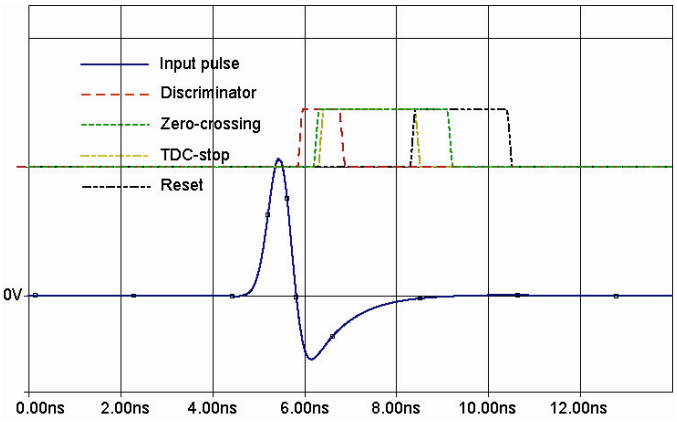

Figure 7: Pspice simulation of the phase measurement circuit.

E. Digital Processing

The digital processing of the board is performed by an FPGA (Altera APEX20K200EQC240-1X). The FPGA reads out the ADC and TDC continuously and performs linearization of the converter characteristics.

The FPGA subsequently outputs the intensity measurements as compressed on either eight or four-bits as LVDS. It may also be programmed with a digital threshold to output a "bunch crossing trigger" or any type of signal needed on the general purpose outputs

Data accumulation of the intensity measurements and phase measurements is triggered via the control interface. The FPGA synchronizes the accumulation to the orbit signal and fills simultaneously the two quantities for each bunch in two FIFOs for 3564 (full LHC turn) consecutive bunch crossings.

The FPGA also provides full control of the attenuator selection, the discriminator threshold, and the programmable clock delays via the Local Bus (see next section).

F. Board Control

In LHCb the electronics boards will all be controlled from the overall Experiment Control System (ECS). In order to access the actual board resources, an ECS interface will be located on each board. The ECS interface is connected to the control network and performs directly all device programming, configuration, control and monitoring of each electronics board. The BPIM is equipped with the same interface as all the electronics in the LHCb counting houses behind the shielding wall. It is based on a commercial Credit Card PC (CCPC) with Ethernet from Digital Logic, AG, Switzerland [4].

All the board resources are accessed via the PCI bus of the CCPC. In order to facilitate interfacing to different types of board control buses, a small intermediate mezzanine card with "Glue logic" has been developed [5]. The glue card is connected to the PCI bus and forms a standard set of simple interfaces needed by all the different electronics boards, such as a parallel 32-bit Local Bus, I^2C, JTAG and an 8-bit General Purpose I/O interface.

The configuration of all the functions implemented in the main FPGA is controlled via the 32-bit Local Bus, including access to the programmable clock delay, the attenuator selection and the discriminator threshold. The data accumulation is also triggered via the Local Bus, and the Phase and Intensity FIFOs are read out via the Local Bus. I^2C is only used to access an onboard memory storing the board identifier.

The main FPGA and its configuration device may be programmed via JTAG directly from the CCPC. The VME interface FPGA is programmed using an onboard JTAG header

Alternatively, a VME interface has been implemented onboard in an auxiliary FPGA to allow the device to be used in a VME-based control environment. It is directly interfaced to the Local Bus of the board. In this environment the configuration device for the main FPGA may only be programmed via an onboard JTAG header.

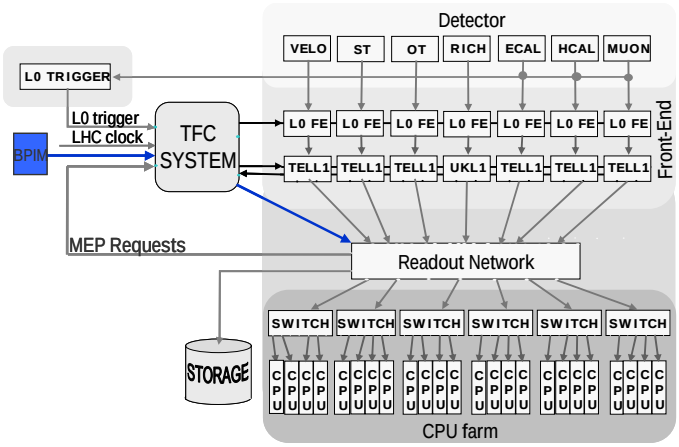

Figure 8: Overview of the LHCb online system with the BPIM interfaced to the LHCb readout supervisor "ODIN" in the TFC system allowing the bunch crossing information to be used in the control of the trigger and to be included in the event data.

IV. Conclusion

The current paper proposes a beam phase and intensity acquisition board (BPIM) for the Button Electrode beam pick-ups installed at each of the LHC interaction points for the experiments. The acquisition board is capable of performing simultaneously measurements of the individual bunch intensities with a 12-bit resolution and the bunch arrival times with respect to the LHC clock with a precision of approximately 100 ps at 40 MHz. In addition to reading out the measurements via the control interface, they are also output on the front-panel of the board at 40 MHz. The latter allows directly interfacing the board to the Timing and Fast Control system of LHCb (Figure 8) in order to add the bunch current information to the data of each event. It also allows the information to be used in the control of the trigger and as a bunch crossing trigger/gate.

V. Acknowledgements

We would like to thank Rhodri Jones and Eva Calvo Giraldo in the CERN-AB/BI group for their help in understanding the Button Electrode beam pick-ups and providing us with a simulation model of the buttons. We would also like to thank Greg Kasprowicz who started this project as a summer student. Last we would like to thank Thilo Pauly for useful discussions and real data from a provisory pick-up on the CERN-SPS.

VI. References

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