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Total Dose and Single Event Effects in a 0.25 μm Silicon-On-Sapphire CMOS Technology

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Silicon-On-Sapphire (SOS) CMOS technology has been attractive to radiation tolerant applications. The Sapphire substrate eliminates single-event latch-up (SEL) and reduces the possibility of single event upset (SEE), but the back-channel leakage current could cause problems to circuitry made in this technology. To better understand the radiation effects in this technology and evaluate its feasibility in applications such as Large Hadron Collider (LHC) experiments, we have developed a custom test chip containing various test structures of MOSFET devices and circuits using Peregrine Semiconductor's 0.25μm SOS CMOS technology. This paper presents the total ionization doze (TID) and SEE measurement result and characterization obtained through the chip.

Summary

Silicon-On-Sapphire (SOS) CMOS technology has been attractive for radiation tolerant electronics. With the insolating sapphire substrate, this technology eliminates the parasitic transistor in the bulk silicon substrate and hence removes the mechanism for latch-ups. This insolating substrate also reduces the possibility of Single event upset (SEU).

SOS technology, like any Silicon-on-insulator technology, does have another source of leakage in the devices, in addition to the edge leakage —back channel leakage at the interface of Sapphire and SiO2. The leakage could cause problems to circuitry since no layout techniques can mitigate this effect. To better understand the radiation effects in this technology and evaluate its feasibility in applications such as Large Hadron Collider (LHC) experiments, we have developed a custom test chip using Peregrine Semiconductor's 0.25μm SOS CMOS technology. We plan to characterize MOSFET devices and circuitry fabricated with respect to TID and SEE.

The test chip contains various configurations of NMOS and PMOS devices, ring-oscillators, resistors, digital standard cells, and D-Flip-flop (DFF) test structures for SEE characterization.

A. Single transistors

The test-chip contains NMOS and PMOS devices with three different channel lengths (W/L=10μm/0.25μm, W/L=10μm/0.5μm, and W/L=10μm/1.0μm). Each transistor is implemented in four different types of layout: standard, edgeless, two-finger and four-finger. Since backchannel leakage is proportional to the channel length, we have designed transistors with different length to characterize the back-channel leakage current. Edge leakage current is proportional to the number of edges in a transistor, therefore the transistors laid out in standard (one-finger), two finger and four-finger transistors can provide us information on the leakage current in transistors without using edgeless layout.

B. Ring oscillator

The test chip contains three different types of ring oscillators to characterize the effect of TID on circuit performance (speed) as well as power dissipation. The ring oscillators include CMOS ring oscillators made of minimum-size inverters, both in standard layout and edgeless layout, and ring oscillator made using current-mode logic.

C. Shift-registers

In order to characterize the single-event effect, we have designed multiple 32-stage shift registers (DFFs) with various setup. The test structures include shift registers with standard-layout, shift-registers with edge less layout, and shift registers with majority-vote circuitry.

In addition, resistively hardened cells have been used extensively to make SRMs rad-hard. In this test chip, we have designed shift-registers with different resistors (1k, 2k, 4k, 8, 16k, 32k, 64k and 128k ohms) connected in the feedback path

of the latch to characterize the SEE of the latch and DFF cells.
D. Digital standard cells
The digital standard cells in the test chip include INVETTER, NAND, and NOR gates in both standard and edgeless layout.
E. Current mirrors
we also put down matched current mirror structures in the test chip to characterize possible leakage current in the current mirrors under different radiation levels.

We are currently working on the test bed development for the 0.25μm SOS CMOS test chip. The results will be presented at the workshop.

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