Development of the input circuit for GOSSIP vertex detector in 0.13 μm CMOS technology.

Vladimir Gromov,
Ruud Kluit, Harry van der Graaf.
NIKHEF, Amsterdam,
The Netherlands.

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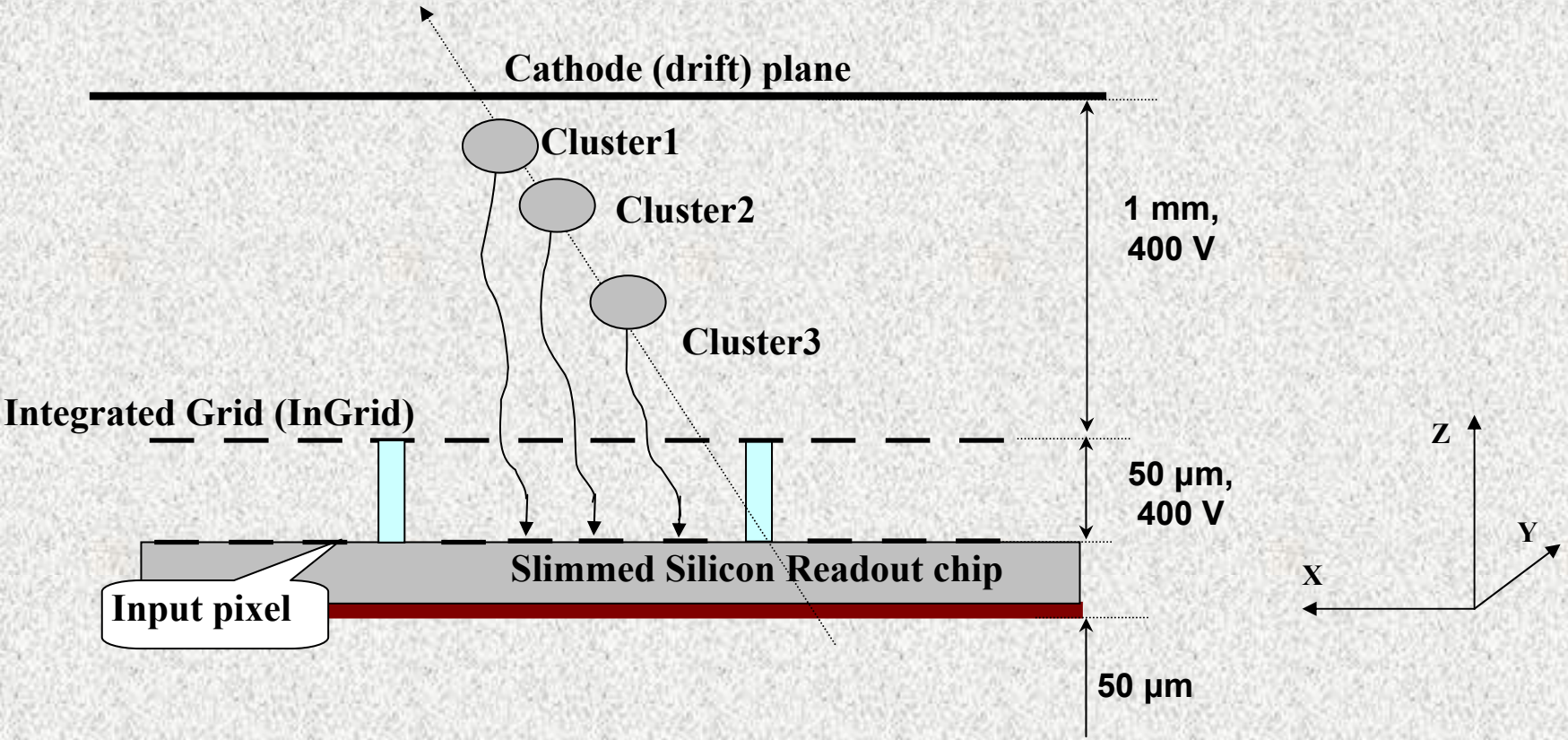
Outline

- GOSSIP detector: principles of operation and features.
- Inputs and requirements for the design of the input circuit.
- The prototype of the input circuit.
- Conclusions and plans.

GOSSIP detector: principles of operation.

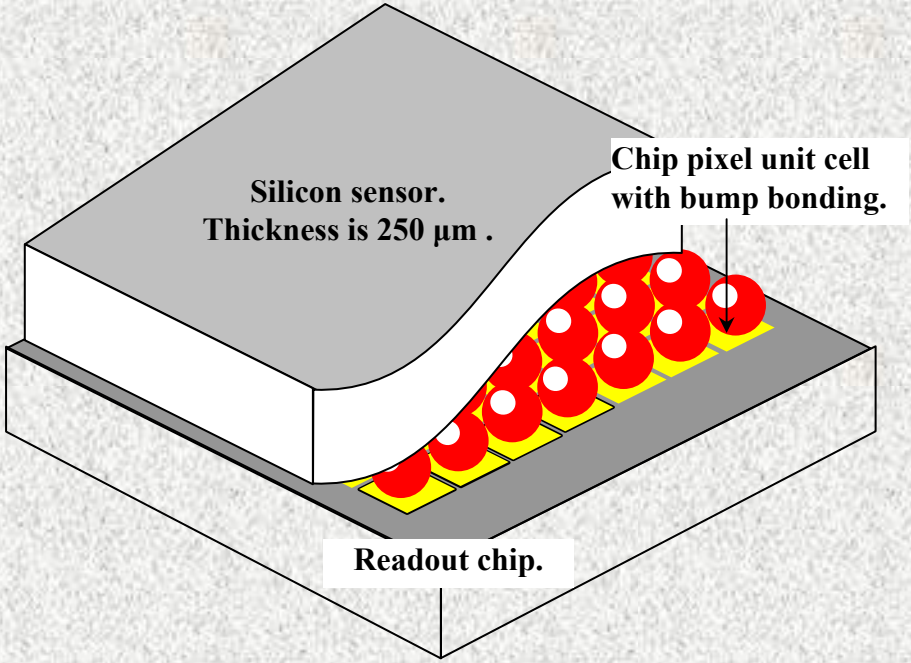
Gas On Slimmed Silicon Pixel (GOSSIP) is a vertex detector combining a thin gas layer as signal generator with a CMOS readout pixel array.



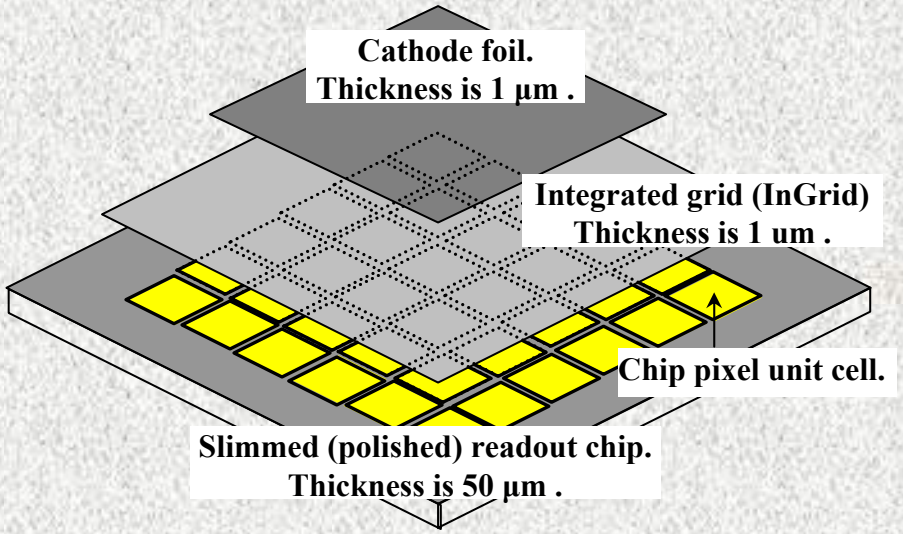
- projection of the track.
- 3D reconstruction of the track. .

GOSSIP detector: main features.

Hybrid pixel detector.



GOSSIP detector.



CONTRA

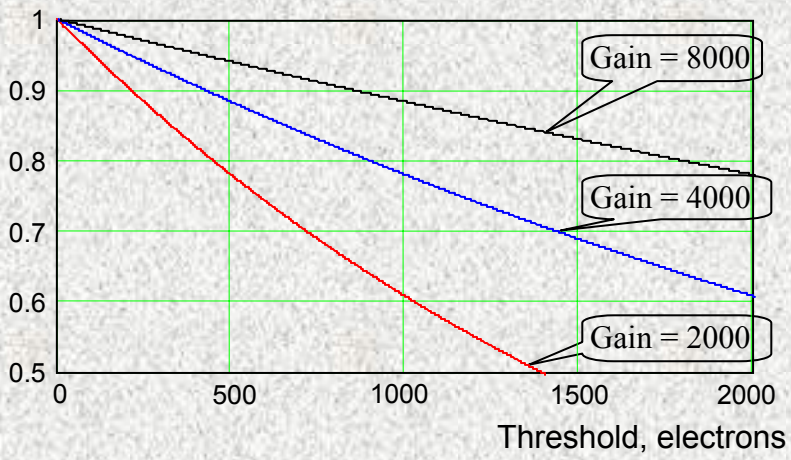
- spark protection

PRO

-can operate up to fluences of 10^{16} cm^{-2}
-low material budget
-negligible detector leakage current
-low detector parasitic capacitance

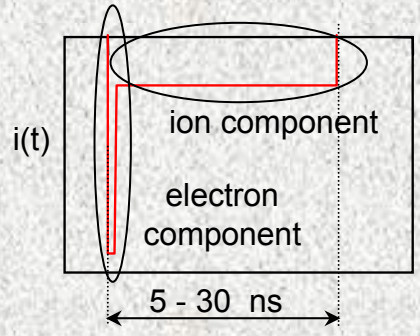
Inputs and requirements for the design of the input circuit.

Single electron efficiency.



- the low-threshold operation (THR < 400 e) is required.

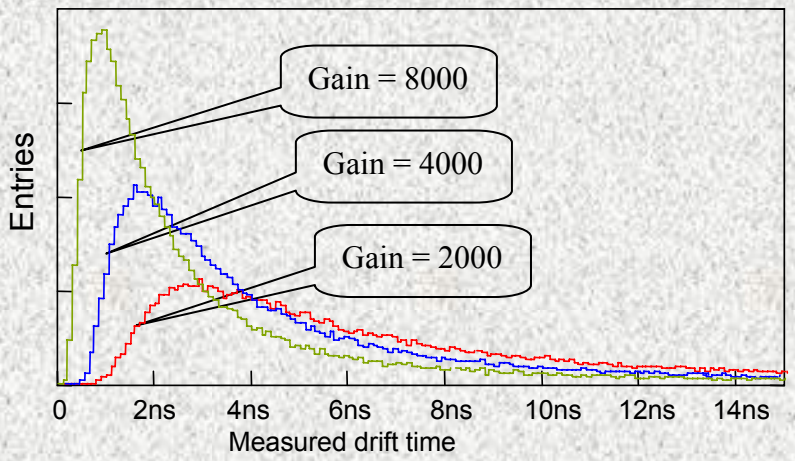
Shape of the detector current.



- motion of ions mainly determines the detector current.

Inputs and requirements for the design of the readout circuit.

Single electron drift time measurements (simulations)



- time resolution

$\sigma^{\text{time walk}}$ = 2 ns (100 μm) .

Power consumption.

Analog: 2 μW / pixel.

Total: 100 mW / cm^2 or 200 mW / chip.

low power dissipation

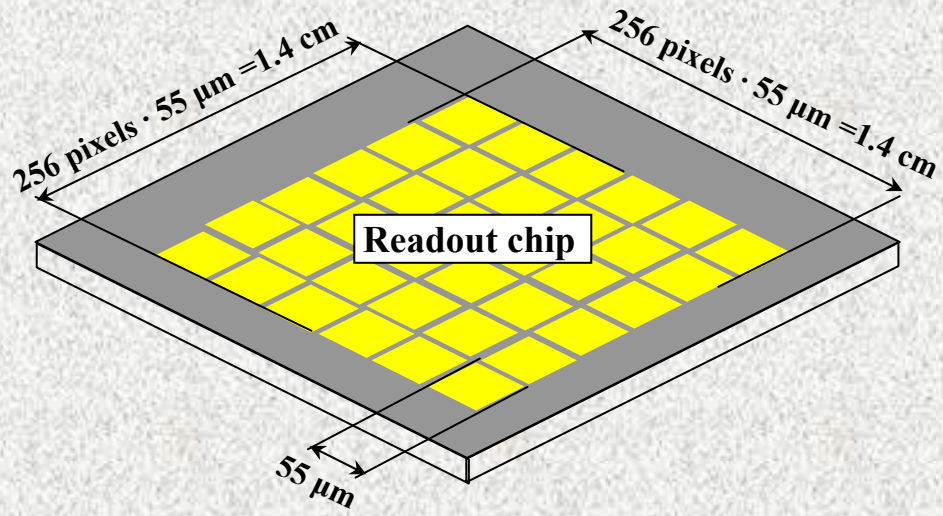
reduction of the material budget .

Inputs and requirements for the design of the readout circuit.

Analog-digital crosstalk.

-the high sensitive analog circuit must be effectively isolated from the high speed switching lines.

Pixel pitch and the chip size.

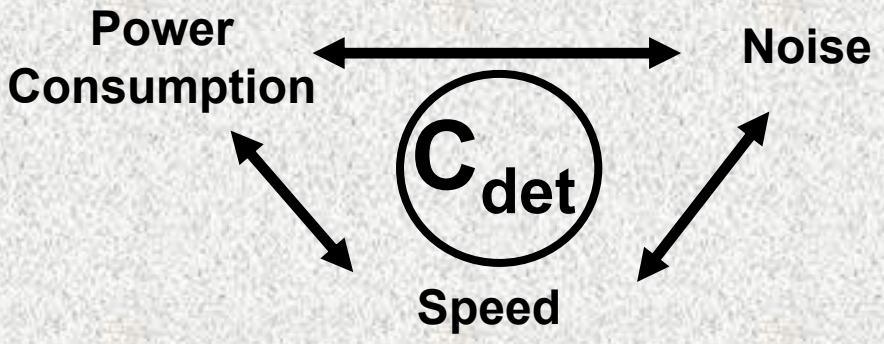


- pixel pitch 55 µm x 55 µm .

- sensitive area a matrix of 256 x 256 pixels (1.98 cm^2).

The prototype of the input circuit.

Parasitic capacitance at the input of the front-end circuit .



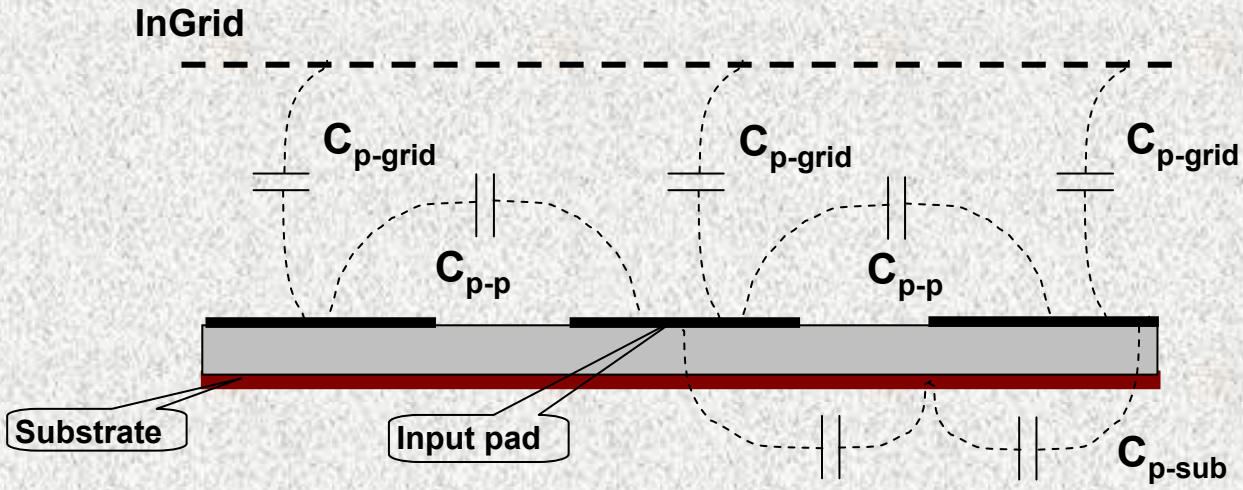
$$C_{det} = C_{par} = C_{p\text{-}grid} + C_{p\text{-}p} + C_{p\text{-}sub} \ ,$$

where

$C_{p\text{-}sub}$ is pad-to-substrate capacitance

$C_{p\text{-}grid}$ is pad-to-InGrid capacitance

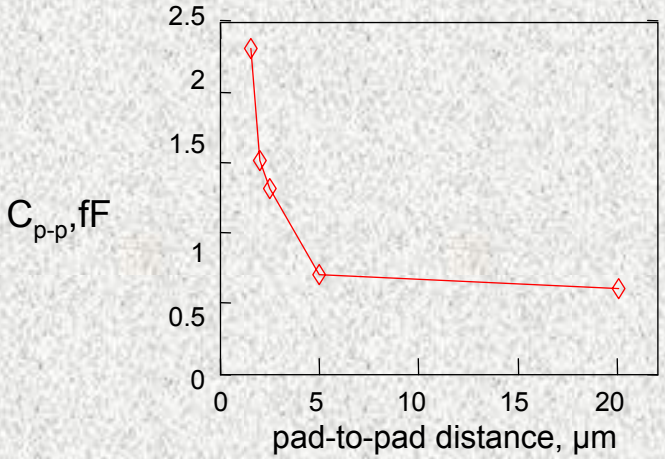
$C_{p\text{-}p}$ is pad-to-pad capacitance



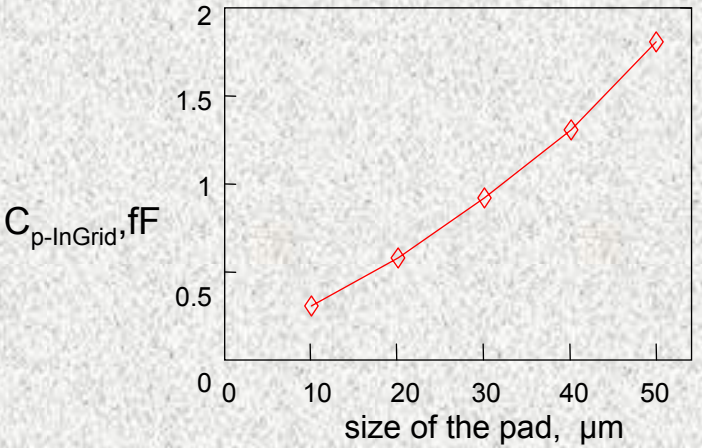
The prototype of the input circuit.

Evaluation of the input parasitic capacitances in 0.13 μm CMOS technology .

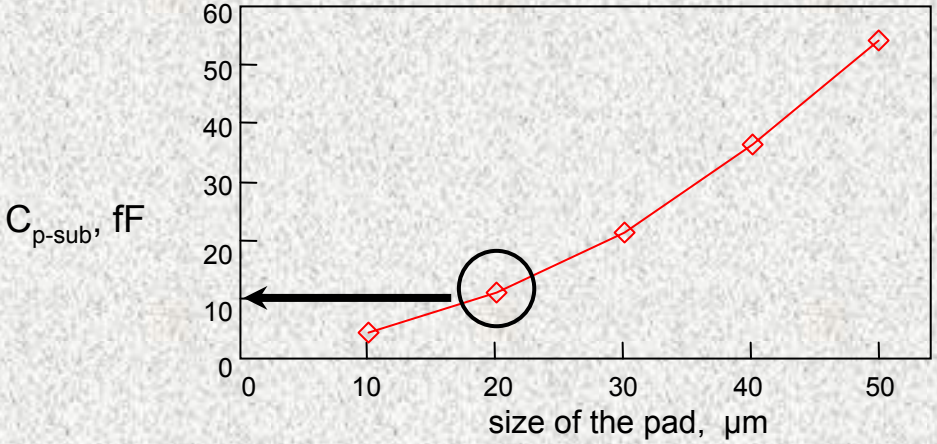
Pad-to-pad capacitance (Cp-p).



Pad-to-InGrid capacitance (Cp-grid).



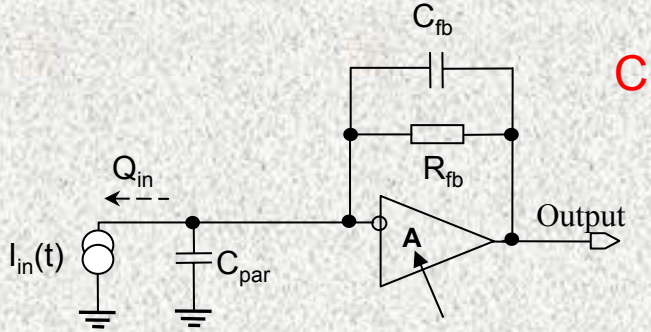
Pad-to-substrate capacitance (Cp-sub).



- input parasitic capacitance ≈ 10 fF.

The prototype of the input circuit.

Gain in the charge-sensitive preamplifier with a very low parasitic capacitance at the input ($C_{par} \rightarrow 10$ fF) .

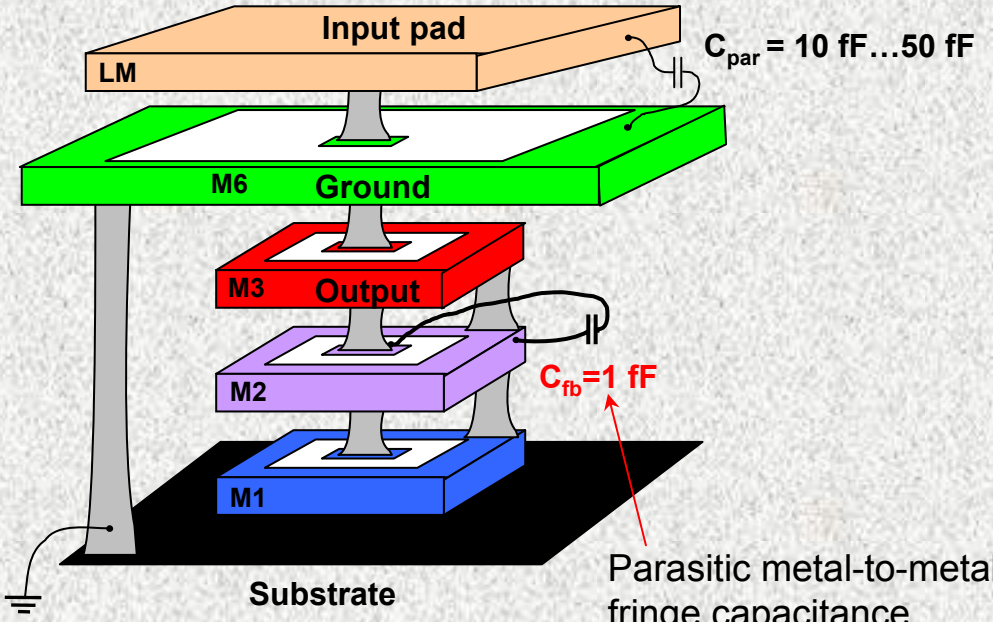


Open loop voltage gain of the OPAMP

$$\text{Charge-to-voltage gain} \approx \frac{1}{C_{fb}}$$

$$C_{fb} >> \frac{C_{par}}{A} \quad C_{par} \approx 10\ \text{fF},\ A \approx 130$$

Coaxial-like layout of the input interconnection.



Parasitic metal-to-metal fringe capacitance.

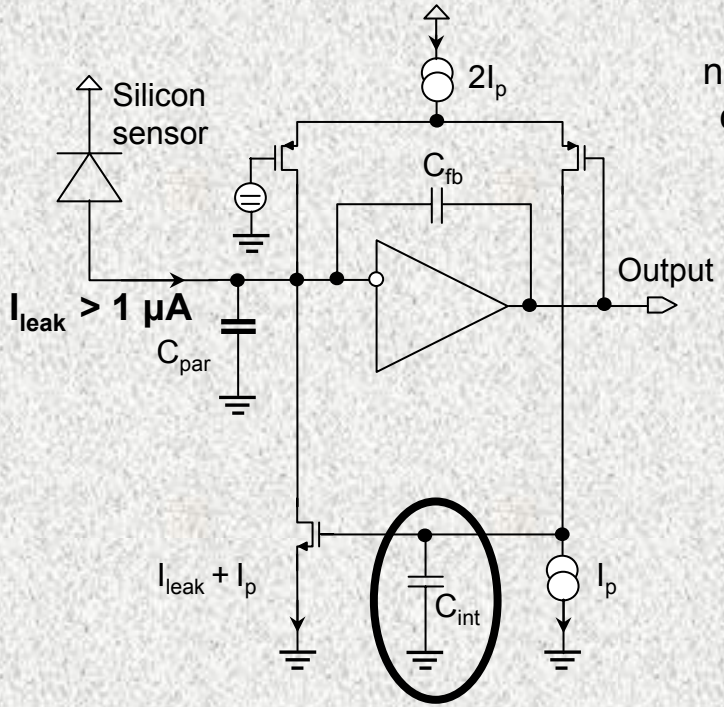
C_{fb} = 1fF ???

- Stability ?
- Physical layout ?

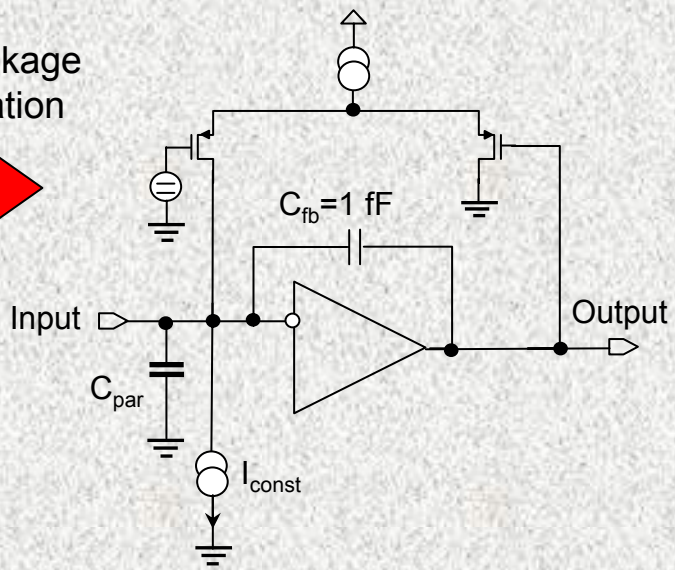
The prototype of the input circuit.

Stability of the charge-sensitive preamplifier with a very low parasitic capacitance at the input ($C_{par} \rightarrow 10$ fF).

- The scheme of F.Krummenacher



no need for the leakage current compensation

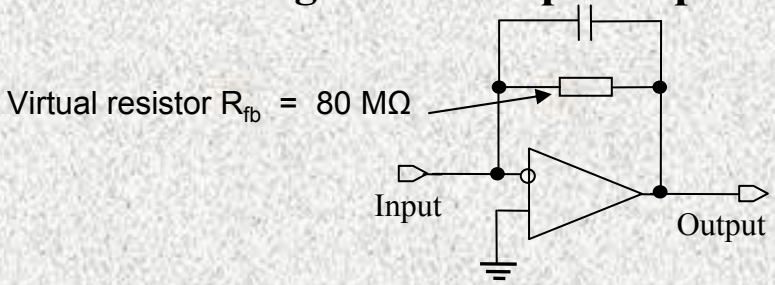


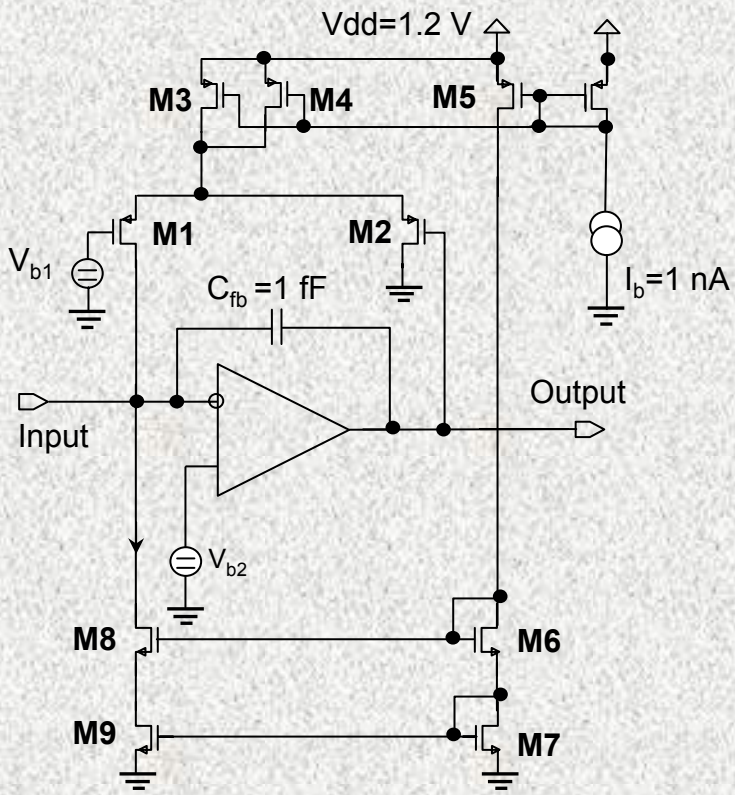
- This circuit becomes unstable when $C_{par} \rightarrow 10$ fF

- This circuit demonstrates a safe phase margin even when $C_{par} \rightarrow 10$ fF

The prototype of the input circuit.

DC feedback in the charge-sensitive preamplifier.





- allows for discharging of the feedback capacitor.

$R_{fb} = 1/gm^{M1} + 1/gm^{M2} = 80$ MΩ

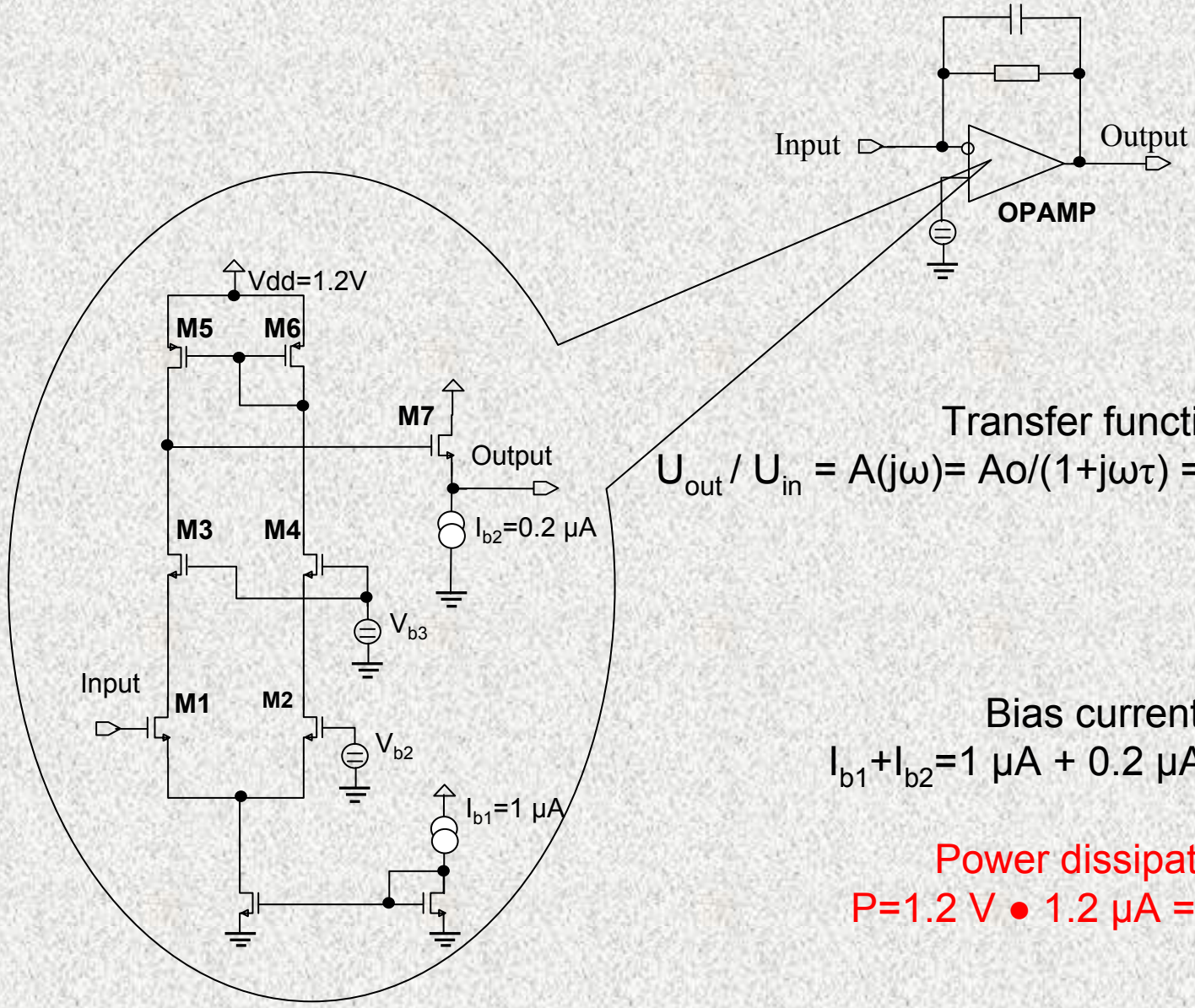
- biases the input of the circuit.

Statistical spread of the offset at the output

$\sigma(\delta U out^{DC}) = 20$ mV (170 e^-).

The prototype of the input circuit.

The operational amplifier.



Transfer function

$U_{out} / U_{in} = A(j\omega) = Ao/(1+j\omega\tau) = 130/(1+j\omega \bullet 14\ ns)$

Bias current

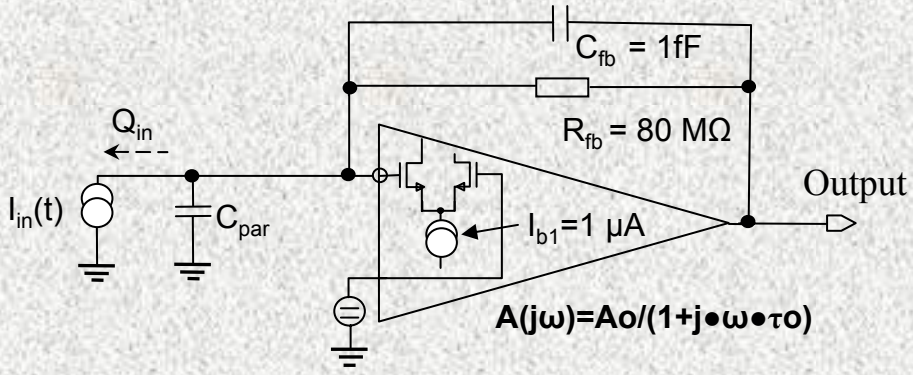
$I_{b1}+I_{b2}=1\ \mu A + 0.2\ \mu A = 1.2\ \mu A$

Power dissipation

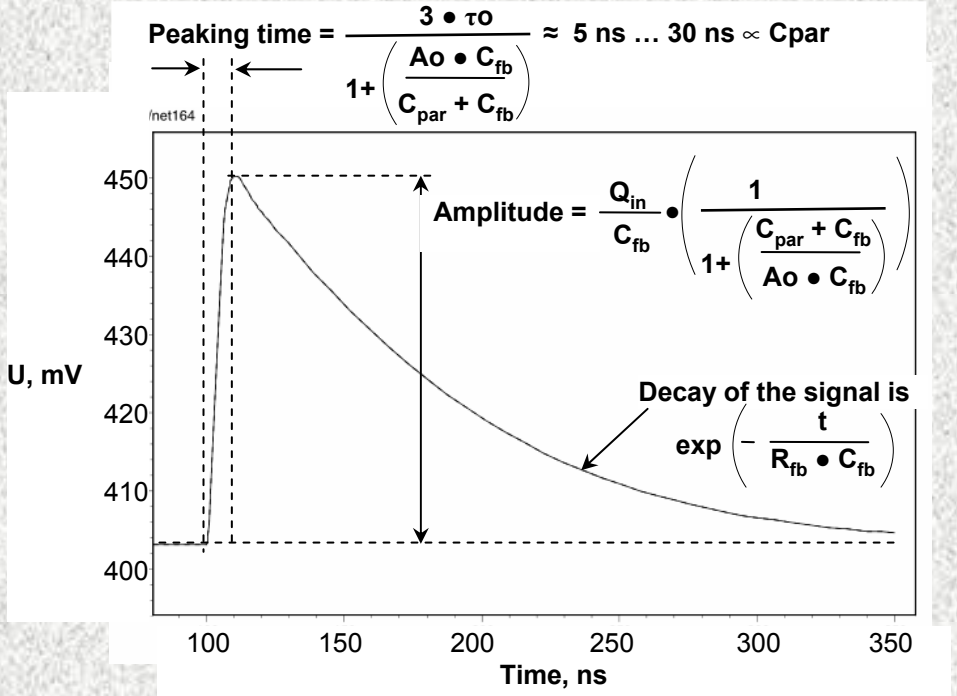
$P=1.2\ V \bullet 1.2\ \mu A = 1.5\ \mu W$

The prototype of the input circuit.

Pulse response and noise.



δ-pulse response of the preamplifier

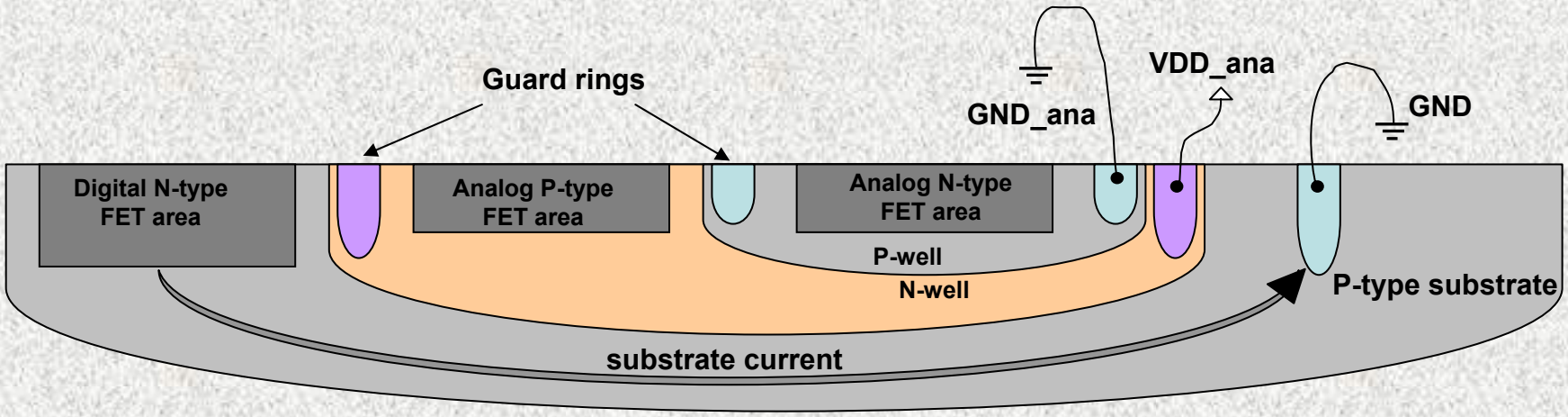


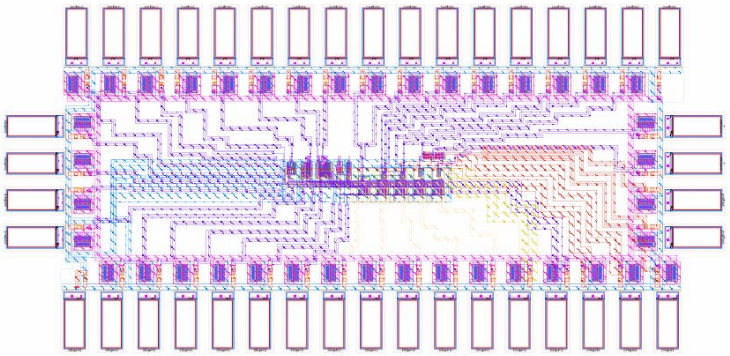
- response peaking time is 5 ns…30 ns.

ENC ≈ 60..80 e^- (RMS)
even with low bias current (I_{b1}=1 μA)
and
fast peaking time.

The prototype of the input circuit.

Physical layout aspect. **Floating P-well for analog NFETs.**



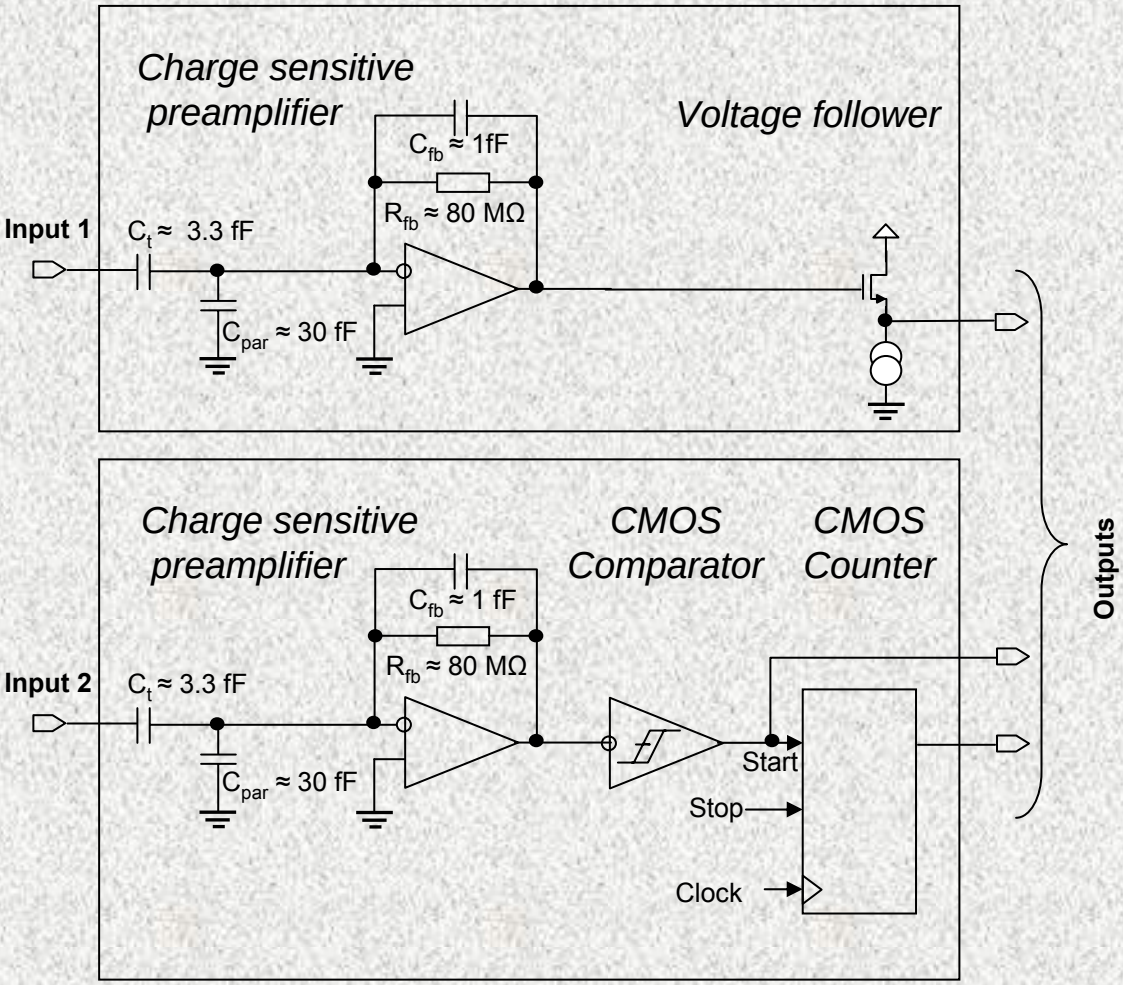


GOSSIPO chip, submitted on December 12, 2005.

- Triple well layout let us better isolate digital and analog parts of the chip.

The prototype of the input circuit.

Principal Block Diagram of the prototype.



Objectives for the first submit.

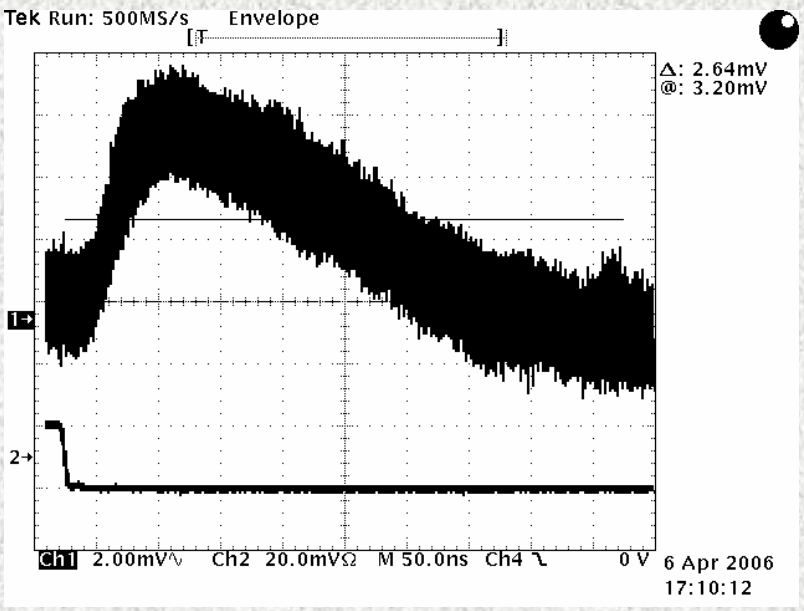
1) Operation of the proposed front-end circuit
   - -stability of the preamplifier
   - -pulse response
   - -noise
   - -channel-to-channel spread.

2) Cross-talk between the high sensitive analog circuit and high speed switching CMOS blocks.

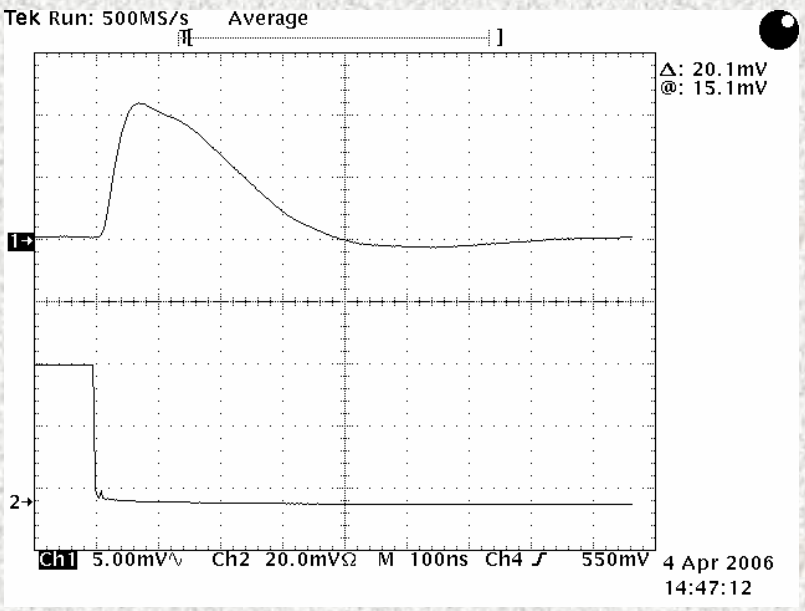
The prototype of the input circuit.

Measurements.

δ-pulse response of the preamplifier. Qin = 410 e^-



δ-pulse response of the preamplifier. Qin = 1000 e^-



- The preamplifier with (C_{par} = 35 fF and C_{fb} = 1 fF) demonstrates a stable operation and an expected pulse response and noise.

ENC = 60 e^- (RMS) .

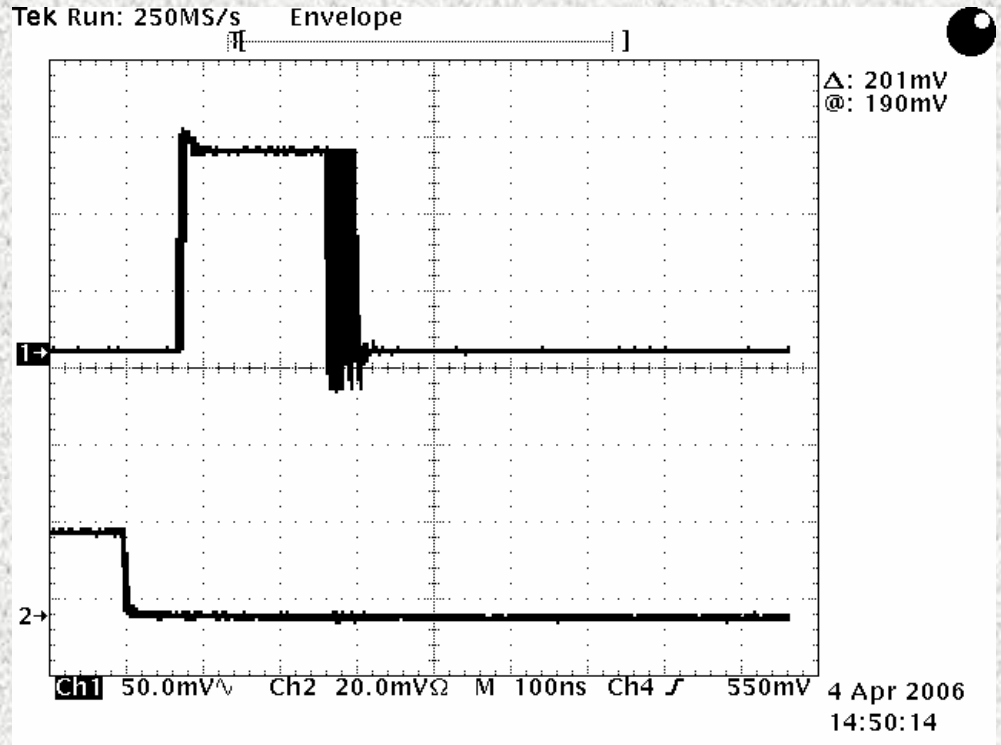
The prototype of the input circuit.

Measurements.

δ-pulse response at the output of the CMOS comparator.

Qin = 410 e^-.

Threshold = 300 e^-.



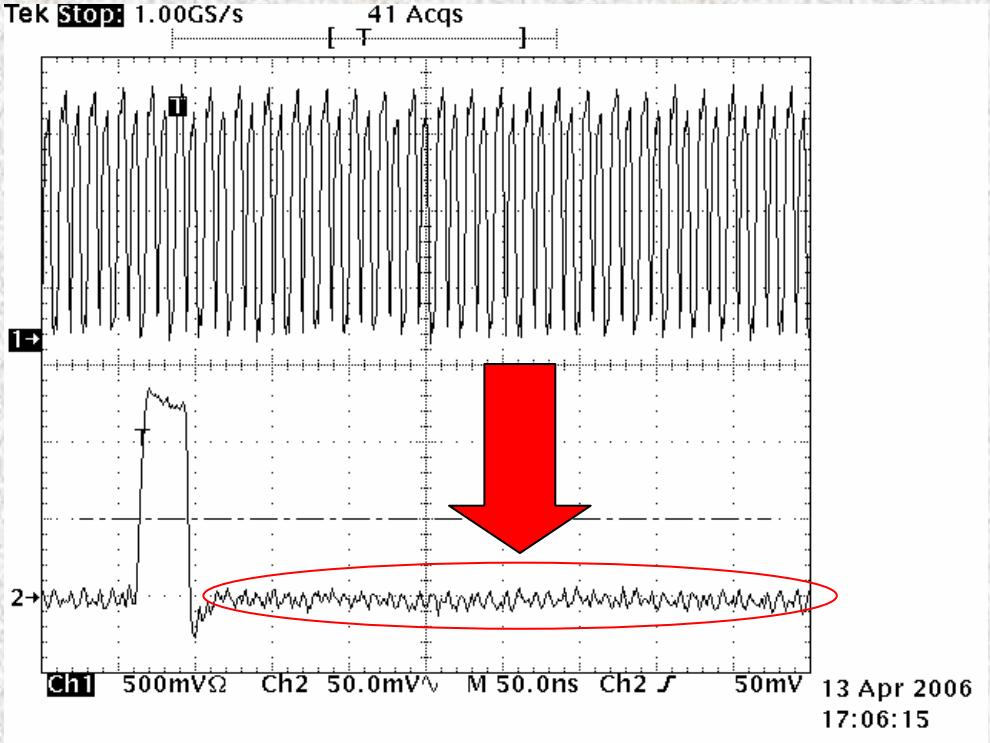
- The channel-to-channel spread of the threshold is $\sigma^{THR} \approx 160\ e^-$ (consistent with simulations).

The prototype of the input circuit.

Measurements.

Clock signal is running at 100 MHz.

The output of the comparator.
Threshold = 300 e^-



- no significant crosstalk between the high sensitive input and the 100 MHz clock line.

Conclusions and plans.

Front-end readout circuit of the GOSSIP chip will benefit from the low detector parasitic capacitance and no need to compensate for the leakage current.

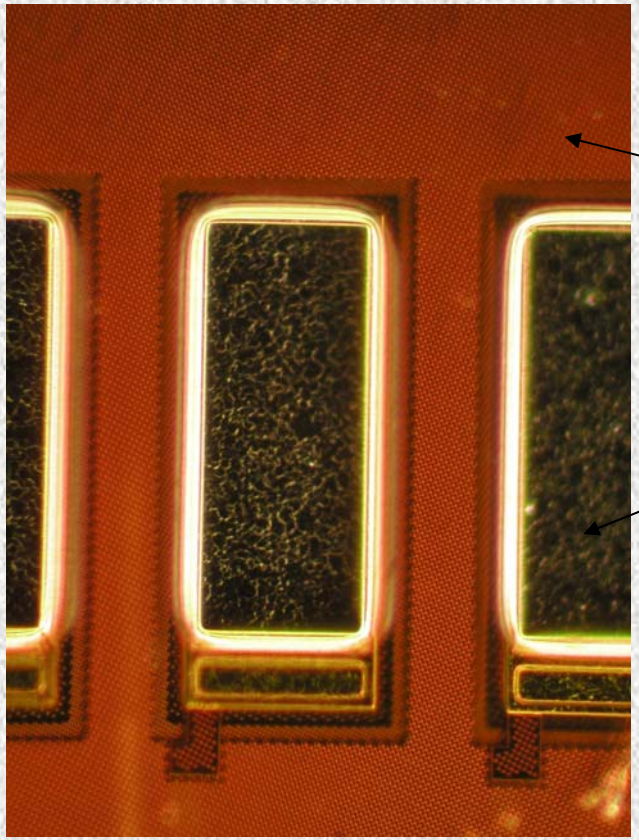
- The first prototype of the fast (40 ns peaking time), low-noise (ENC = 60 e^- (RMS) and low-power (2 μw per channel) input circuit for the GOSSIP chip has been successfully implemented in 0.13 μm CMOS technology.

- Owing to the triple well layout used in the prototype, the high sensitive analog inputs have been effectively isolated from the high speed switching gates.

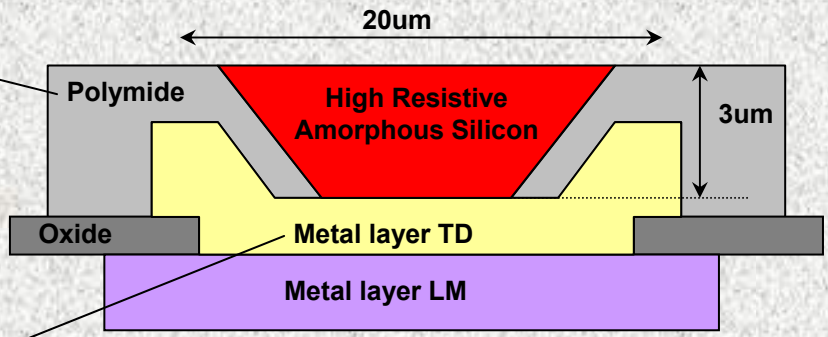
- A new prototype featuring TDC-per-pixel concept will be submitted in the end of 2006.

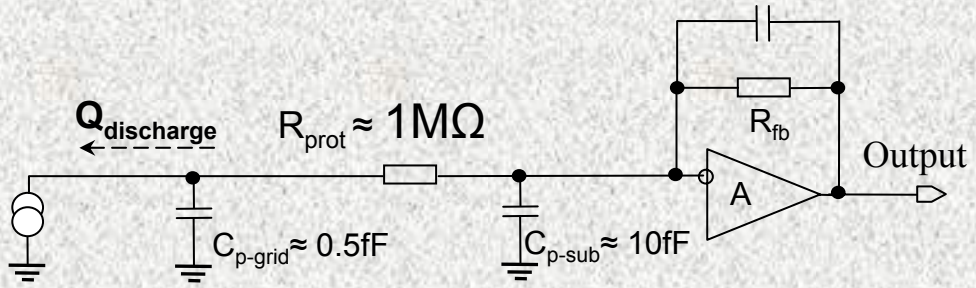
Additional slide.

Protection against discharges.



Layout of the input pad





- protective resistor causes neither signal distortion nor noise increase as long as $R_{prot} \bullet C_{p\text{-}grid}$ is less than 1ns.

Additional slide.

Integrated Grids.