Performance of the CMS ECAL Very Front End Electronics

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Abstract

We report the results of tests of 12880 Very Front End (VFE) readout cards for the barrel of the CMS electromagnetic calorimeter. A thorough test sequence was applied to each card including power-on test, burn-in and final calibration.

Cards failing the tests were at the few per mille level. The results prove the very high quality of the VFE cards.

I. INTRODUCTION

The CMS [1] electromagnetic calorimeter (ECAL) is divided into the Barrel (EB) and two end-caps (EE) made of 61200 and 14648 crystals, respectively. The EB is split up into 36 supermodules with 1700 crystals each [2]. The EE is made of 4 DEE's with 3662 crystals each.

The scintillation light of the crystals is converted into an electrical signal by two Avalanche Photo-Diodes (APD) for the EB. The Very Front End (VFE) card is used to amplify, shape and digitize the signals coming from the Avalanche Photo-Diodes. The VFE comprises five identical read-out channels, serving five crystals.

Each channel has a Multi Gain Pre-Amplifier (MGPA) [3] and a four channel ADC followed by LVDS to CMOS level-converters (LVDS_RX). The signals are pre-amplified and shaped and then amplified by three amplifiers with nominal gains of 1, 6, and 12, covering a dynamic range of 60 pC. The shaping is done by a CR-RC filter with a shaping time of 40 ns. The output pulse non-linearity of the MGPA is less than 1%. Its noise, in the Barrel case, is about 8000 electrons for gain 6 and 12, and about 28000 electrons for gain 1. The MGPA contains three programmable 8-bit DACs to adjust the output signal levels to the ADC inputs. An integrated test pulse generator with amplitude which is adjustable through an 8-bit DAC allows a test of the read-out electronics over the full dynamic range.

The 3 analog output signals of the MGPA are digitized in parallel by a 4-fold 40 MHz 12-bit ADC (AD41240) [4]. It has an effective number of bits of 10.9. Digital logic internal to the ADC selects the highest not saturated pulse for output. A Detector Control Unit (DCU) measures the leakage currents of the five Avalanche Photo Diodes. In addition it measures the resistance of thermistors which are attached to every 10^{th} crystal hence monitoring the temperatures.

Each VFE is identified by a barcode (figure 1). This allows its unique identification and registration into a data base.

All active components are application specific integrated circuits (ASICs) implemented in 0.25 μm technology.

The electronics production for the ECAL Barrel and the tests of all 12880 VFE cards, which corresponds to 340 cards per supermodule and spares, is completed. The electronics production for the ECAL end-caps is on going.

The test sequence included:

- Automatic Optical Inspection (AOI) done by the manufacturer.
- Power-on test: It is the first electrical test of the VFE cards. It measures the voltages, the currents and performs a functional test of the card.
- Burn-in [5] test for 72 hours at 60 ºC.

Calibration of the characteristics of each individual channel by measuring the gain in units of ADC counts per pC, the pedestal, the noise, the linearity including a complete functional test.

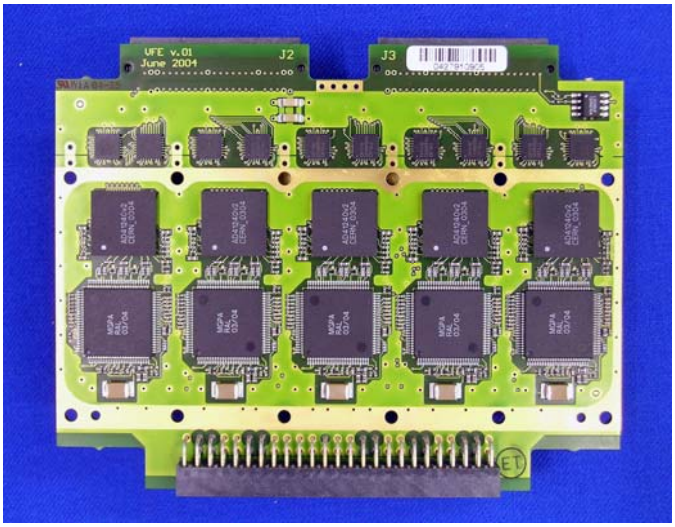

Figure 1: Very Front End card

II. POWER ON TEST

The power-on test [6] is a quick (~30s) electrical test of the VFE card [7]. All VFE cards are tested twice, once by the manufacturer (ASCOM Schweiz AG) before delivery and after reception in the ECAL electronics integration centre at CERN. Three copies of the test system have been built: one system is at CERN and two are at the manufacturer.

The test system is composed of a programmable power supply, a barcode reader, a dedicated electronics board which includes a Xilinx FPGA, and one NI DAQ card. A Labview program interfaces the test system via RS232 bus.

The VFE needs three separate supply voltages of 2.5V: one for the MGPA and the analog part of the ADC, one for the digital part of the ADC and a third one for the LVDS to single ended CMOS buffers (LVDS-RX converter). The output voltage of the power supply and the 3 input voltages of the VFE card are measured with a NI DAQ PCI-6013 card. The corresponding currents are determined by measuring the voltage drops over calibrated shunt resistances with nominal value of 0.033Ω.

A functional test of the VFE is performed using the Xilinx FPGA to acquire the data digitized at 40 MHz:

It records and analyzes the data generated by the MGPA's internal test pulse system.

It selects the ADC gain modes.

It reads simulated APD leakage currents and crystal temperatures from the DCU.

The FPGA triggers and reads one pulse per channel and verifies the correct shape of the signals. It collects 64 equidistant samples and determines the pedestal, the noise and the amplitude of the three output pulses and calculates the real gain of every channel. Pulse heights and pedestal are compared within defined limits. The pulse shapes are plotted and the calculated numbers are printed on the front page of the test program (see fig.2).

The system also measures the leakage current from the DCU and the temperature. The results of the power-on test are stored in two different text files, one for voltage and current and another for the functional test.

The distribution of the analog, digital and buffer voltages measured by the power-on test are Gaussians with mean values of (2.489, 2.499 and 2.45) V and RMS errors of (0.001, 0.001 and 0.03) V.

The distribution of the currents are Gaussian with mean values of (1.482, 0.529) A and with RMS errors of (0.008, 0.01) A, respectively for the analog and the digital part; the buffer current is included into the digital measurement.

Of the 12880 VFE cards produced, 109 cards were rejected during the power-on test.

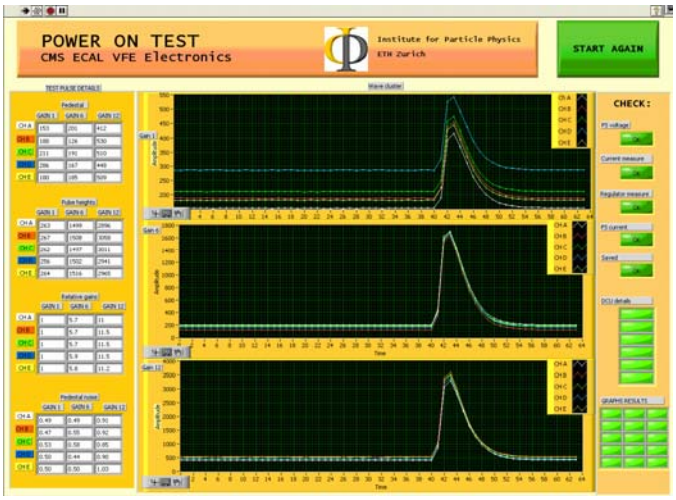

Figure 2: POT front page: on the left pulse height, pedestal, noise and relative gains are given. On the right the plots show the pulse shape of the 3 gains.

III. BURN IN

All the ECAL Barrel VFEs that have passed the power-on test are burned-in.

The burn-in [8] [9] is carried out to find infant mortality failures and freak failures and to guarantee the device's reliability. Typical problems that can be observed during burn-in are for example broken chips, bad soldering or nearly open bonds. They usually occur in the first 20 hours of the card's operation.

Freak failures result from defects in the component's structure leading to a hot spot. The lifetime of freak failures is usually higher than infant mortality failures.

The tests are performed at higher temperature since the failure rate depends exponentially on the temperature; according to the Arrhenius model the reaction rate varies as $e^{-Ea/kT}$ with an estimated activation energy of E_a = 1 eV. Thus the aging of the device is 100 times faster if its operating temperature is increased from 25°C to 65°C. Therefore a burn-in period of 3 days at an elevated temperature of 60°C has been chosen. Up to 300 cards are tested in one go. All cards are powered at their nominal voltage of 2.5 V during the test. The 40 MHz clock is distributed to the cards using a special mother board. A PC workstation monitors the clock and the total current of each of the 300 VFE cards.

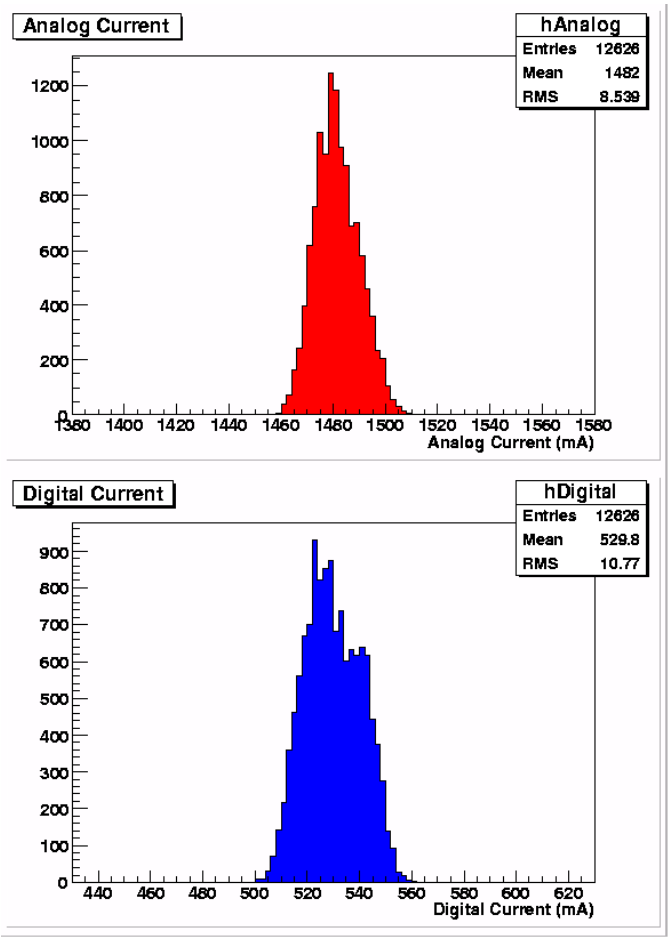

Figure 3: analog and digital current distribution for the whole production of VFE for the ECAL BARREL

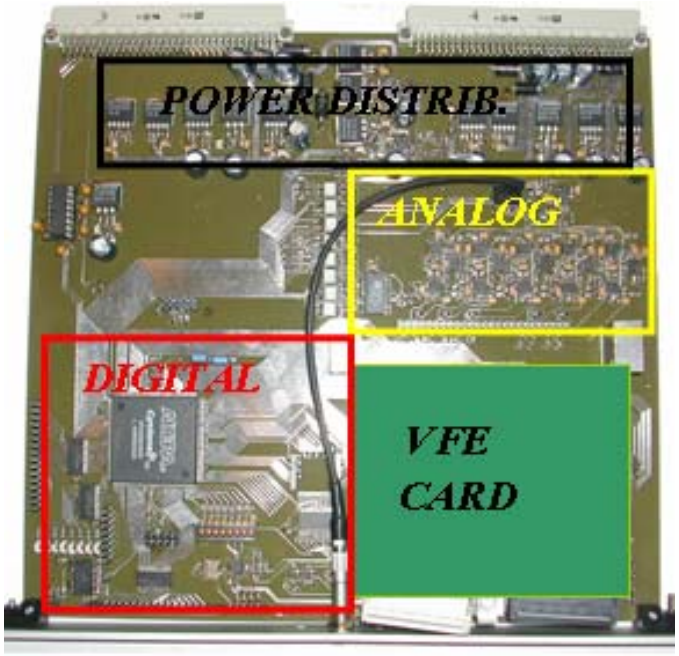

Figure 4: the calibration board

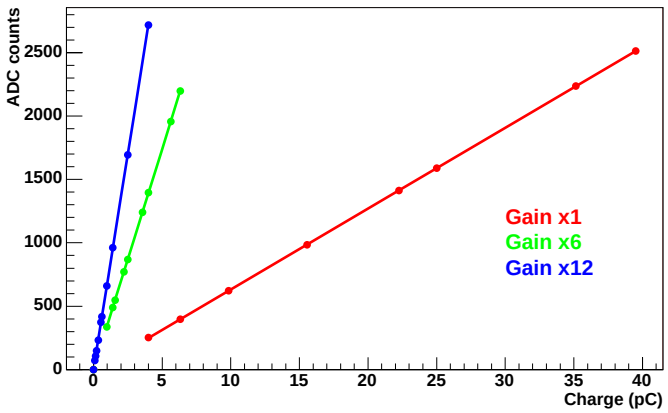

Figure 5: typical set of calibration curves for the 3 gains of a single channel of a VFE card.

IV. CALIBRATION TEST

The calibration test [6] [8] determines the characteristics of each channel by measuring the pedestal, noise and the linearity for the three different gains.

The calibration set up comprises:

- Six calibration boards (fig. 4).
- an Agilent 33250A waveform generator
- programmable CAMAC attenuator
- a PC running LabWindows
- a CAMAC fan out
- a bar code reader

The whole setup is housed in a 6U crate with a custom designed backplane. The backplane provides the power for the digital and analog part of the six calibration boards. It also controls the communication between the different calibration boards and the PC via a RS232 interface.

A. The calibration sequence

Each VFE is inserted into a calibration board using a dedicated mechanical support. An ALTERA FPGA (see fig. 4) present in each calibration board sets the pedestal values for each channel and gain to roughly 160 ADC counts.

The linearity of the MGPA is measured by injecting 21 different charges (see table 1). The charges are generated by applying different voltages onto calibrated capacitors (10.0±.01) pF. These voltages are obtained from a constant voltage source using a programmable attenuator. Plotting the known charges versus the ADC response yields a curve whose slope corresponds to the gain measured in ADC counts per pC (see fig.5). In this way the full dynamic range of the 3 gains is covered. Cross calibration of the 3 gains is achieved by taking advantage of overlapping gain curves (cf. table 1).

The input charge of 3.9 pC is the only value that can be measured in all three gains.

Charge in Gain 1	Charge in Gain 6	Charge in Gain 12
3.9	1.0	0.09
6.3	1.4	0.16
10	1.6	0.22
15.8	2.2	0.35
22.3	2.5	0.56
25.0	3.5	0.62
35.4	3.9	1.0
39.7	5.6	1.4
	6.3	2.5
		3.9

Table 1: Input charges for the three nominal gains. Values measured in more than one gain range are indicated in red.

	Gain 1	Gain 6	Gain 12
Slope (ADC counts/pC)	64.6±0.8	350.3±3.8	683.2±7.9
Offset (ADC counts)	-6.2±0.9	2.4±1.1	1.7±0.9

Table 2: Gains and offsets extracted from the calibration data of the 12625 VFE cards having passed all criteria.

B. Analysis and results

During the calibration test a program performs an on-line linearity check of each channel for all the three gains. The charge pulses are fitted and the peak position are determined (see fig.7). The three gains are obtained by plotting the extracted peak positions versus the corresponding input charges and by applying a linear least square fit to the data points (see fig.5). Slopes, offsets of the fitted lines are given in table 2. Only channels with coefficient of determination $r^2 > 0.9999$ are accepted.

A similar test is done using the internal test pulse of the MGPA. In this case 12 charges are injected instead of 21.

The accuracy of the APD leakage current measurement is tested using a current source to simulate a leakage current between 0 and 200 nA on the input of the VFE card. The data are collected by the DCU chip on the VFE and are sent to the data acquisition system via the RS232. The test board uses a digital potentiometer instead of a thermistor to test the temperature read out. The resistance of the potentiometer is varied in 15 steps from100 to 160 kΩ. All measured values are saved, and later stored in the REDACLE database [10] together with all other results.

Since the calibration set-up did not allow to measure precisely the RMS error of the pedestal,

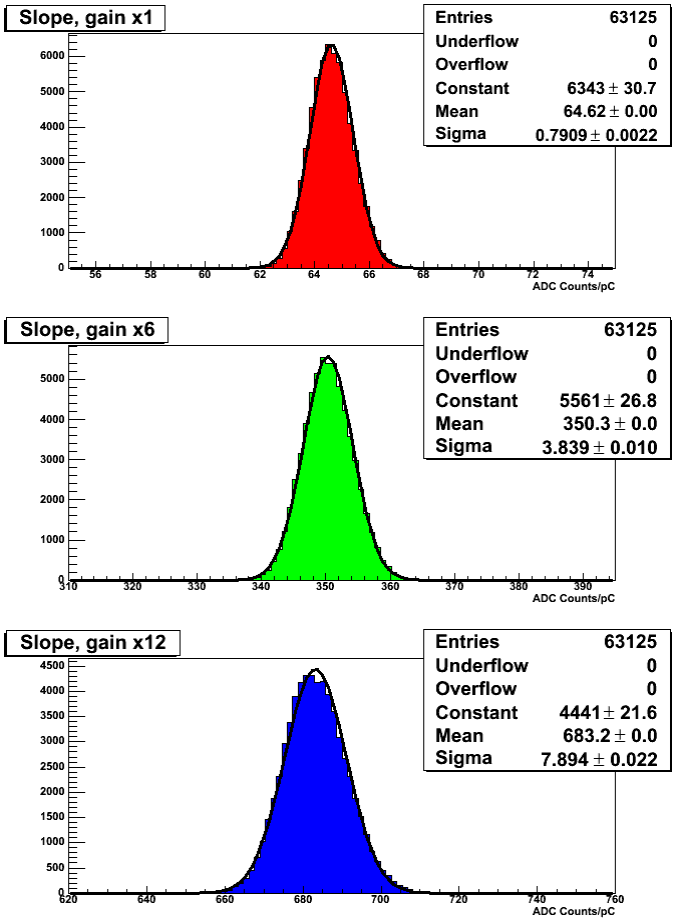

Figure 6: distribution of the slope in the gains 1, 6, 12

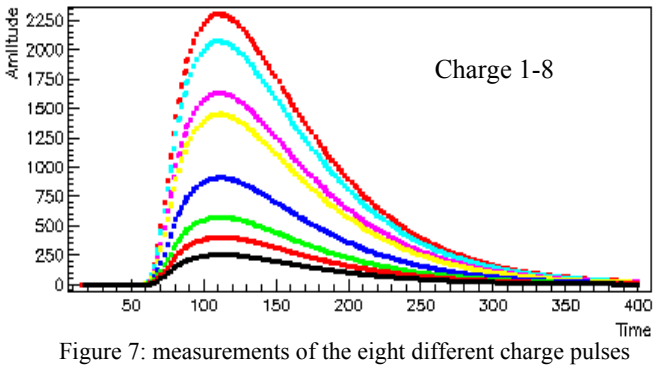

Figure 7: measurements of the eight different charge pulses injected in gain 1

the noise figure reported here stems from measurement of VFE cards already integrated in supermodules. Of the 36 supermodules 23 have been fully assembled and have shown a uniform and extremely stable noise distribution (see fig.8). The noise obtained is typically 1.1, 0.75 and 0.6 ADC counts for gain 12, 6 and 1, respectively; the relative gains (see fig.9) are 5.42 and 10.57 with RMS values of 0.047 and 0.11 compared to the design values of 6 and 12, respectively.

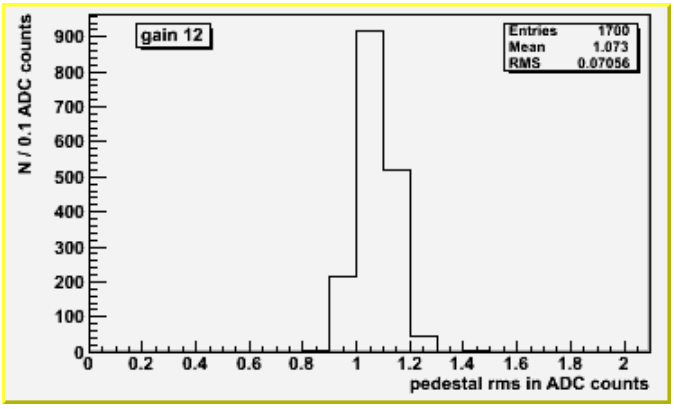

Figure 8: typical noise distribution of gain 12 in a supermodule.

V. Conclusions

The production of the VFE cards for the ECAL Barrel is finished and all cards are tested and calibrated. Roughly 66% of all supermodules of the Barrel calorimeter are fully assembled.

Given the quality achieved the tests and actions chosen were adequate and the overall test strategy was a success.

Of 12880 cards produced, 2% failed the tests: 149 were rejected during calibration and burn-in, 106 were rejected during power-on. 12625 cards passed all tests.

VI. References

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[10] **REDACLE Database website** http://pceth69.cern.ch/redacle/pages/php/index.php

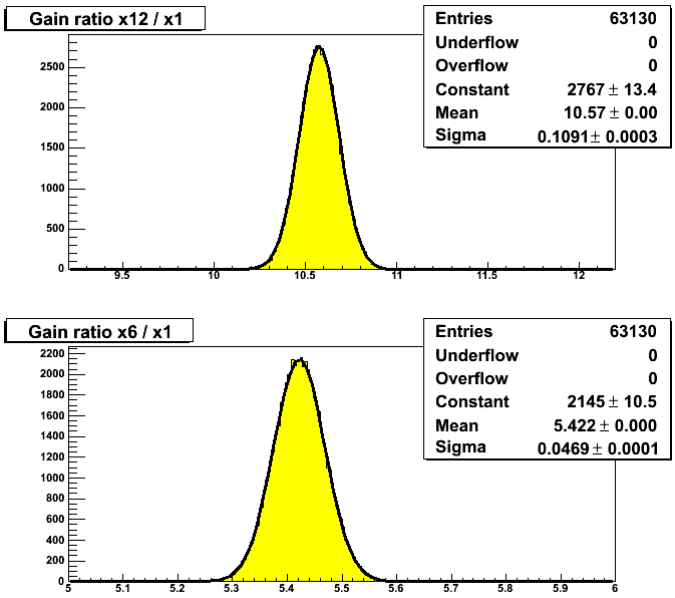

Figure 9: final distribution of the gain ratio.