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A Read-out Driver for Silicon Detectors in ATLAS

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I present an overview of a read-out driver (ROD) for silicon detectors in the ATLAS experiment at the Large Hadron Collider (LHC). Two silicon-based ATLAS tracking systems, referred to as the Pixel Detector and the Semiconductor Tracker (SCT), are controlled and read-out using a common 9U VME board. A hybrid design of Field Programmable Gate Arrays (FPGAs) and Digital Signal Processors (DSPs) has allowed the Silicon ROD to meet the challenges of format error-counting and event trapping without interfering in the construction and transmission of event fragments to the next level in the read-out system. Performance of the ROD during detector assembly, calibrations and cosmic-ray data-taking are also discussed.

Summary

The ATLAS experiment is a general-purpose detector centered around one of the LHC *pp* collision points. Two major ATLAS detector subsystems lie closest to the interaction point–the Pixel detector, comprised of more than 8.0×10^7 channels (1744 modules), surrounded by the SCT, itself containing more than 6.2×10^6 channels (4088 modules); both are essential for providing the tracking information used to tag secondary vertexes from b-hadron decays. The ROD is a 9U VME board common between both of these detector systems and designed to meet the formidable challenge of module configuration and read-out, trigger distribution and event fragment construction.

Each VME board is responsible for the configuration and read-out of up to 48 SCT or 32 Pixel modules. A hybrid architecture of FPGAs and DSPs allow the ROD maximum versatility during physics-running and calibrations. The FPGAs are dedicated to performing ROD setup and module configuration in addition to the formatting, building and routing of events. A single Master" and fourSlave" DSPs reside on the board and are utilized for the control and coordination of on-ROD operations, as well as performing high-level tasks such as data monitoring and module calibration. Once configured, the ROD FPGAs handle the event data path to Level-Two without further assistance from the DSPs.

The Master DSP (MDSP) controls and coordinates ROD operations via a register bank connected to one of its external memory interfaces (EMIF). Two additional EMIFs are utilized for storing additional program code and general data (\emph{ e.g.}, module configuration data). A re-programmable boot ROM is attached to the fourth EMIF allowing the MDSP to load initial code upon start-up. The MDSP's host port interface allows a host CPU continuous access to its internal memory banks.

The four Slave DSPs (SDSPs) are used for error counting as well as event capture and histogramming. One EMIF of each SDSP is connected to a separate pipeline in the Router FPGA, thus allowing events to be transferred independently to any SDSP. SDSP external memory is used to store event histograms. The full memory range of the four SDSPs are available to the MDSP through registers attached the the SDSP host port interfaces.

ROD calibration mode is utilized for running a sequence of module communication and functionality tests that optimize optical receiver settings, verify the function of BC and Level-1 ID counters, set charge injection timing and measure gain offset and noise. Calibration mode has been used extensively during detector assembly–an individual silicon module is thoroughly tested prior to being mounted on a barrel or a disk.

With the advent of SCT commissioning using cosmic-rays, the optimization of ROD software and firmware will continue in concert with working to meet the challenges of Simple Link Interface (S-LINK) readout during physics-running and multi-ROD operation.

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