The LHC beam loss monitoring system's data acquisition card

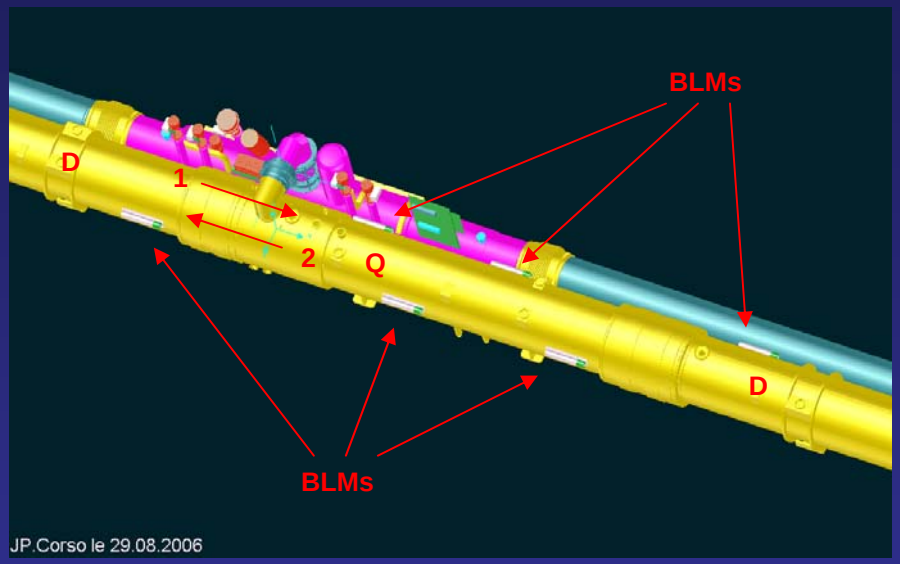
Ewald Effinger

AB-BI-BL

Outline

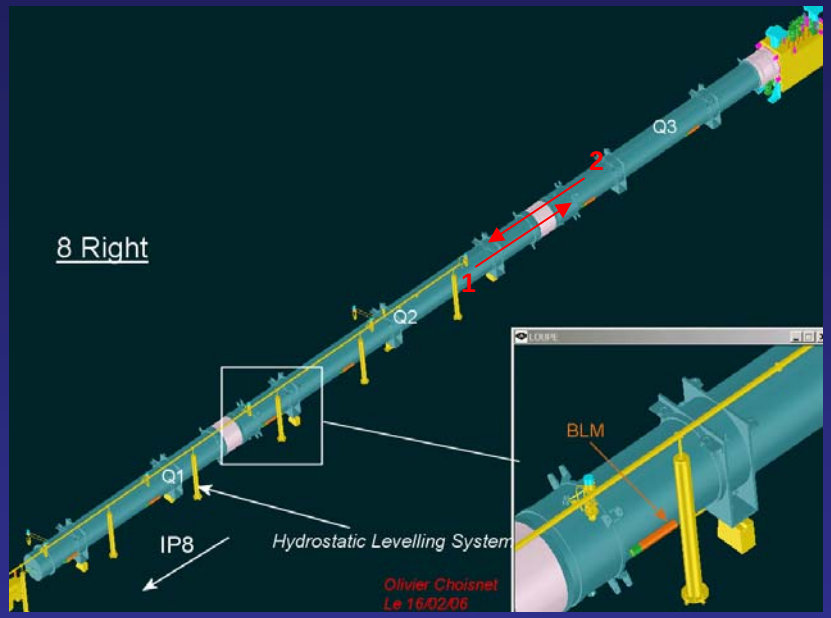
- Introduction: the BLM System
- Specification of the BLM DAC
- The data acquisition card
- FPGA functionality
- Tests during operation
- Measurement results
- Conclusion
- Acknowledgement

Introduction: the BLM System



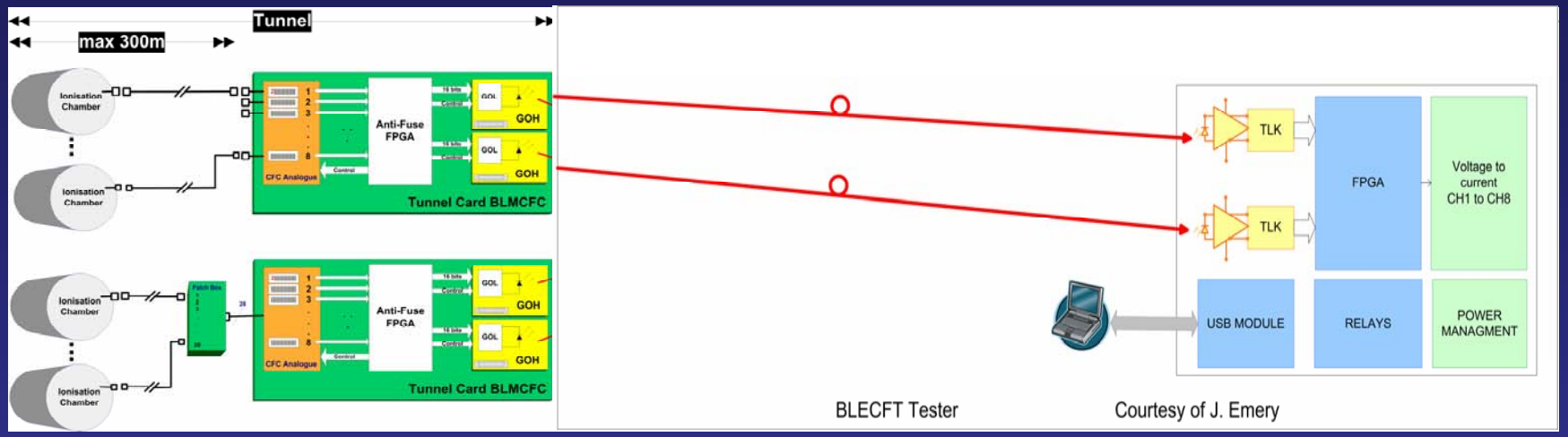
- 3680 Ionization chambers
- 290 Secondary emission monitors
- 650 BLM data acquisition cards
- The cards in the arc are installed underneath the magnets in a 19'' create

Introduction: the BLM System



- Electronic cards are installed in the nearby side-tunnels, because of reduced radiation level
- Up to 6 x 19“ crates with 10 DACs are installed in the straight section
- Signal cable with length up to 600m

Introduction: the BLM System



- Optical links are connected to 340 threshold comparators (TC) with an optical receiver card on the surface
- 25 VME creates are distributed around the LHC
- Each create includes a PowerPC (data logging), a Combiner card (connected to the beam interlock system), and two timing cards
- USB connected system for test and development

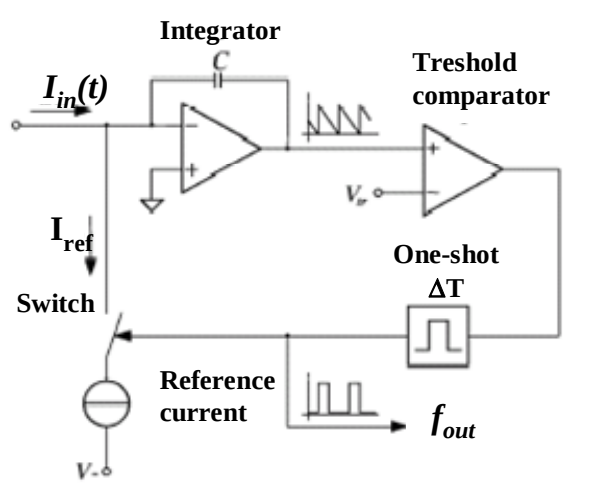
Specification

- Radiation tolerant up to 500Gy (20 LHC lifetime)
- Reliability level SIL3 (10^{-6} to 10^{-7} failure/h) to protect the equipment of damage
- Current measuring range 2.5pA to 1mA
- Error +/-25% in the range from 1mA to 1nA
- Error +100%/-50% in the range from 1nA to 10pA
- Integration time window 40us

Specification

- Input over-current protection: 10A@100µs
- Input over-voltage protection: 1500V@100µs
- Redundant optical data transfer to surface
- Test features for system check
- Survey of the card voltage supplies
- Survey of detector high voltage supply

The acquisitions card

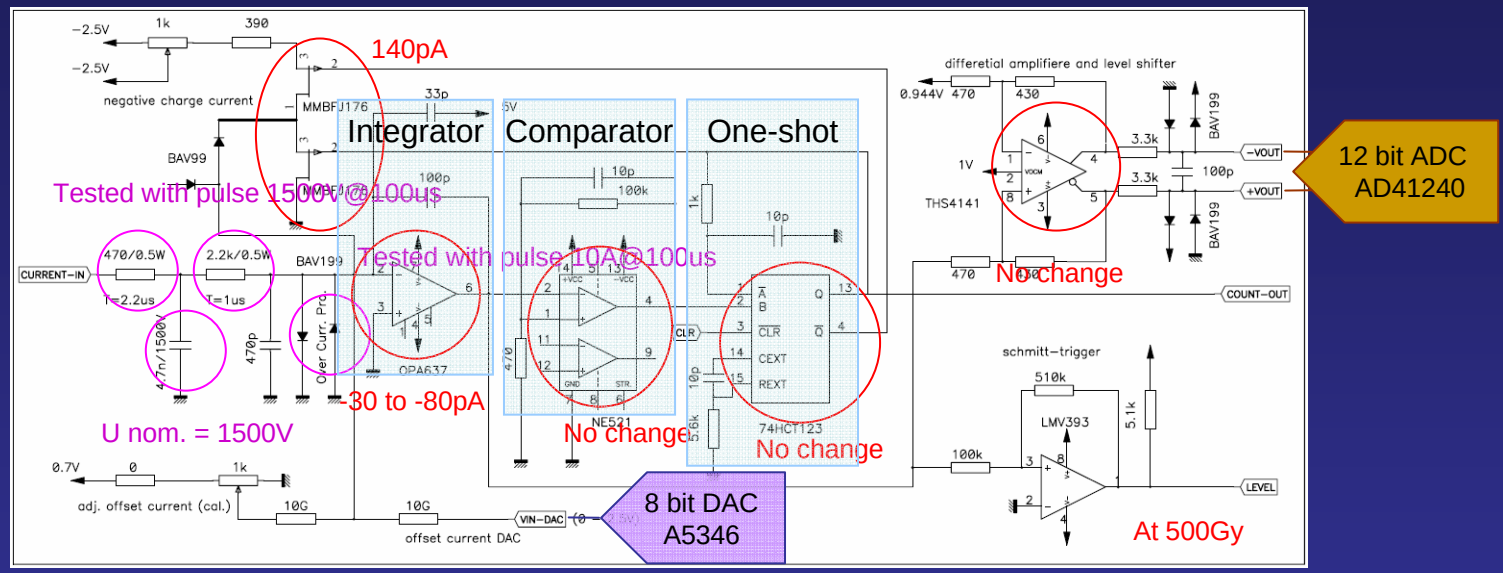


Input Current	Output frequency
1mA	5MHz
1uA	5kHz
1nA	5Hz
1pA	5mHz

Essentials of the input circuit

- Current to frequency converter (CFC)
- Balanced charge integrator
- No charge loss (“no blind time”)
- Very large dynamic range
- Output frequency depends on input current

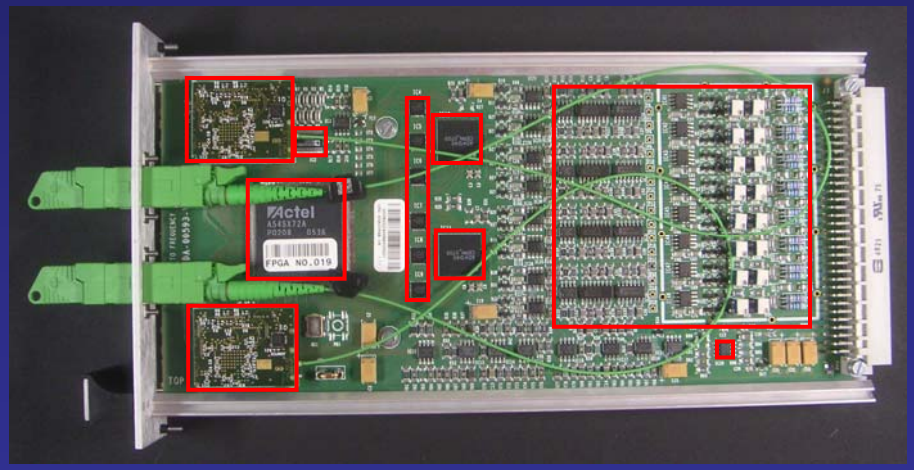
The acquisitions card



Measures to fulfill the specification

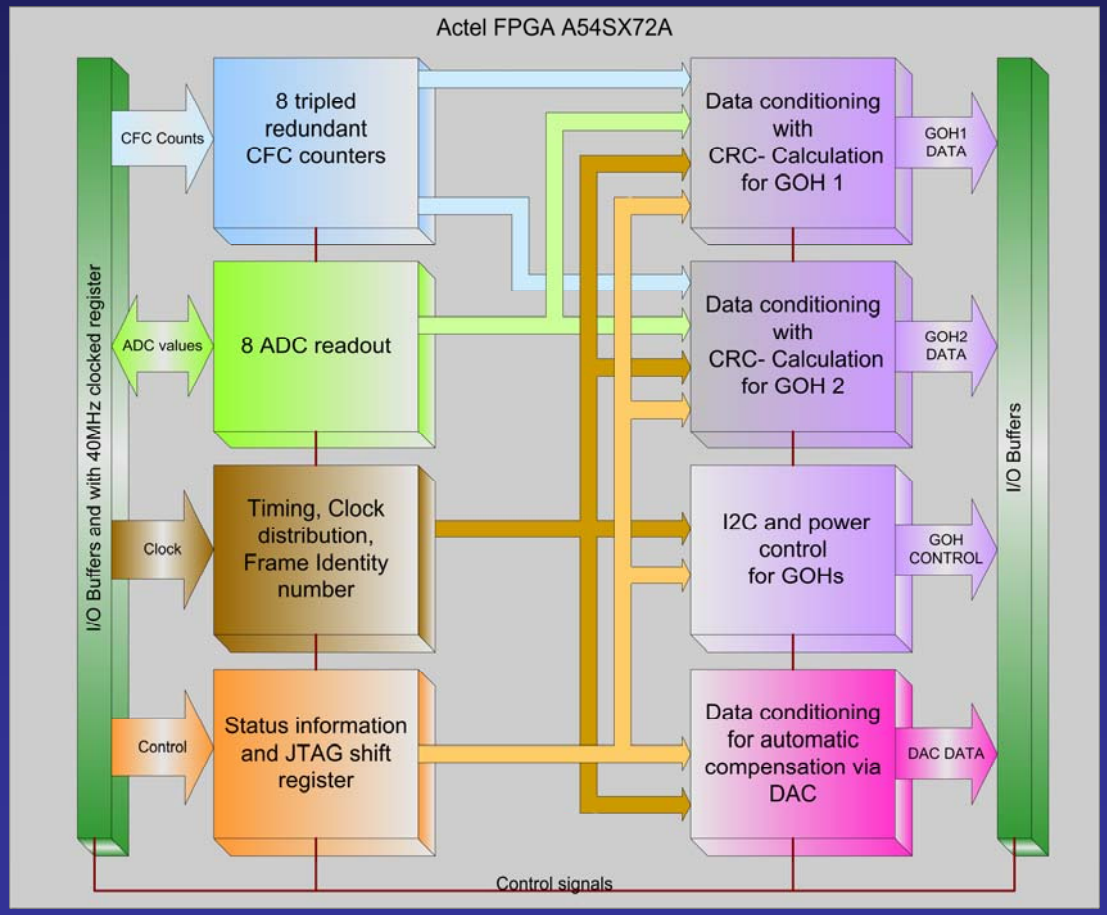
- Irradiation of single components (JFET, OP, Comparator, One shot, …)
- Insertion of fast protection diodes, high voltage capacitors, and leaded resistors on the input
- ADC added to decrease response time / increase dynamic range
- Automatic feedback loop with DAC to compensate leakage current due to integrated dose

The acquisitions card



- 8 current inputs (CFC)
- ADC AD41240 CERN ASIC
- LM4140 voltage reference
- FPGA for data combination
- Two redundant GOH from CMS (including CERN ASIC)
- Line driver CRT910 CERN ASIC
- DAC AD5346

FPGA functional description



- Actel antifuse FPGA A54SX72A
- 4024 sequential cells
- 2012 combinational cells
- Total logic usage: 85%
- Pin usage: 100%
- 40 MHz clock

Tests during operation

- Constant 10pA offset current
  - Check on channel availability
  - In case of exceeding limits, a beam dump can be generated
- Continuous status monitoring
  - Monitoring of voltage supplies and other status information
  - Should failure occur, a beam dump can be generated

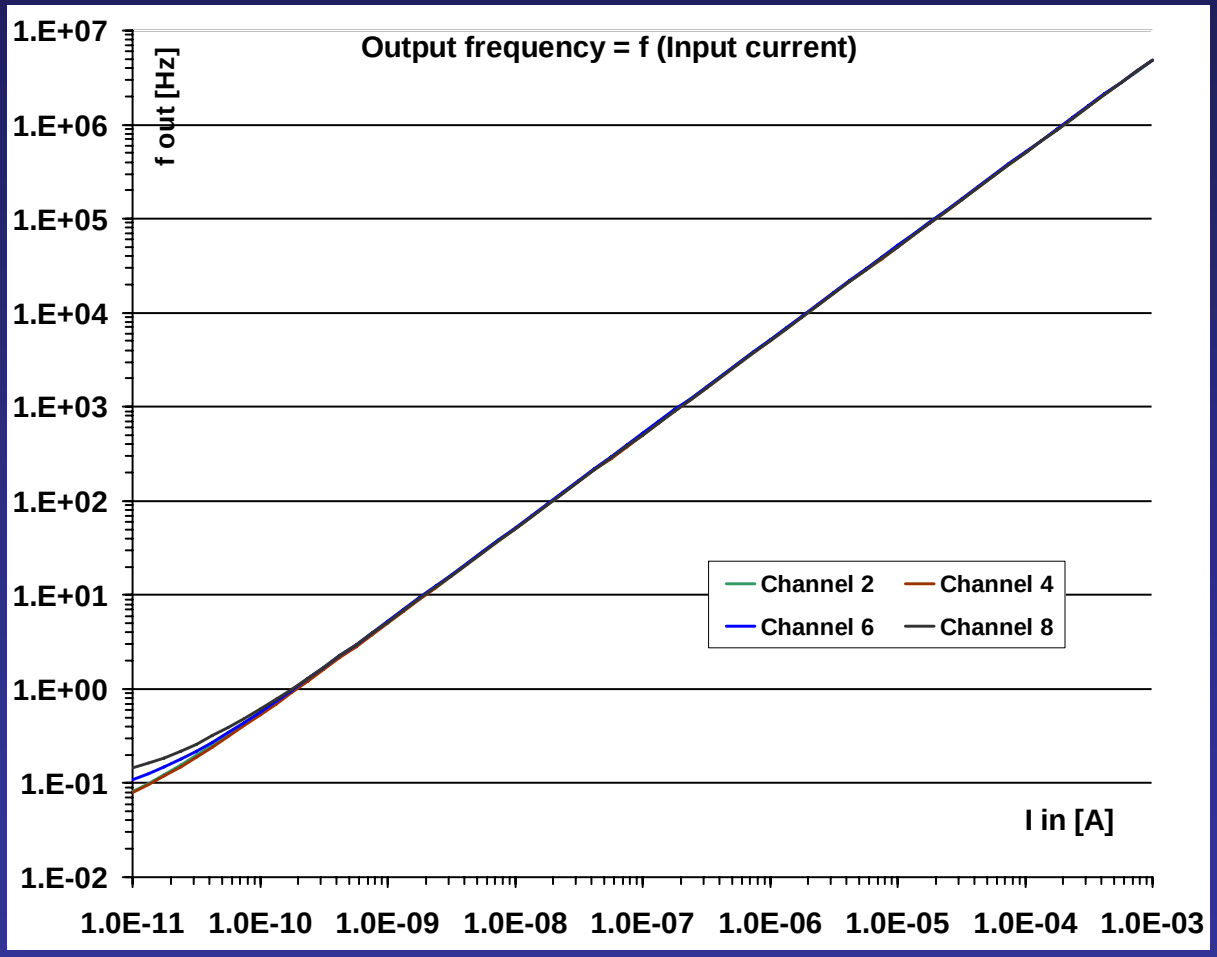
Tests during operation

- Continuous check during data transmission
  - Checked at each transmission
    * Card identity number check
    * Frame identity number check
    * Cycle redundancy check
  - Should failure occur, a beam dump can be generated

Tests during operation

- High Voltage (HV) activation test
  - 100pA added, dynamic test
  - Degradation of electronic can be detected
  - In case limits are exceeded, no beam permission given
  - To be carried out before each beam fill
- HV modulation test
  - Capacitive current injection via chamber electrodes
  - Degradation of complete chain can be detected
  - In case limits are exceeded, no beam permission given
  - To be carried out before each beam fill

Measurement results



CFC input circuit

- Dynamic range over 8 decades from 1mA to 10pA
- Down to 1nA max error of 6.5%
- Down to 10pA max error of 96%

Conclusion

- Error
  - +/-25% down to 1nA
  - +100%/-50% down to 10pA
  - improvement possible with accurate calibration

  Radiation tolerance of 500Gy
  - 74HCT123 (one shot), malfunction at 300 to 350Gy components recovered when not irradiated
  - 54SX72A (FPGA), malfunction at 480 to 790Gy, no SEU detected up to 1x 10^{12} p/cm^2
  - All other components were working up to 1500Gy
- Input over current and voltage protection
  - completely fulfilled

Conclusion

- Survey and test features
  - All features working correctly
- Optical link
  - Radiation tolerant design
  - Installed test system at HERA, no CRC error occurred for several months
- Extra system test
  - Temperature test: 0 – 70°C passed
  - Magnetic field test: 1000Gauss passed, performed for CMS

Acknowledgment

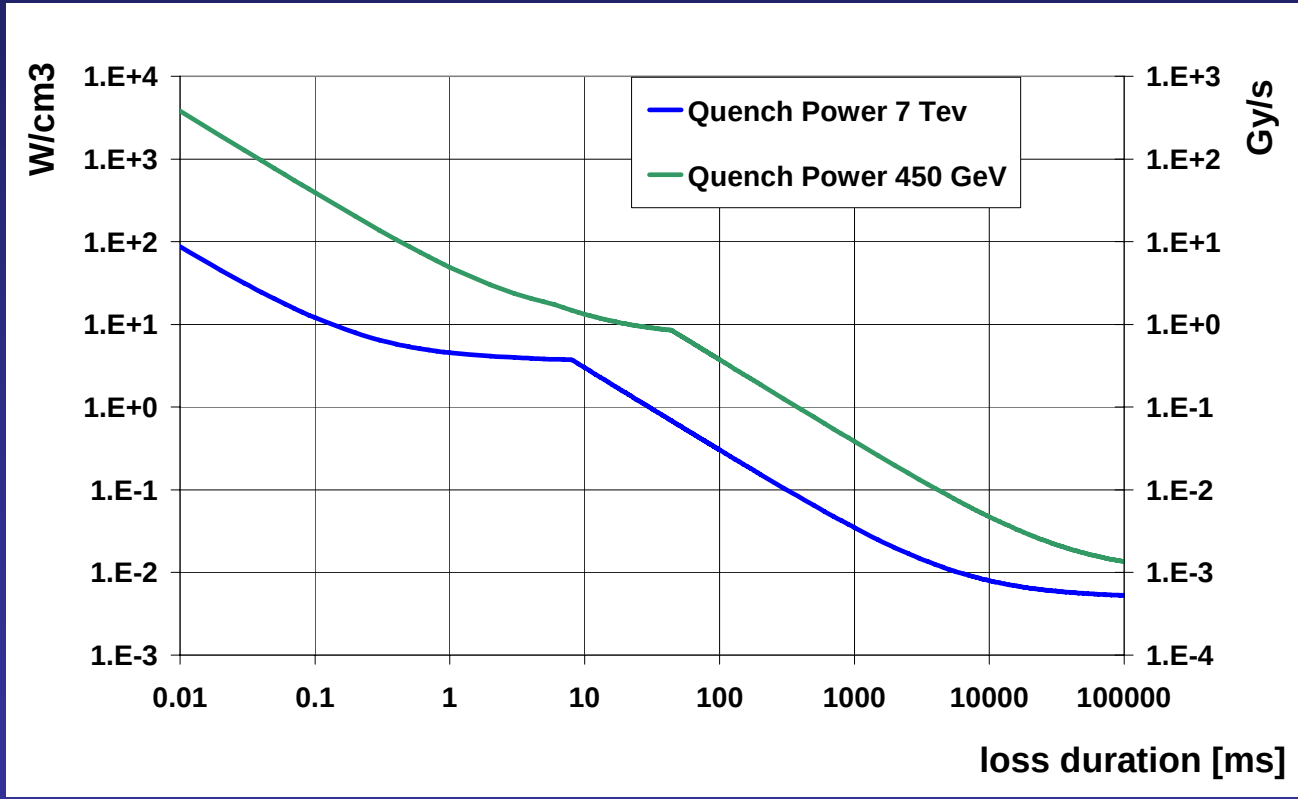
- I would like to thank
  - K. Kloukinas, P. Moreira, A. Marchioro for providing help with the ASICs from PH/MIC
  - A. Singovski, F. Vasey, R.Rusack for providing help with GOH from CMS
  - The beam loss section

- Further information can be found:
  - The LHC Beam Loss Monitoring System's Surface Building Installation (Poster/Paper LECC 2006 from C. Zamantzas)
  - Functional and linearity test system for the LHC beam loss data acquisition card (Poster/Paper LECC 2006 from J. Emery)
  - http://www.cern.ch/BLM

Appendix

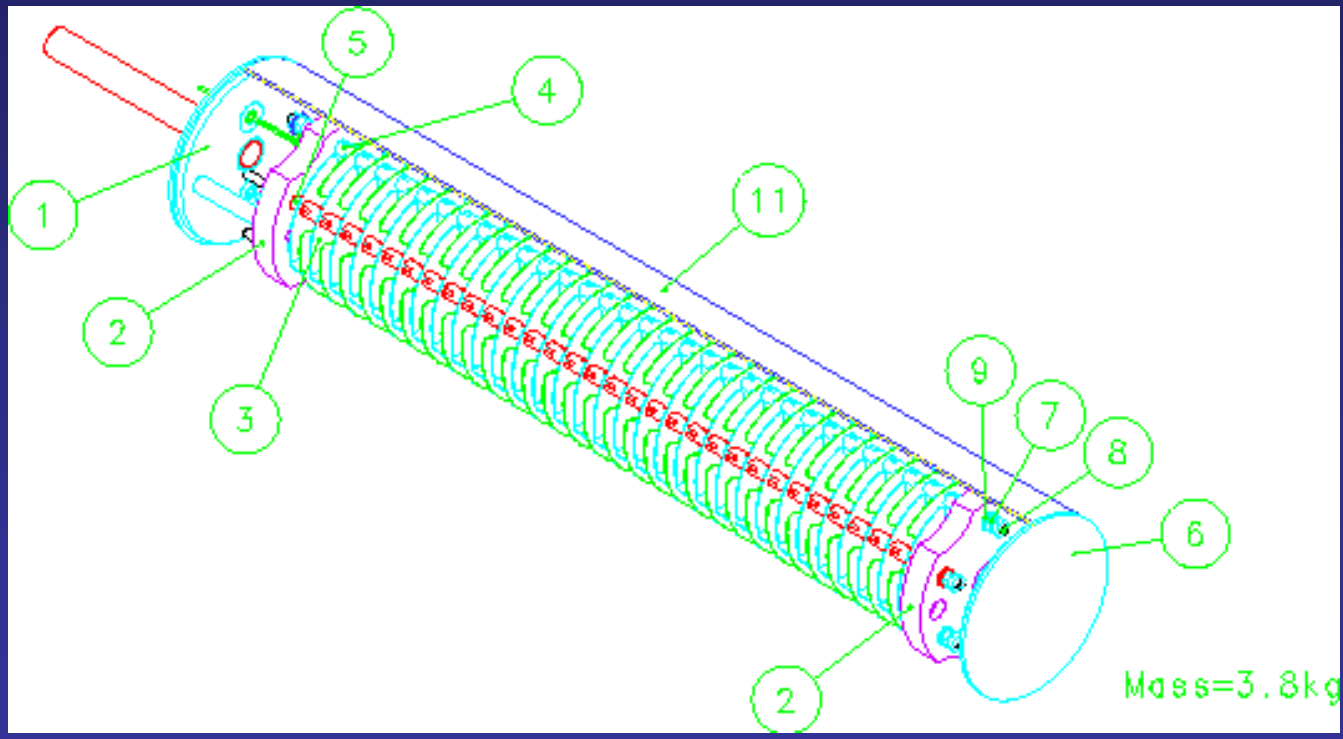
Appendix

- Magnet quench levels

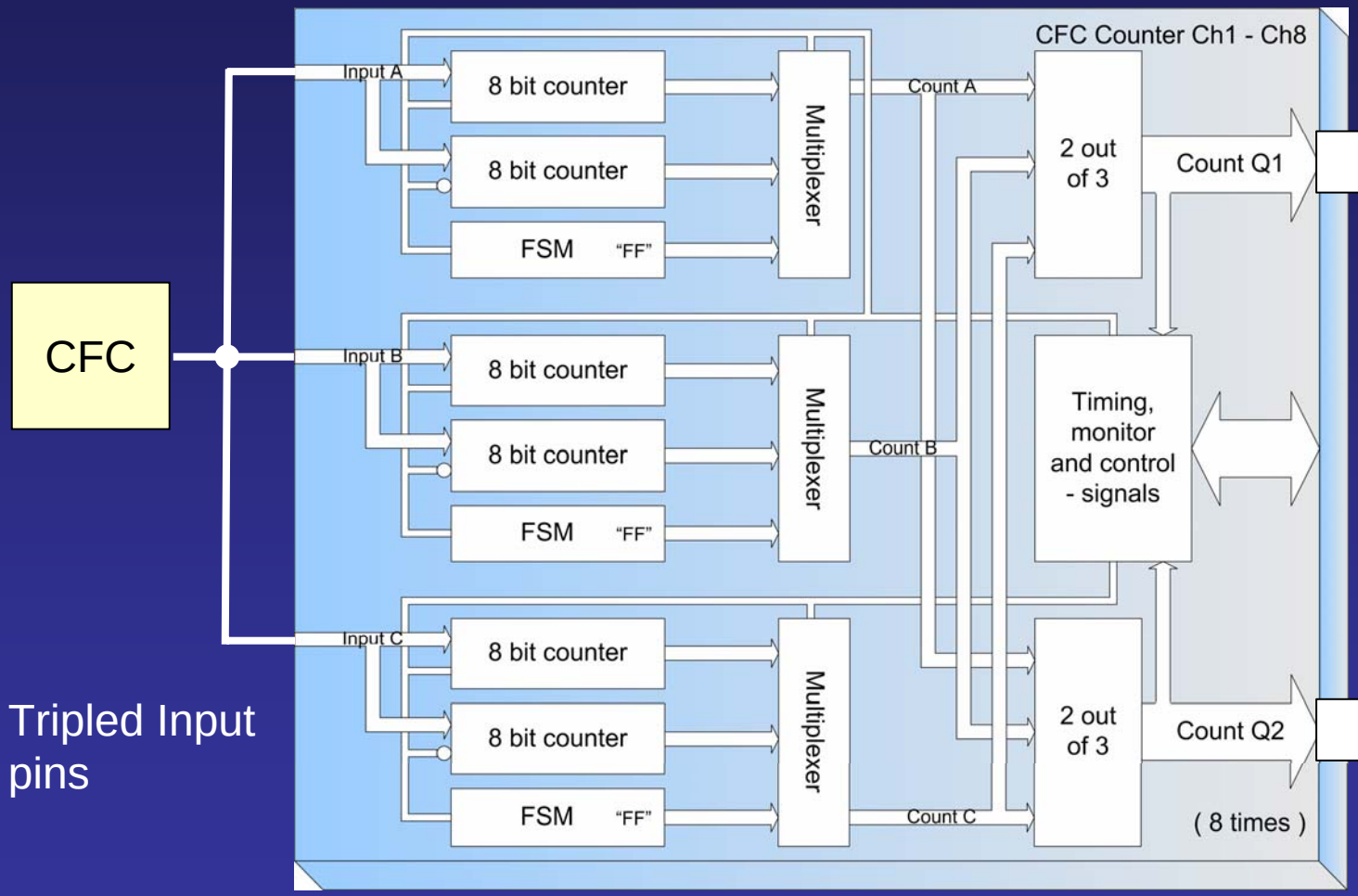


Appendix

- Ionization chamber

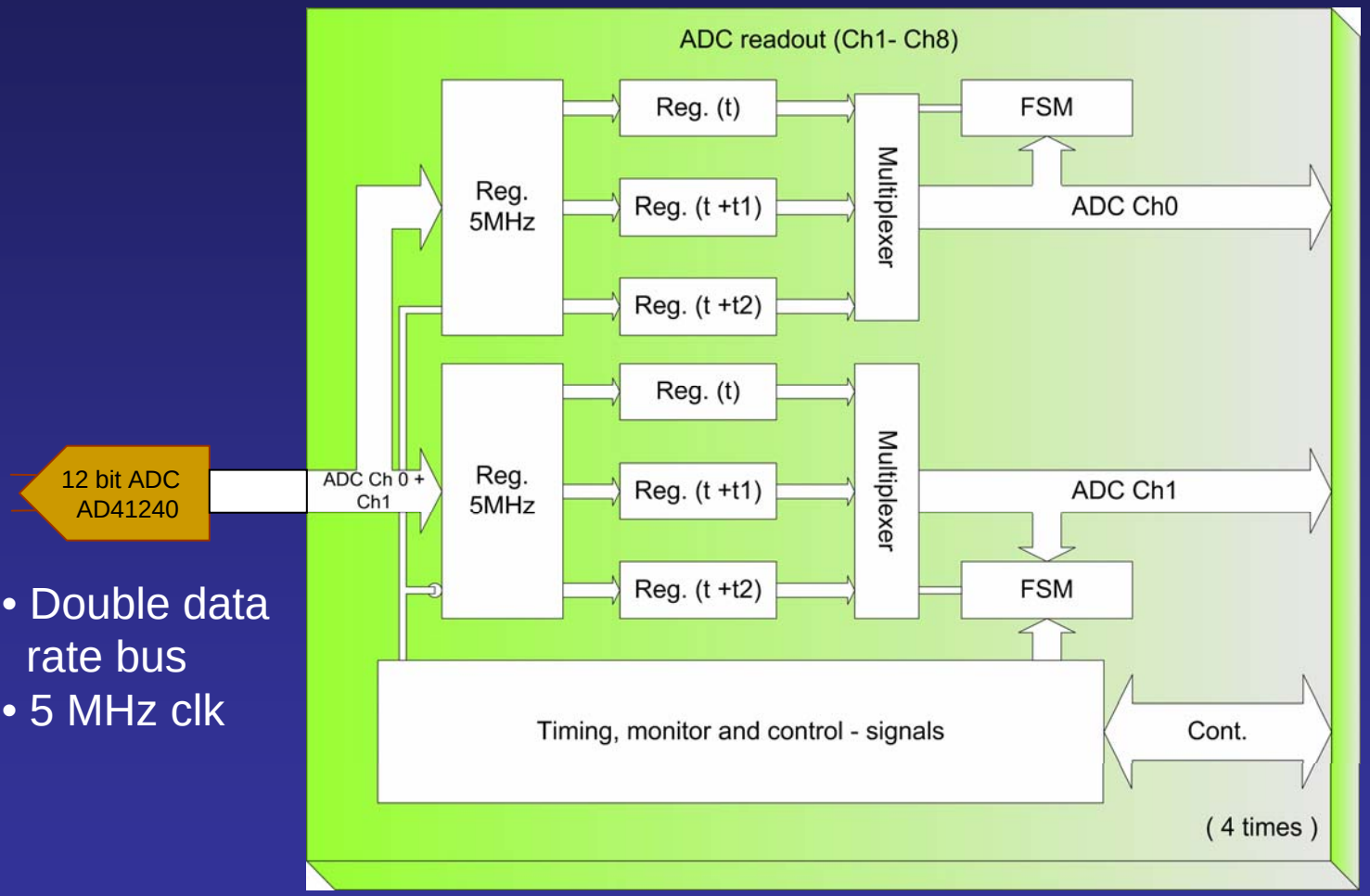


FPGA functional description



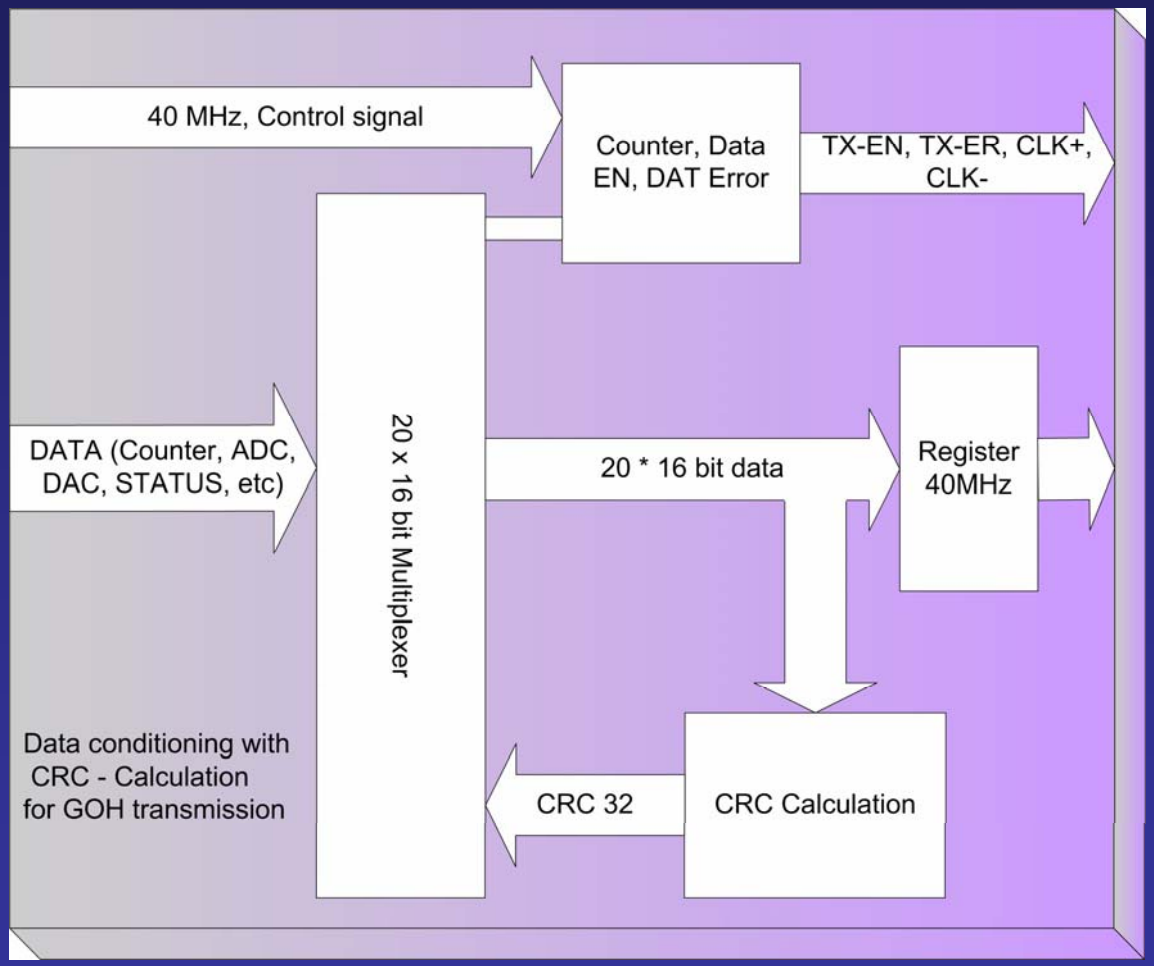
- Tripled redundant logic
- 2 x 2 out of 3 voter connected to two GOHs

FPGA functional description

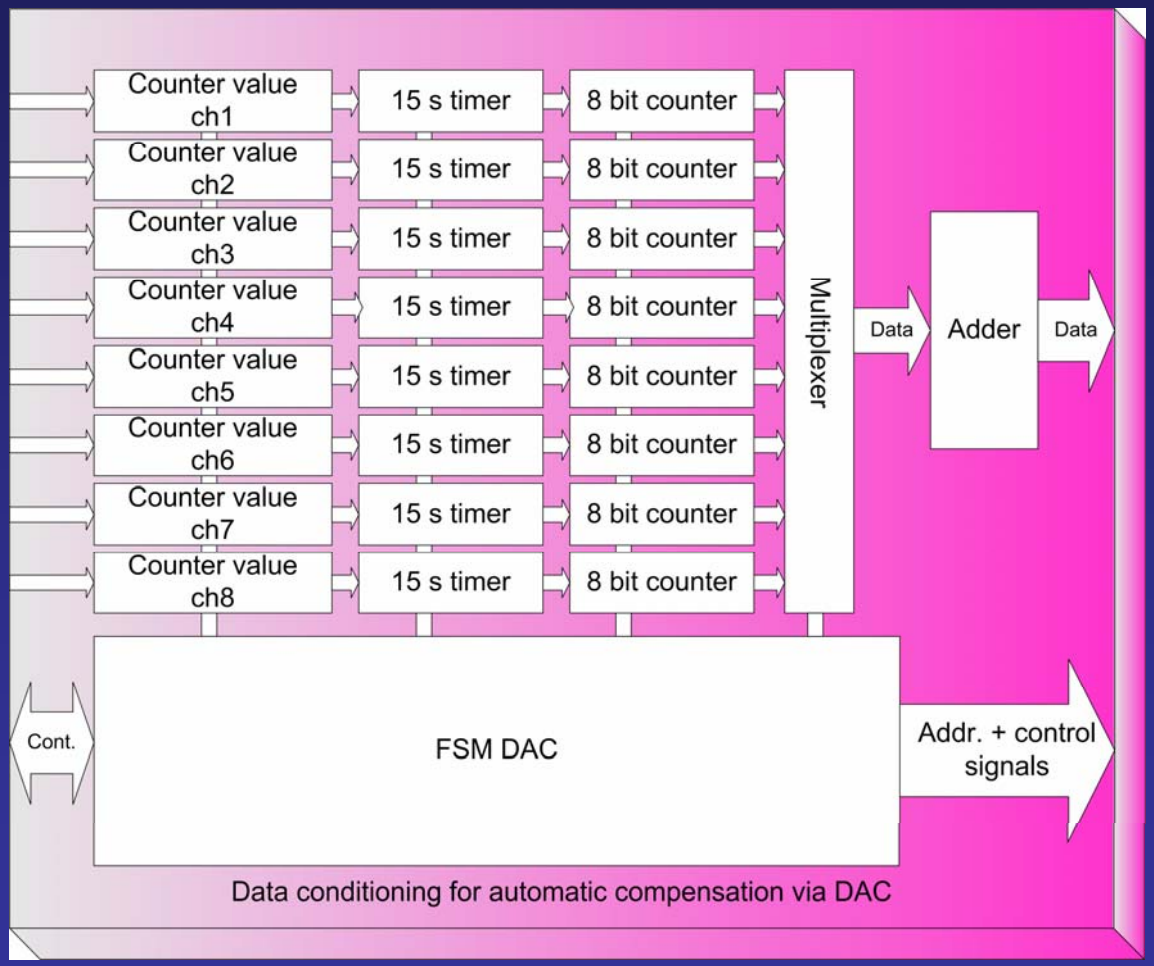


- Double data rate bus
- 5 MHz clk

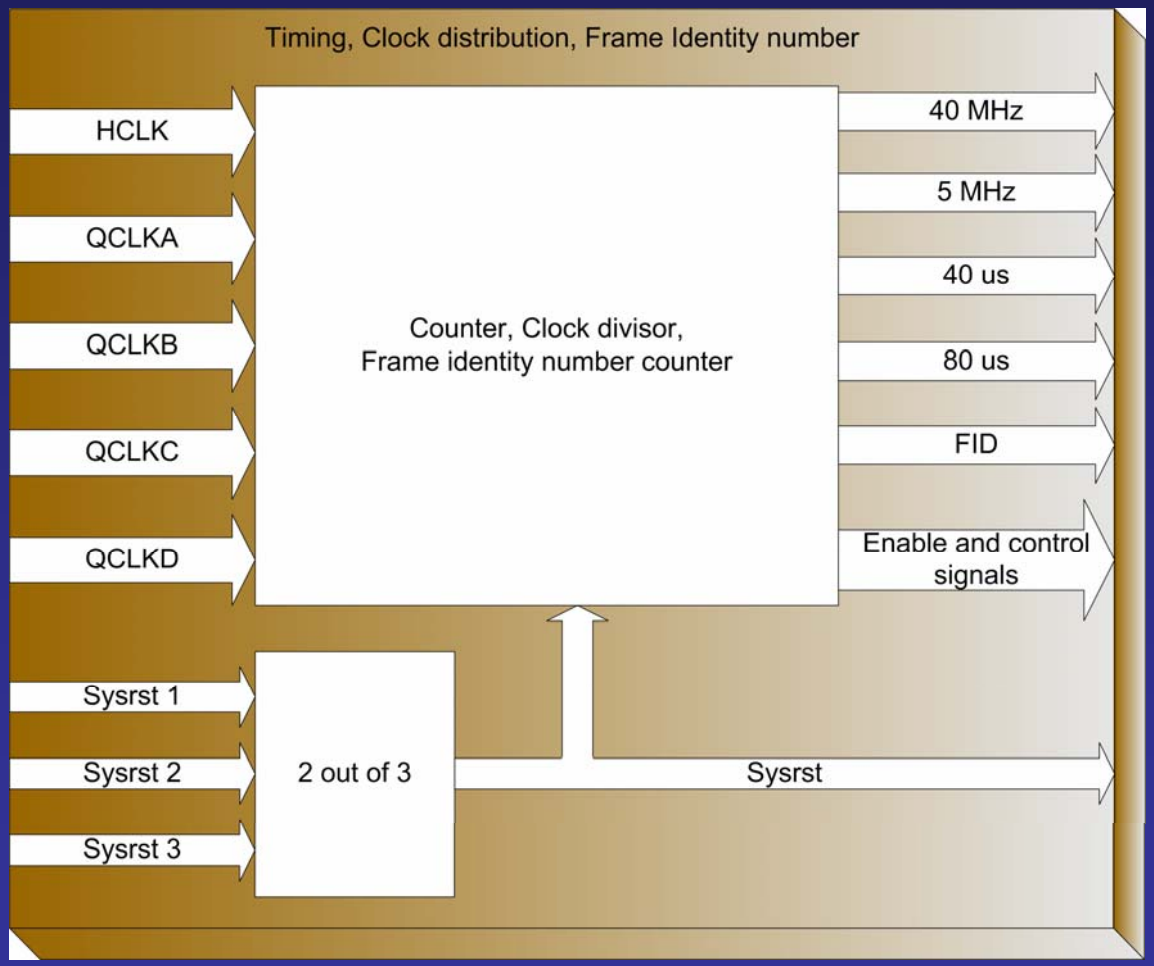
FPGA functional description



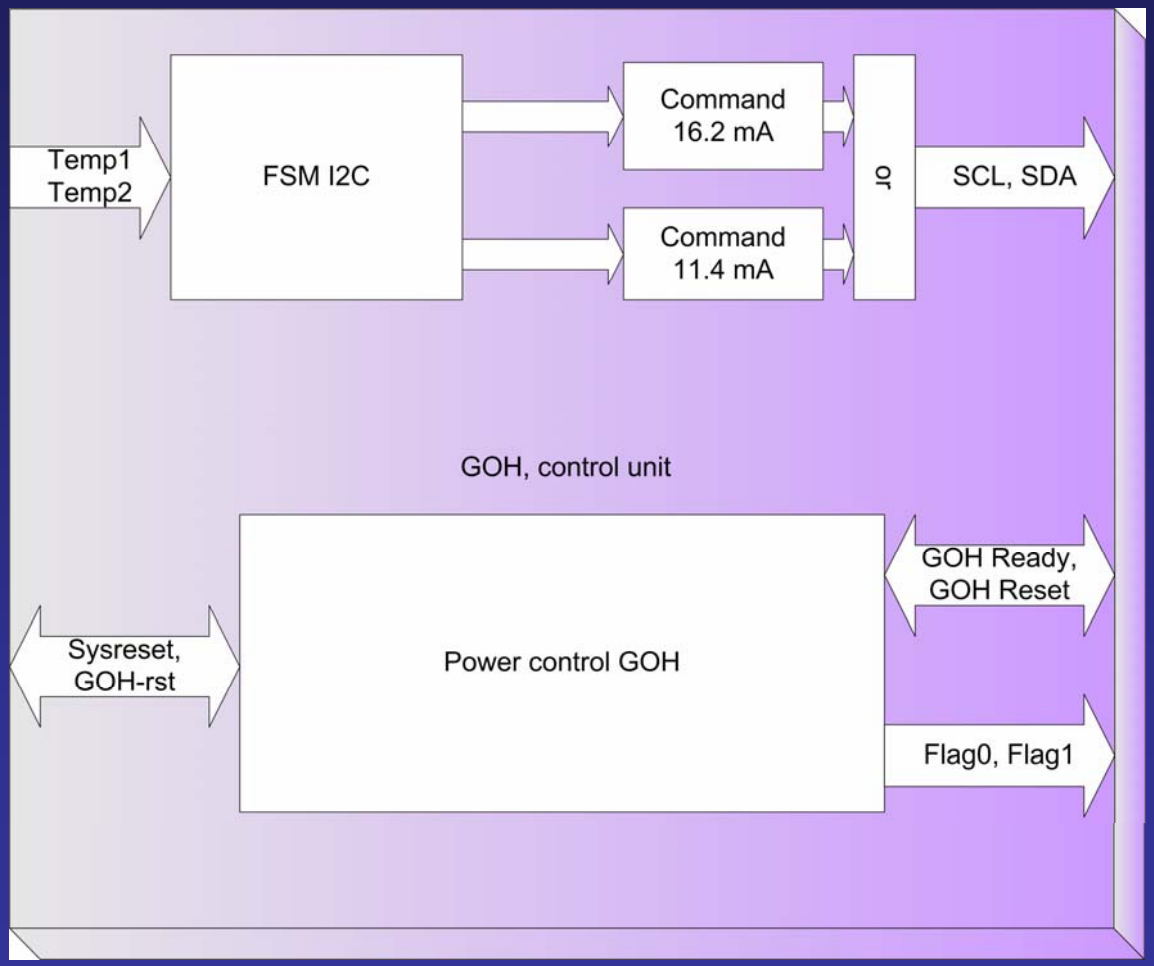
FPGA functional description



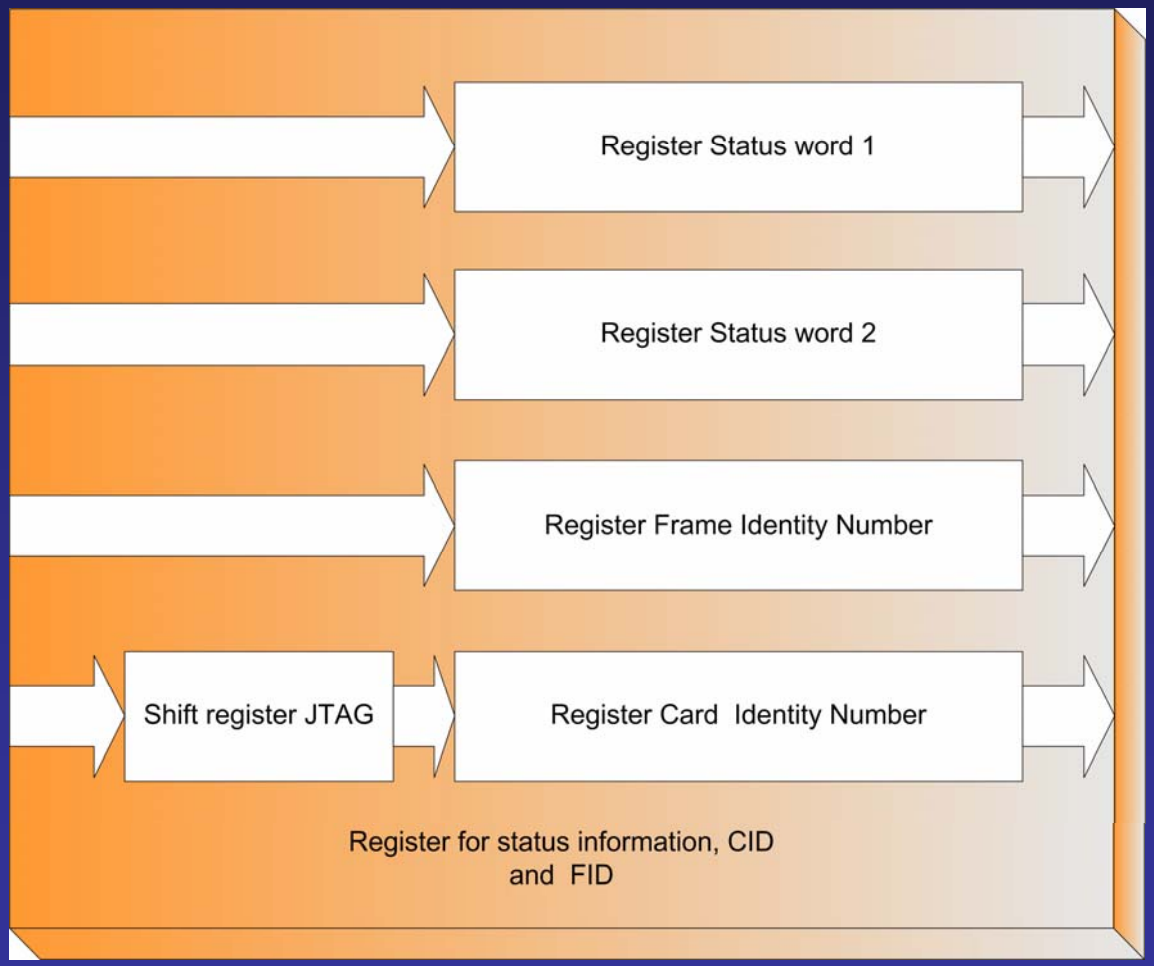
Functional description of FPGA



Functional description of FPGA



FPGA functional description



FPGA functional description

CID (card identity number)	
STATUS 1	
STATUS 2 (Level 1-8, CFC-ERR 1-8)	
Count 1	ADC 1
ADC 1	Count 2 / ADC 2
ADC 2	Count 3
ADC 3	Count 4
Count 4	ADC 4
Count 5	ADC 5
ADC 5	Count 6 / ADC 6
ADC 6	Count 7
ADC 7	Count 8
Count 8	ADC8
FID (frame identity number)	
DAC1	DAC2
DAC3	DAC4
DAC5	DAC6
DAC7	DAC8
CRC	
CRC	

FPGA functional description