Preamplifier-shaper prototype for the Fast Transition Detector of the Compressed Baryonic Matter (CBM) experiment at FAIR

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Abstract

In this work a preamplifier-shaper prototype for the Fast Transition Detector of the Compressed Baryonic Matter (CBM) experiment at FAIR fabricated using a 0.35 μm CMOS technology will be presented. The ASIC integrates 16 identical Charge Sensitive Amplifiers (CSA) followed by a Pole-Zero network, two bridged-T filters, Common-Mode FeedBack (CMFB) network and two non-inverting level shifting stages. The circuit is optimized for a detector capacitance C_d of (5-10)pF. Measurement results confirm the noise of 330 e^- + 12 e^-/pF obtained in simulations for a pulse with a Full Width Half Maximum (FWHM) of 71 ns. The circuit recovers to the baseline within 200 ns. The conversion gain is 12.64 mV/fC. An integral nonlinearity of 0.7% is also achieved. The maximum output swing is 2 V. The power consumption is 16 mW/channel where the main contributors are the input transistor and the level shifting stage with 5.3 mW and 6.6 mW, respectively. The total area of the chip is 12 mm^2. Although the circuit was designed for a positive input charge it has in addition the ability of handling negative current pulses of about 85% of the typical charge of 165 fC without any degradation of the signal. The chip was submitted for manufacturing in AMS's C35B4M3 0.35 micron CMOS technology in October 2005. This circuit has been successfully used in the CBM test-beam at GSI Darmstadt in February 2006.

I. Introduction

The CBM experiment is a dedicated fix target heavy-ion experiment for the future accelerator Facility for Antiproton and Ion Research (FAIR). The major experimental challenges are posed by the extremely high reactions rates of up to 10^7 events/s. These conditions require unprecedented detector performance concerning speed and radiation hardness. The high reactions rates require electronics with fast shaping time. A Fast Transition Radiation detector will be part of the CBM experiment. A sketch of the proposed CBM experiment is shown in Figure I.. The setup will measure both hadron and electrons with large acceptance up to beam energies of about 40 GeV/u following a new concept [1].

In the field of radiation detectors a fundamental role is played by the analogue front-end, which is responsible for the signals generated by the detector to the digitization circuitry and for optimizing the signal to noise ratio. In many cases the measured quantity is the energy deposited by each ionizing particle or photon. This is usually accomplished by measuring the amplitude of the electrical pulses generated by the detector. After a first low-noise preamplifier a second stage is needed to filter as much noise as possible while preserving the useful information. This function, along with an additional amplification, is accomplished by the shaping amplifier. A unipolar filter is needed for an optimum measurement of the pulse amplitude that carries the information of the incident energy.

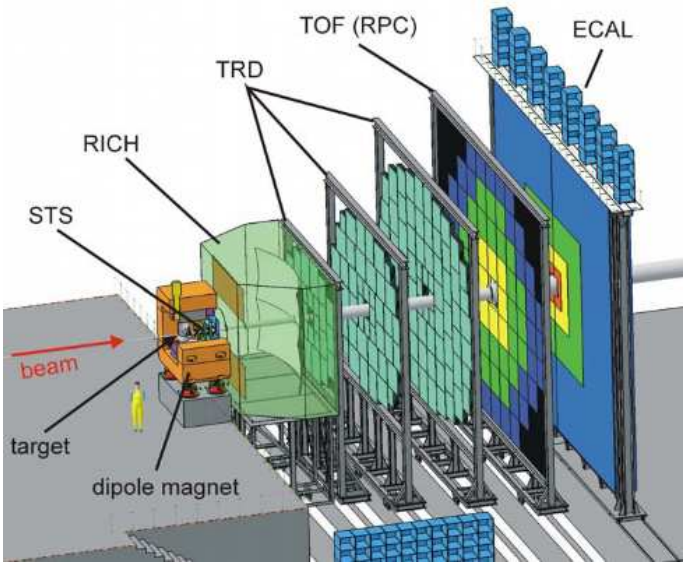

Figure 1: Sketch of the proposed experimental setup for the CBM experiment. The beam enters from the left hand side. The Fast TRD detector is shown as the light blue part.

II. CBM Preamplifier-shaper overview

A block diagram of the preamplifier-shaper chain is shown in Figure II.. Each channel of the 16-channel version consist of a preamplifier, a Pole-Zero network, two bridged-T filters, two non-inverting amplifiers, a CMFB network and a self-adaptive bias network.

The principal parameters in the design were Equivalent Noise Charge (ENC), Full Width Half Maximum (FWHM), Integral Non-Linearity (INL) and conversion gain (Table 1).

This topology has successfully and extensively been used in other applications like the ALICE TPC [2] and the ALICE TRD [3]. Each of the parts of the circuit is briefly explained in sections III, IV and V. The simulated and measured results are presented in sections VI, VII and VIII.

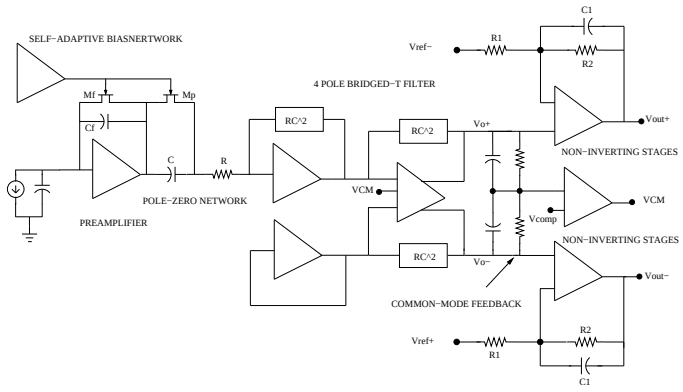

Figure 2: Block diagram of the preamplifier-shaper chain of the realized ASIC. All parts, the preamplifier, the Pole-Zero network, two bridged-T filters, two non-inverting amplifiers, the CMFB network and the self-adaptive biasnetwork are shown.

III. The preamplifier and the Pole-Zero network

Since the required FWHM of the preamplifier shaper circuit is 70 ns, a NMOS transistor is preferred at the input due to higher transconductance (gm) and to the lower white noise compared to a PMOS transistor at the same current. The chosen architecture for the preamplifier is the well known folded cascode CMOS circuitry shown in Figure III.. The input is optimized for a detector capacitance of about (5-10) pF. This gives for the input transistor a width over length ratio (W/L) of 800/0.35 and a drain current of 1.85 mA.

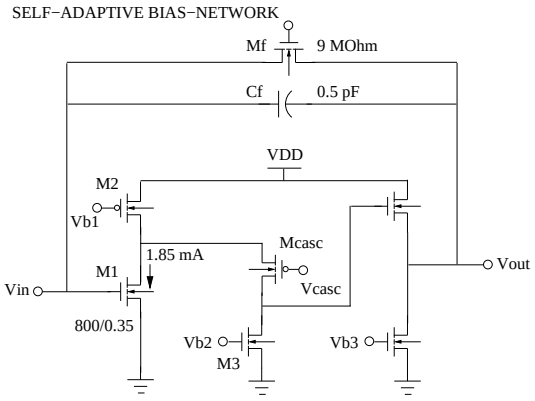

Figure 3: Block diagram of the preamplifier Folded cascode CMOS circuitry

This part has in addition an active feedback network consisting of a capacitor Cf (0.5 pF) and large feedback transistor Rf in the area of 9 MΩ to reduce the parallel noise contribution. The time constant for the feedback network was chosen as a trade-off between noise and ballistic deficit. This relatively long time constant given by the feedback network RfCf, has the disadvantage that the CSA produces a very long tail at the output due to the long discharge time. This long discharge time, relative to the short rise time, makes this topology inefficient for high count rate application due to its sensitivity for pile-up. Therefore a high-pass filter consisting of the CR part FigureII. is included to reduce the length of the tail. The reduction the tail (low frequency part) and the following quick return to base-line ($<$ 200 ns) increases the circuits capability to process events with high occupancy.

Also the implementation of the 9 MΩ integrated resistance could be a problem due to the large area occupied. A resistance of this size is only doable if a MOSFET biased in the triode region is used. The use of the MOSFET as a replacement for the feedback resistor has also the advantage that it reduces the parasitic capacitances associated with the large resistor. To bias the feedback transistor Mf the well known self-adaptive bias network is used. The chosen self-adaptive biasing scheme with non-linear pole-zero cancellation allows us to use a MOS device operated in triode region as the DC feedback element while eliminating non-linearity and sensitivity to supply, to temperature and to process variation. The circuit is continuously sensitive and requires no external adjustment to set the feedback resistance. This part of the circuit is designed following the design procedure given in [4]. This is normally realized as a copy of the CSA, but in our case we use a scaled version. We do not see any visible effect in doing so, confirming previous experience where the same scaling strategy has been used.

The presence of large input signals increases the drain-source voltage of this feedback transistor, which in turn decreases the feedback resistance. This feature has the advantage that the time constant of the feedback network reduces, and as a consequence the probability for pile-up with large pulses will also decrease.

To reduce any possible crosstalk between channels, each channel has its own independent self adaptive bias-network.

IV. Shapers

In order to decrease the rise and the fall time of the produced pulses, to meet the gain specifications, and to reduce the noise through the bandwidth reduction of the filters, the CSA and the P-Z network are followed by two bridged-T filter stages that give in total a CR-RC4 semi-Gaussian shape as seen in Figure 4. The first shaper must fulfill the following requirements, keep the Vgs relative to ground equal to the Vgs of the CSA for process, temperature and supply voltage variation, in addition to amplification and bandwidth limitation. To preserve a perfect Pole-Zero cancellation one of the requirements is that the first shaper input transistor has the same Vgs relative to ground as the CSA. This is best done by choosing the same topology as the CSA. A scaled version of the preamplifier is here used to save power and area. This will not influence the quality of the Pole-Zero cancellation as seen in Figure 4 and Figure 5 for simulation and measurement results, respectively. The pulse return smoothly to the baseline without any undershoot in about 200 ns.

The second shaper is built around a fully differential folded cascode amplifier that converts the signal from a single ended output signal to a differential output signal. To hold the common-mode voltage of the differential output at a known

voltage Vcomp, a CMFB circuit is used to sense the average of the amplifier output Vo+ and Vo-. The output of the CMFB network is VCM. The average of the Vo+ and Vo- is generated with the help of the resistor/capacitor combination applied at the input of the CMFB network. This voltage is compared with an equally and externally given voltage (Vcomp). These two voltages are then compared, and the output of the CMFB circuit is then fed back through the VCM to adjust any deviation from the externally given Vcomp. These scheme ensures fully balanced outputs [5] over a voltage range limited by the CMR of the two non-inverting amplifiers and the source follower output of the second shaper. The combination of these two filters gives a very good semi-Gaussian pulse with a peaking time of 70 ns from 0 - 100% of the maximum pulse amplitude. Due to the symmetry of the fully differential folded cascode topology, the different polarities of the signal will be handled equally around the common mode voltage. This part of the topology together with the part described in the following section is therefore optimal for a dual polarity detector.

V. The non-inverting output stages

After the signal is shaped and optimized for noise, the differential output signal from the differential amplifier is split in two around the common-mode voltage, in this case 1V, in order to increase the maximum output swing. The output DC-level is set by Vref+ (1.5V) and Vref- (0.5V), giving a DC level at the output of 0.5V (Vout+) and 1.5V (Vout-), respectively. The amplifier used here is a Miller CMOS OTA. The two equally designed amplifiers are then used in an non-inverting topology (Figure II.), each with a closed loop gain of 2. The proposed topology can easily be adjusted to adapt to both polarities by interchanging the two reference voltages Vref+ and Vref-. This allows a symmetrical system so that the CBM CSA chip will have nearly identical response to both the negative and positive input signal, only limited by the cut-off region of the feedback transistor Mf and the cut-off region of the output stage of the first shaper. The circuit has been proven to handle a negative input charge of 140 fC without any visible degradation of the signal or of the specifications. With this topology the user can change the DC level as wanted, and to some degree decrease the gain of this stage by adding externally a resistor with appropriate value in series with R1 in Figure II.. This will, of course, also change the output DC and must be compensated for by increasing/decreasing the reference levels.

VI. Transient analysis

A simulated pulse response for a delta input charge of 165 fC with a detector capacitance of 5 pF is shown in Figure 4. The pulse response shown here, has a FWHM of 71 ns, a conversion gain of 12.6 mV/fC, a simulated noise of 350 e^-, a return to base-line after 200 ns and no undershoot. Therefore, we can conclude at this stage that the circuit fulfills all the requirements (Table 1) from the simulation point of view.

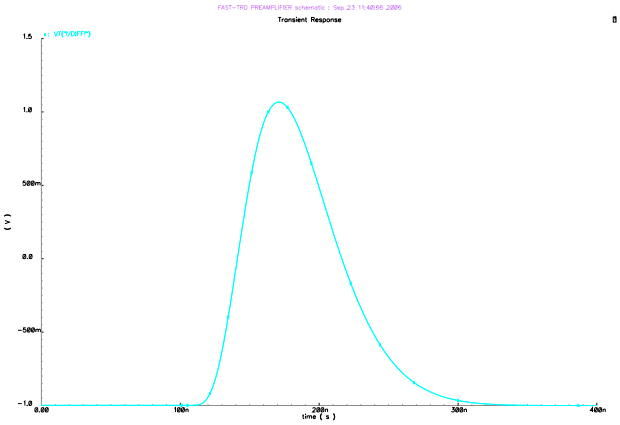

Figure 4: A typical simulated pulse response of the circuit for a delta input charge of 165 fC with a 5 pF detector capacitance.

VII. Measured characteristics of the circuit

The first prototype preamplifier shaper for the Fast TRD at CBM has been tested. The circuit has been realized in AMS's C35B4M3 0.35 um CMOS process.

Parameters	Specifications	Simulated (typ.)	Measured
Equivalent Noise Charge	1000 e^- C_d 5-10pF	350 e^-@5pF 412 e^-@10pF	387 e^-@5pF 446 e^-@10pF
Conversion Gain	12mV/fC	12.6 mV/fC	12.64 mV/fC
FWHM	70ns	71 ns@5pF	71 ns@5pF
Undershoot		1mV	-
Baseline shift		3mV	-
INL	$< 1\%$	$<0.45\%$	0.7%

Table 1: Main requirements given for the preamplifier shaper design. Simulated and measured values are also given.

The total power consumption of the circuit is 256 mW for 3.3 V power supply. The ASIC consist of 16 channels, so this gives a power consumption of 16 mW/channel. The circuit has a typical output range of 2 V.

The circuit was tested for ENC, conversion gain, INL and FWHM.

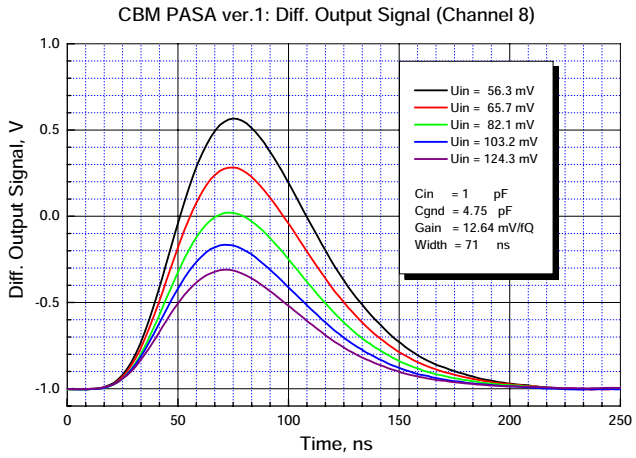

Figure 5: Measured pulse response with a typical load of about 5 pF for several different input charges.

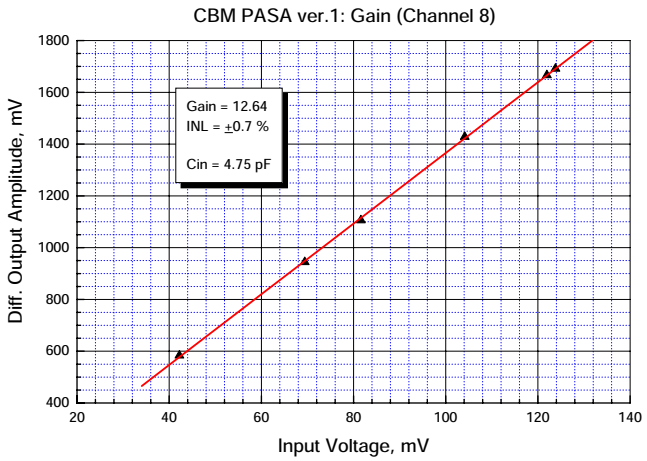

Figure 6: Measured conversion gain and integral non-linearity as a function of input charge.

The pulse response was measured with a typical detector capacitance of 5 pF, with an input signal ranging from 56 mV (56 fC) to 124 mV (124 fC) through an injection capacitance of 1 pF. The measured result (Figure 5), gives an FWHM of 71 ns, showing a superior agreement with the simulated value of 71 ns for the same detector capacitance. An equally good agreement is also observed between the measured conversion gain (12.64 mV/fC) and the simulated one (12.6 mV/fC).

The INL has been measured for input signal from about 40 fC to 125 fC. The overall INL obtained here is 0.7% as seen in Figure 6. This is well below the required INL of 1% and close to the simulated value of 0.45%.

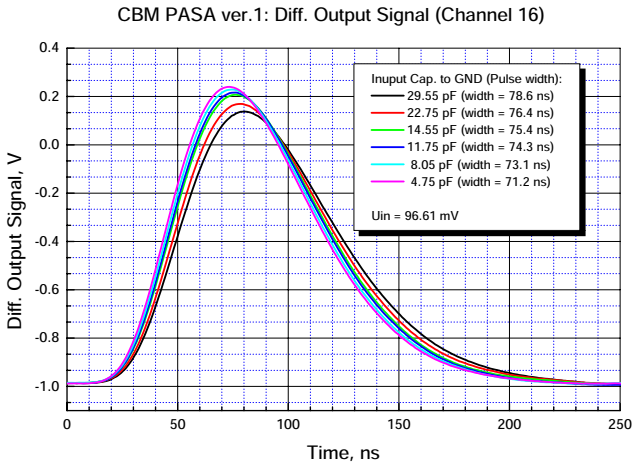

Figure 7: Measured pulse response for different load capacitances.

The measured pulse response for different detector capacitances are shown in Figure 7. The signal shape for both FWHM and conversion gain shows a weak variation with the input capacitance due to the reduction of the bandwidth of the CSA as obtained in simulations. The measured results are shown in Figure 8. The amplitude (conversion gain) decreases when increasing capacitance (Figure 8,bottom) while the width increases (Figure 8,top). The two effects compensate resulting in a constant area (Figure 9).

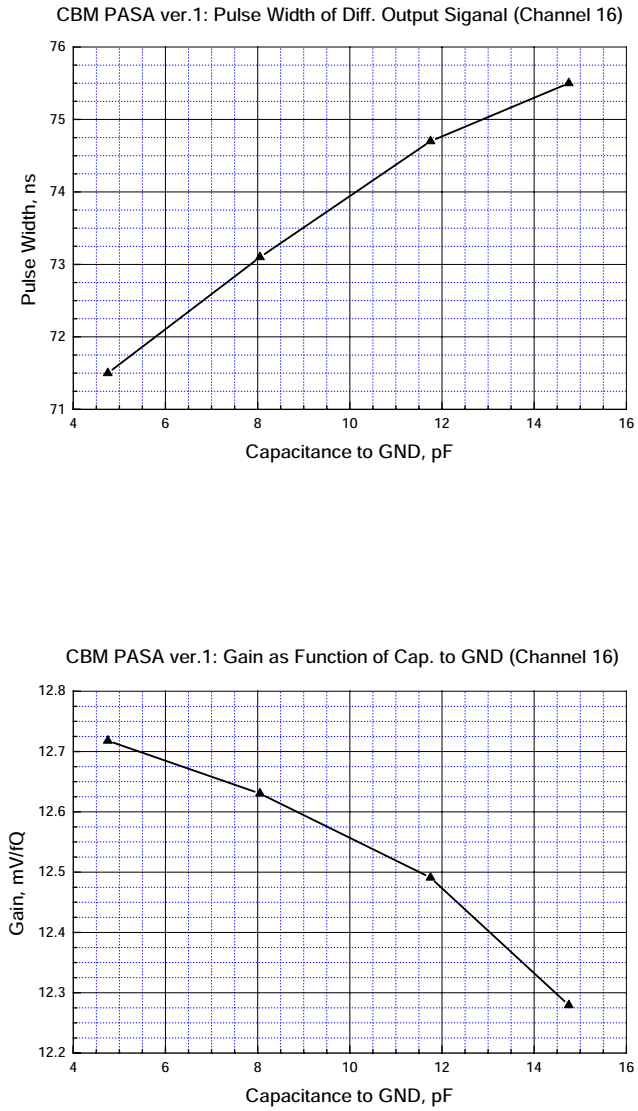

Figure 8: (Top): Measured FWHM of the signal for different load capacitances. (Bottom): Measured conversion gain for different load capacitances.

The ENC measured noise for 5 and 10 pF (detector capacitance working area) is 387e and 446e, respectively (Fig. 10,top). The small offset in noise compared to the simulated results is given by the pick-up as seen in Fig. 10,bottom. This gives a measured noise slope of 11.8e/pF compared to 12.4e/pF simulated. This shows again a very good agreement between simulated and measured values.

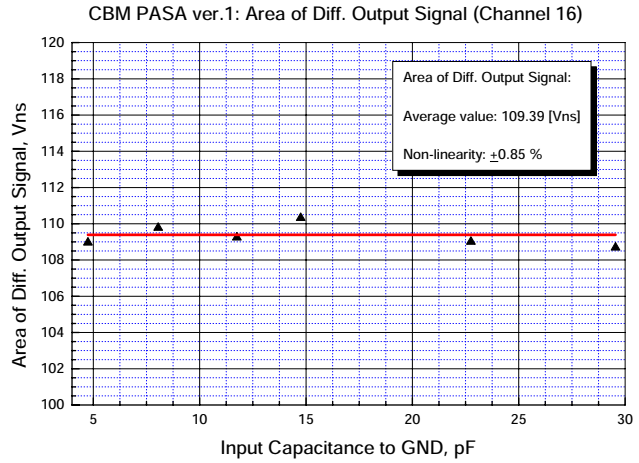

Figure 9: Area of the measured signal for different load capacitances

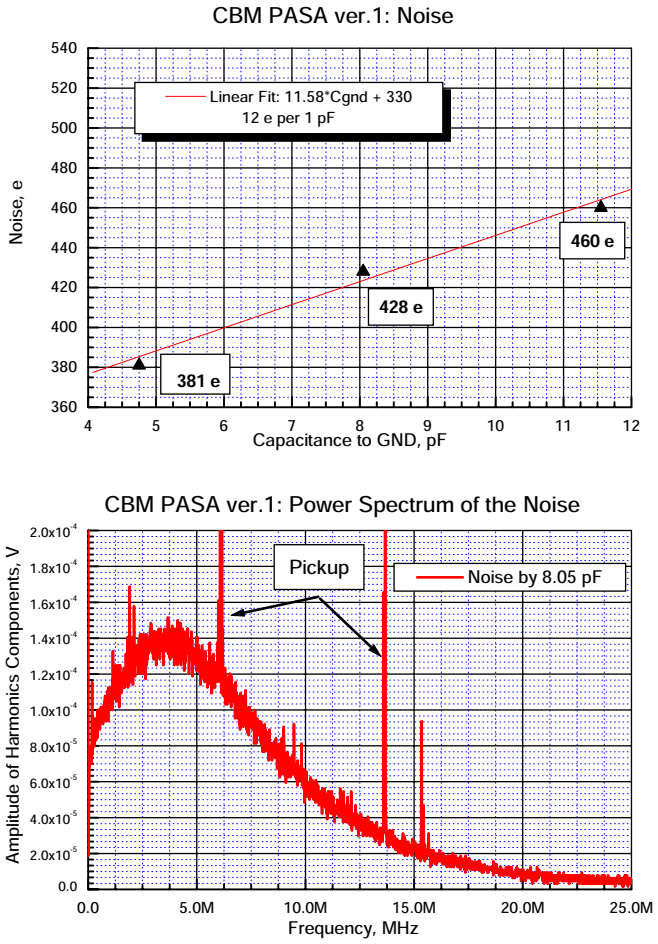

Figure 10: (Top): Measured Equivalent Noise Charge (ENC) for different load capacitance. (Bottom): Measured noise spectrum for a capacitance load of about 8 pF.

VIII. Conclusions

A new low noise multi-channel Application Specific Integrated Circuit (ASIC) has been designed with the AMS's C35B4M3 0.35 um CMOS process for use in CBM test-beam at GSI Darmstadt February 2006. This circuit has successfully been used in that test-beam for both polarities. The ASIC consist of 16 channels, and the total power consumption is 256 mW. The chip is designed to handle a typical input charge of 165 fC. The ASIC is optimized for capacitance in the region of about 10 pF. The total area of the chip is 12 mm^2. In total 15 circuits out of 15 have been measured successfully. The presented circuit fulfilled all requirements. A superior correlation between simulated and measured values has been shown.

IX. Acknowledgments

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