

Functional and linearity test system for the LHC beam loss monitoring data acquisition card

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Abstract

In the frame of the design and development of the beam loss monitoring (*BLM*) system for the Large Hadron Collider (*LHC*) a flexible test system has been developed to qualify and verify during design and production the *BLM LHC* data acquisition card [1]. It permits to test completely the functionalities of the board as well as realizing analog input signal generation to the acquisition card. The system utilize two optical receivers, a Field Programmable Gate Array (*FPGA*), eight flexible current sources and a Universal Serial Bus (*USB*) to link it to a *PC* where a software written in LabWindows/CVI[®] (National Instruments) runs. It includes an important part of the measurement processing developed for the *BLM* [2] [3] in the future *LHC* accelerator. It is called Beam Loss Electronic Current to Frequency Tester (*BLECFT*).

I. HARDWARE

The *BLM LHC* data acquisition card (*BLECF*) also called tunnel card is used to measure the current of the ionization chambers, to digitalize and to send it to the surface through optical fibers. To design, operate and test the tunnel card the *BLECFT* card has been designed. The analog part must be able to handle 8 orders of current settings from 10pA to 1mA and to be able to decode the information sent by optical fiber. The final system includes the card and the power supplies in an easy transportable housing. It is powered by the 230V 50Hz or by a *PC* through the *USB* connections (for the portable version without power supplies).

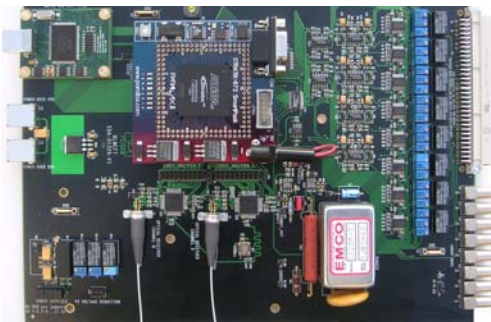


Figure 1: The *BLECFT* card.

The second use of the *BLECFT* is to emulate the processing of the future *LHC* system. For this reason, the choice of a compatible *FPGA* to the *BLM* one was taken to simplify the integration of the hardware description processing. Because this feature was implemented in a small integrated system, the *BLECFT* was often used in proton irradiation campaigns for the design validation of the tunnel card.

A. *FPGA* Description

The programmable logic has a central role on the board. It connects the *USB* module with the rest of the components like the *DAC*, relays and analog switches as well as processes and transmits the measurements and information received from the tunnel card.

The used *FPGA* type on the board belongs to the same family (Altera Stratix[®]) as the one of the *LHC BLM* system but with less logic elements. With this feature, it is possible to reuse code from the *BLMTC* (Running Maxima). The number of channels is reduced from 16 to 8, except this modification the code is identical (to the *BLMTC*). It permits to get similar data as the final *LHC* processing to realize test in real situations.

To implement the different modes, the description take advantage of the parallel processing of programmable logic to allow real time analysis of packets (Running Maxima mode) even during visualization in another mode (Frame Mode). The user can choose the information downloaded into the *PC* by selecting the correct input of the multiplexer corresponding to the mode of operation selected.

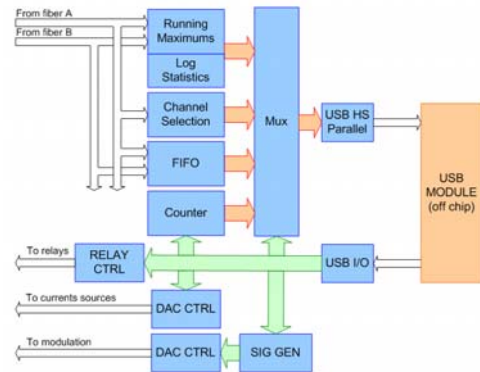


Figure 2: The *FPGA* description blocs.

There are two data channels between the hardware and the *PC*. The control of the *BLECFT* is done through a low speed connexion between the *PC-USB* and the *FPGA*. The I/O are directly controlled by the software to create an 8bits parallel bus where transit addresses of registers (8 bits) and data (16 bits). These data are then parallelized and distributed to all registers. A simple protocol has been specified using these addresses and data to modify the registers values. To get the measurements and status information quickly, the *FPGA* uses a high speed connection with 16 bits parallel bus to the *USB* chip.

The *BLECFT FPGA* includes also logic to control the current sources through *DAC* converters, relays and analog

switches. To reduce the use of output pins on the *FPGA*, the control and data signals are multiplexed. There are two *DACs*, which share their lines. To simplify the logic needed for the control, the update is done continuously between the *FPGA* internal registers and the *DAC*. When the user changes one voltage, the software actually writes in the *FPGA* register the new value. When the refresh process starts, the new setup value will be taken and the *DAC* output voltage updated. With this implementation, the software doesn't have to be specialized for each functionality of the card, it just writes to registers and the *FPGA* does the rest.

There are at least 3 clock domains which have to cohabite together. The speed rate of the data from the tunnel card is 40 MHz, which is synchronised with its own quartz. The second domain is the global clock of the *FPGA* at 40 MHz. The last one is the link to the *USB* module, which runs at 48/33 MHz, because the master of this link is the *USB* mezzanine module. The used bus speed used is 33 MHz to avoid errors due to latency. The clock has to travel from the *USB* to the *FPGA* before the data are updated for the next clock cycle. Even for small connection length, we experienced wrong behaviour using the 48 MHz transmission. In order to separate correctly these clock domains, *FIFOs* are wildly used.

B. Optical link

The optical link consists of two one way fibres connecting the tunnel card to the *BLECFT*. Data packets of twenty words (16 bits) are sent through this 800Mbps single fibre mode link every 40 μ s. The encoding is 8b/10b, which is compatible with the transceiver *TLK1501* from Texas-instruments. The parallel link between this chip and the *FPGA* is a parallel 16 bits bus working at 40MHz. The used components are identical to the one of the BLM receiver card of the *LHC* system.

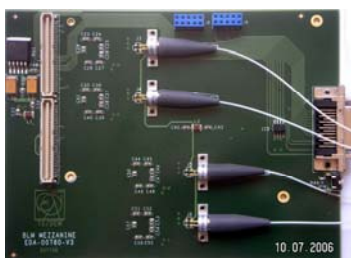


Figure 3: The *LHC BLM* Mezzanine receiver card.

The photodiodes and the transceiver have been directly integrated on the board next to the *FPGA* on the *BLECFT* card. The packets contain card identification number, packet identification number, status of the card, measurements from the *ADC* and counter results of the current to frequency circuit. These data are then processed or send directly to the *PC*.

C. USB module

The use of a *USB* module has been launched by the thesis work of R. Leitner [4] prior to the building of the *BLECFT*. The use of a *USB* transceiver and hardware core inside the *FPGA* has been studied but the effort for adapting a driver under Windows[®] was too high for the purpose of the project.

Another option for the link was given by the use a dedicated chip with embedded handling of the *USB* protocol. The chips from *FTDI* are components specially made to handle the entire link and provide different interfaces (serial or 8 bits parallel) to the user. The *PC* side is handled by a library provided by the company and permits to access the chip by calling some simple functions in this specific library.

The last product tested is a module with the famous Cypress chip *FX2*[®], which is an *USB2* controller and a microcontroller on one chip with high throughput capabilities via a direct data channel path and *FIFO*, bypassing the processor. The module developed by a small company is provided with a custom library to be used with the module. The *USB* protocol is hidden and the user can focus on the functionality of the system.

The choice between these modules has been determined by the transfer speed they can reach (use of *USB 2.0* and 16 bits parallel bus) and by the availability of a complete library of functions. For the *BLECFT*, the last module presented has been used.

D. Current sources

The current source provides currents from 10pA to 1mA on eight channels to feed the inputs of the tunnel card. The central component of this circuit is a Digital to Analog Converter (*DAC*) providing voltages for a resistor network. If the resistor value is high enough compared to the input resistance of the board (worst case: 1M Ω over 2.7k Ω , 0.27%), the error can be neglected. To select the current range, an analog multiplexer permits to choose between the resistor values from 1M Ω to 10G Ω . The variation of the components and systematic errors can be compensated by the calibration (voltage control at the output of the *DAC*) stored into an independent file on the *PC*.

To provide the high currents accurately enough (10 μ A to 1mA), its generation had to be designed separately from the rest with a current sense feedback. The voltage across the control resistors and the second analog switch (to select the range) is measured by a differential circuit, which regulates the voltage on the control resistor in order to reach the needed current (the voltage on the *DAC*).

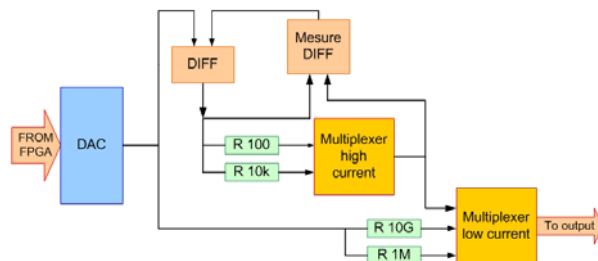


Figure 4: Current source schematic.

E. High voltage module

The *BLECFT* has also the capacity to generate a high voltage to feed one or more ionisation chambers to simulate test procedures. Because of the working voltage (1500V) of these ionisation chambers, there is a need of a specific module capable of generating such high voltage.

One of the tests implemented in the *LHC* system is the modulation of a small portion of the high voltage power supply (*HVPS*) and to check in the Running Maxima if a variation is seen. The hardware and software of the *BLECFT* is available to realize this function. The *FPGA* generate a harmonic signal with a memory based processing, which is added to the base control voltage of the *HVPS* with an analog addition. This voltage is connected to the high voltage power supply module and is multiplied with a factor of 1000. Due to the capacity of the signal electrodes of the ionisation chamber, a small current is induced and measured with the tunnel card. The *BLECFT* process these measurements (Running Maxima) and returns the results to the *PC*. This test will be implemented in the *LHC* system to check the connection of the whole acquisition chain.

II. SOFTWARE

The Windows[®] based application has been developed to provide to the user a graphical environment to configure the hardware and read/store/show measurements in a user friendly way.

The software has been written with a graphical environment called LabWindows/CVI[®] from National Instruments, which provides all graphical facilities and required “C” as programming language. It helps the programmer to focus on functionalities rather than on details.

It includes analysis of raw data coming from the tunnel card as well as result visualisation of the real-time processing done in the *FPGA* similar to the future *LHC* one [3].

A. Event driven coding

The software is event driven and is separated on different files and functions to clarify the code. When the user want to start to read information from the tunnel card, a click on a specific button starts an interrupt with a definite period. Each time the interrupt is called, a function is started, which reads the data from the *USB*, process it in the appropriate way depending on the mode of operation (see II.C) and display it for the user. This style of programming permits to save computer processing power. The program is more often in wait state than in processing state. It is also very easy to add functionalities to the core code without changing timings and initial code.

B. Structure

There are three principal windows composing the software. The first one is dedicated to show and control the way the information from the hardware is handled. The second one contains the options to configure this hardware. The last one is the test window which includes all control and visualisation objects to do the functional test of the tunnel card.

C. Modes of operation

The software has been segmented in 3 modes. 1) The Frame mode catches the raw information directly from the tunnel card, analyzes and displays it as the data are arriving. 2) The running maximum works exactly as the future *LHC* system [3]. The data are processed inside the *FPGA* and the

software takes the results with a user defined period for the display and storage.

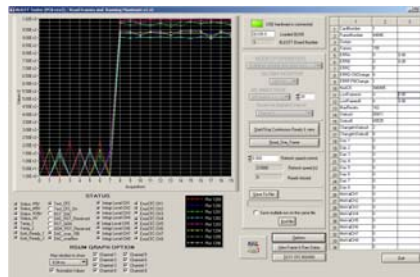


Figure 5: The Running maxima mode of the software.

The last mode is the oscilloscope mode which permit to see all the data (40us period) of a given channel for a defined window. In mode 1 & 2, it is possible to visualize the status of the tested card, save the data shown on the screen and control the parameters like the applied test current or the applied high voltage.

D. Functional test and calibration

The test procedures have been implemented as an upper layer of the existing functions of processing, visualisation and analysis of data. When a test is launched, the appropriate mode is set and the readout starts. The test function configures the parameter to be tested and analyses the resulting behaviour. The result of each step inside a test is written in a log file and the number of errors and the severity is totalised in order to label each card for the repair management.

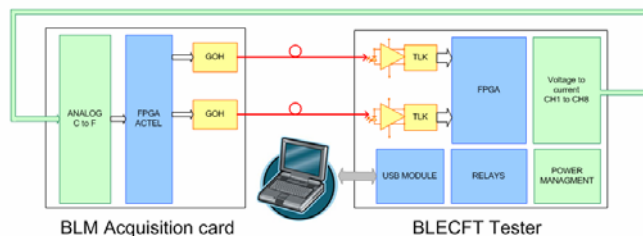


Figure 6: Test setup of the tunnel card.

There are numerous parameters to check during the functional test; the optical link connection status, the board status, the test mode response and the linearity of the inputs.

1) The optical link connection

Prior to further test, the optical link must be working as defined. In addition to the connected/not connected test, the error detection is checked (*CRC*) and reported.

2) The tunnel card status and auto-test functionalities

There are 32 statuses to be checked. There are 16 for the state of the inputs; if one channel is not functioning like defined (the voltage on the integrator is saturated at the maximum) a status is showing this. If this status stays longer than 100 seconds another status is set. To realize this test, a feature in the current sources permits to invert the current sent and then saturate the input stage.

The power supplies are also monitored on the tunnel card. To test this, the *BLECFT* includes a command to lower the

power supplies feeding the tunnel card and then setting the status warning.

The rest of the statuses are related to the auto-test functions. To enter in these test modes and be able to verify their correct behaviour, the input of the high voltage survey has to be controlled by the *BLECFT* with a *DAC*. For each auto-test and command (4 in total) the voltage is set by the test function and the result is controlled.

3) Calibration of the tunnel card inputs

The system is used to calibrate accurately the gain and input offset current of the tunnel card. The operator has to adjust the 16 potentiometers on the card. The software is showing the actual values and informs when the correct position is reached while the operator is manipulating the card.

4) Linearity of the measurements

One of the most important verification is the linearity check. For this purpose the current sources have been carefully built and calibrated. The test is driven by a text file, which specifies every measurement. The software follows each step and compares the measurements with predefined thresholds to determine if the input is usable or not and saves the result into a file.

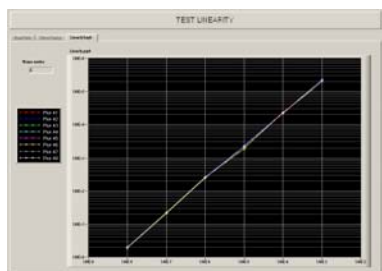


Figure 7: Window of the linearity test result.

Summary

The beam loss monitoring system for the *LHC* uses a radiation tolerant acquisition card (*BLECF*) to measure the current of the ionization chambers. The data are transmitted to the surface to a *VME* board (*DAB*) using optical links. The data are processed in it and decisions are taken in case of dangerous losses. In order to visualize and test the *BLECF* in an efficient way, a single card with dedicated software has been developed with flexible and powerful features.

The card is able to check the linearity of the measurements from the *BLM* acquisition card. A complex current source has been developed to be able to feed the inputs with currents from 10pA to 1mA (8 orders) with a reasonable accuracy (better than the input tolerance). To check if the results are in the expected tolerances a sequence of current settings is launched with the software to scan the whole dynamic range. When the system operates in the similar mode as the future *LHC* system (Running Sums acquisition), it is possible to check different indicators like the number of wrong Cyclic Redundancy Check (*CRC*) of the optical link or the type of error appearing in the receptions of the packets. In order to check specific data during the development of the *BLECF*, visual displays have been implemented in the software to

display the acquisitions versus time values of the current-to-frequency converter and the sampled value of the Analog to Digital Converter (*ADC*), which are entering in the calculation of the final current.

The optical receivers use photodiodes with automatic gain control and are interfaced with an 8b/10b transceiver. The *FPGA* holds the reception logic for the data, the processing of them (taken from the future *LHC BLM* system) and the logic for the link to the *PC* (including control and acquisition). The software is able to integrally control the card in its different mode of operation including a reading of the raw data, a high speed reading, visualization of the resulting processing of the *FPGA* calculation (running sums) and the functional and linearity tests. The program has been written in C and linked with a user friendly interface. The board can be powered over the *USB* of a laptop.



Figure 8: The *BLECFT* final box.

The system has been successfully used during the development phase at *CERN* and especially used for the *BLECF* during the validation of the *FPGA* description. Since the processing of the data is similar to the final system and very compact, the box has been successfully used as readout system during radiation tolerance campaigns for the *BLECF* at *PSI*. For the same reason, the system will also be used during installation and commissioning of the *LHC BLM*. Another use of this system is the investigations for the beam condition monitors of the *CMS* experiment using diamond detectors.

III. REFERENCES

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