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Functional and linearity tester system for the LHC beam loss monitoring data acquisition card

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In the frame of the design and development of the beam loss monitoring (BLM) system for the Large Hadron Collider (LHC) a flexible tester has been developed to qualify and verify during design and production a data acquisition card. It permits to test completely the functionalities of the board as well as realizing analog input signal generation to the acquisition card. The system utilize two optical receivers, a Field Programmable Gate Array (FPGA), eights flexible current sources and a Universal Serial Bus (USB) to link it to a PC where a software written in LabWindows (National Instruments) runs. It includes an important part of the measurement processing developed for the BLM in the future LHC accelerator.

Summary

The beam loss monitoring system for the LHC uses a radiation tolerant acquisition card (BLECF) to measure the current of ionization chambers. The data are transmitted to the surface to a VME board (DAB) using optical links. The data are processed in it and decisions are taken in case of dangerous losses. In order to visualize and test the BLECF in an efficient way, a single board with dedicated software has been developed with flexible and powerful features.

The board is able to check the linearity of the measurement from the BLM acquisition card. A complex current source has been developed to be able to feed the inputs with current from 10pA to 1mA (8 orders) with a reasonable accuracy (better than the input tolerance). To check if the results are in the expected tolerances a sequence of current settings is launched with the software to scan the whole dynamic range. When the system works in the similar mode to the future LHC system (Running Sums acquisition), it is possible to check different indicators like the number of wrong Cyclic Redundancy Check (CRC) of the optical link or the type of error appearing in the receptions of the packet. In order to check specific data during the development of the BLECF, visual displays have been implemented in the software for the values of the current-to-frequency converter and the sampled value of the Analog to Digital Converter (ADC) entering in the calculation of the final current.

The use of a USB module has been launch by a student in his thesis. The choice of the modules have been determined by their speed which they reached (use of USB 2.0) and by the availability of a complete library of functions. The optical receivers use photodiode with automatic gain control and are interfaced with an 8b/10b transceiver. The FPGA holds the reception logic for the data, the processing of them (taken from the future LHC BLM system) and the logic for the link to the PC (including control and acquisition). The software is able to integrally control the board in its different mode of operation including a reading of the raw data, a high speed reading, visualization of the resulting processing of the FPGA calculation (running sums) and the functional and linearity tests. The program has been written in C and linked with a user friendly interface. The board can be powered over the USB of a laptop.

The system has been successfully used during the development phase at CERN and especially used by the designer of the BLECF during the validation of the FPGA description. Since the processing of the data is similar to the final system and very compact, the board has been successfully used as readout system during radiation tolerance campaigns for the BLECF at PSI. For the same reason, the system will also be used during installation and commissioning of the LHC BLM. Another use of this system will be the investigations for the beam condition monitor of the LHC CMS experiment using diamond detectors.

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