

# Wafer test of the LHCb Outer Tracker TDC-chip

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## Abstract

The OTIS-TDC is the front end readout chip for the LHCb Outer Tracker. It is designed to measure drift times with a resolution better than 1 ns. As the chip will be directly mounted to its board, the test have to be performed on the wafer itself. As the testing period for 7 000 chips was only three weeks, many test routines have been implemented on a FPGA. Each chip is subjected to detailed probe testing to ensure the full functionality as well as a good performance.

Overall 47 wafer have been tested. From the chips passing the test 2 000 have been used in the Outer Tracker front end electronic.

## I. INTRODUCTION

The LHCb Outer Tracker is a straw tube detector. In order to measure the drift times of the electrons in the straws, the OTIS chip was designed. A detailed description can be found in [1]. It is a 32 channel time to digital converter (TDC) chip and was developed at the ASIC laboratory at the Heidelberg University. It is implemented in a 0,25  $\mu\text{m}$  commercial CMOS process using radiation hard layout techniques. The chip can be divided into four major components:

- The TDC core
- The control algorithm
- The pipeline memory and derandomising buffer
- The  $I^2C$  slow control

The TDC core performs the drift time measurement, performed by a 64 stage delay lock loop (DLL). Therefore the clock cycle is divided into pieces of 390ps length at the LHCb frequency (40MHz). If a channel is hit, the logic latches the clock position in the DLL into the corresponding 6 bit channel hit register. At each clock cycle this information is passed on to the pipeline register along with further status informations.

The control algorithm prepares the data for read out. Two read out schemes are implemented. In the first mode (encoded hitmask) the logic searches for the first hit in each channel. Up to 3 bunch crossings (BX) are looked at. A second hit within the 3 BX is not transferred to the memory in this mode. The second mode (plain hitmask) provides a multi hit capability. It first encodes, in which channel and BX a hit occurred. This hitmask is followed by the pure 6 bit drift time informations. Therefore several consecutive hits on the same wire can be read out with one trigger.

The pipeline memory is build with dual ported SRAM cells with a dimension of 164x240 bit. Organized as a ring buffer, each line is stored for 4s (164x25ns) in the memory awaiting

the L0 trigger decision. After this time the information is overwritten by a new data set. Up to three lines are copied into the derandomising buffer on a positive L0 decision. The buffer compensates for trigger rate fluctuations that may occur.

A schematic overview of the OTIS-TDC chip can be seen in figure 1.

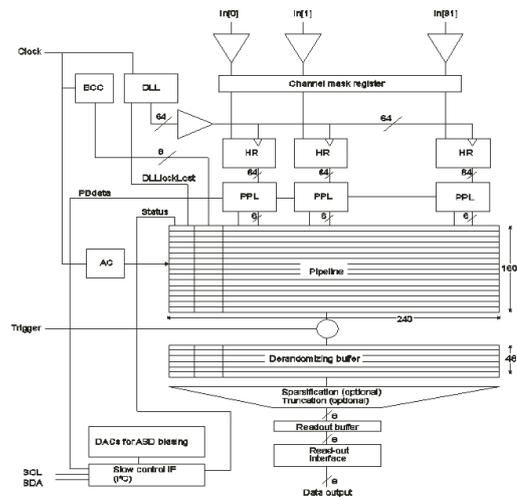


Figure 1: A schematic overview of the OTIS-TDC chip

The chip was produced as part of the multi project wafer run 15 by CERN. The wafer contained two versions of the OTIS-TDC, namely 1.2 and 1.3. The difference between these versions are very minor modification which promised a better performance in extreme conditions. For this wafer test these variations can be neglected and therefore the two versions are treated in the same way. The wafers were delivered in one lot of 47 wafers, each containing 71 Otis chips of each version. The lot was received on November 15<sup>th</sup> 2005. Due to the other projects the wafers had to be send back on December 5<sup>th</sup>.

The chips were identified by the wafer name and location on the wafer. The test results were stored into log-files and summarized in a wafer map. Only chips passing all tests are used for the Outer Tracker front end electronic.

## II. THE WAFER TEST

The test should verify the digital functionality of the chip and study its performance. The test setup is divided into three parts. The first part is the semi-automatic probe station. The probe station is controlled by a PC running a vendor specific software. This software can receive commands from other computers and provides status information.

These commands are given by the master PC of the test

setup. This PC orchestrates the complete test procedure. It is running a LabView application to control the test flow. It also performs measurements of analogue voltages, monitors the power consumption and provides a test of the slow control.

The final part of the test setup is the slave PC. It is also running a LabView application which communicates with a FPGA card via the PCI-bus. The FPGA card contains an ALTERA Stratix S25 chip which is also the DAQ of the real experiment. The FPGA is needed to get a reliable and fast DAQ in the test. It also provides all fast control signals such as clock and resets. Figure 2 shows an overview of the test setup.

The complete test procedure consists of ten steps:

1. Access next chip and make contact
2. Switch on power of the needle card
3. Measure power consumption
4. Program and verify the register on the chip
5. Start the FPGA measurement
  - (a) Check header bits and data integrity
  - (b) Check all 32 data channel
  - (c) Time measurement on 4 channel
  - (d) provoke an error condition
6. Program and verify the register on the chip with a second setting
7. Set and measure DAC values of the chip
8. If one of the steps 3) to 7) fail, repeat them with a separation of the needle card and chip performed
9. Switch off power
10. Separate needle card and chip and go to 1)

The repetition of test steps in case of an error was due to the imperfections of the probe stations. As its chuck and therefore wafer was not completely flat with respect to the needle card, the contact quality to the chip pads changes. A short separation of the needle card and the wafer solves this contact problem.

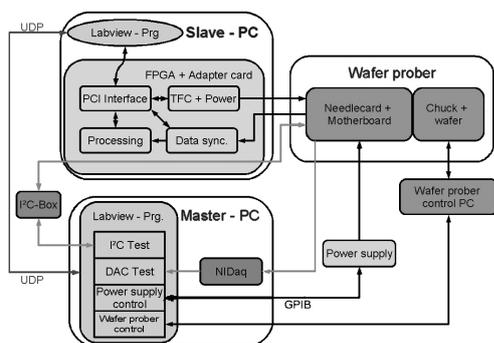


Figure 2: A schematic overview of the test setup

### A. Tests by the master PC

Apart from steering the test flow, the master PC also performs some of the infrastructure tests. The first check includes the power consumption. It verifies, that there are no short circuits on the chip. If too much current is drawn, the chip is marked faulty by power consumption.

The second test concerns the slow control. It writes a checker pattern into the  $I^2C$  register. The register values are read back and compared to the initial ones. Any failure is marked as a digital error. The read only register are compared to the expected value. After the FPGA test is performed, this test is repeated with a second pattern on another  $I^2C$  address. This should exclude any stuck bits in the slow control register part of the chip.

The third test done by the master PC is the measurement of the analogue voltages. In order to produce the threshold voltages for amplifier chip, the Otis contains a DAC to provide four voltages. These voltages can range from 0 to 2,5 mV and can be set via  $I^2C$  register. The test sets now these 8 bit register with values of 0,1,2,4,8,16,31,64,128 and 255. The measured voltage has to be in range of 50 mV from the expected value. Also the difference of all four DAC values have to be in the same range compared to each other. An error in this test is marked as a threshold voltage error.

### B. Tests by the slave PC

The tests done by the slave PC concerns the data received from the Otis chip. In order to handle the high data rate all the test function are implemented on a FPGA chip. The Stratix FPGA chip was chosen due to the fact that the same chip type is also used in the buffer boards of the LHCb experiment.

#### FPGA firmware

The firmware of the can be divided into four parts:

- Infrastructure
- DAQ
- Analysing functions
- PCI interface

In order to get the Otis chip working, a infrastructure, namely the fast control signals have to be provided. These signals contain the clock signal, the trigger signal and all reset signals such as L0 reset and event count reset. In order to get a time measurement, a pulser was also implemented. It is based on the PCI clock signal and therefore it is completely independent of the LHCb clock signal. This ensures a kind of random hit signal.

The DAQ part searches for the OTIS data in the data stream. It tries to synchronize using the data valid signal as well as the comma word. A successful synchronization is a check of the data quality in itself. The data found in the data stream are then prepared for the histogram unit. The raw data is also written into a Fifo for debugging propose.

With the histogram unit errors in the header bits are counted. It also builds a histogram of the event IDs as a check of the data quality. It counts the hits in each of the 32 channel and makes a detailed time histogram for one channel.

All these parts are read out and controlled by the PCI interface. An overview is shown in figure 3

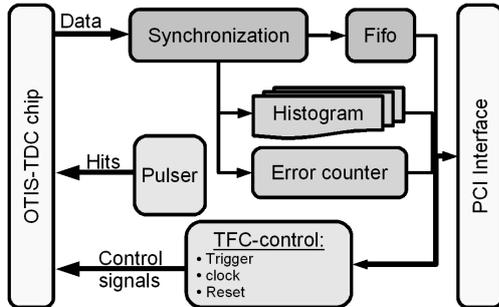


Figure 3: A schematic overview of the FPGA firmware

#### FPGA tests

Four tests are performed by the FPGA. The first test is a general look at the data integrity. All the header bits are compared to an expected value and errors are counted. It is also checked, if the number of event matches the number of triggers. Any error in this test is marked as a digital error.

The second test checks all the channels. This is done by pulsing first the even channel and requesting 10 000 data sets. It is then looked, if each even channel have measured 10 000 hits. All the odd channel are expected to have seen only view hits. In a second round the odd channel are pulsed. Any channel which does not receive 10 000 hits in its round is marked as dead channel.

The third test performs a time measurement on the four most critical channels. This is done by calculating the differential non-linearity (DNL) for each channel.

$$DNL(i) = \frac{Hits(i) - Hits(i-1)}{expected\ Hits(i)}$$

$i = channel\ number$

$$Hits(i) = hits\ seen\ in\ channel\ i$$

The DNL is a indication on the size of each time bin. The DNL for the complete chip is then calculated by adding the absolute values of the minimum and maximum of the DNL(i).

In the actual test a "random hit" signal is send. In an perfect chip this would result in a DNL of zero. As this can not be achieved by the OTIS chip due to the design the limit was set to two time bins (780 ps). All chips with greater DNL are marked an error in the time measurement.

The final test provokes an error condition and checks the re-action of the chip. On a failure in one of the test steps results in one repetition of all the test steps. An error is only marked if the failure occurred in the repeton as well.

### III. TEST RESULTS

Overall 7332 chips have been tested. The yield obtained was 91,5% for the version 1.3 chip and 88,7% for version 1.2 . From the over 6000 chips passing the test, the LHCb OT will use around 2000.

The distribution of errors is given in table 1. Figure 4 shows the yield of each wafer.

Table 1: Distribution of errors

Error	OTIS 1.2	OTIS 1.3
Time measurement	1,8%	1,9%
Threshold voltage	2,4%	0,8%
Dead channel	7,6%	4,5%
Digital	10,0%	7,2%
Power consumption	3,0%	1,3%

### IV. ACKNOWLEDGMENT

We would like to than the Heidelberg ASIC Laboratory Team for supporting this work.

### REFERENCES

- [1] H. Deppe, U. Stange, U. Trunk, U. Uwer, The OTIS Reference Manual Physikalisches Institut, Universität Heidelberg, Version 1.2 $\gamma$ , 2005

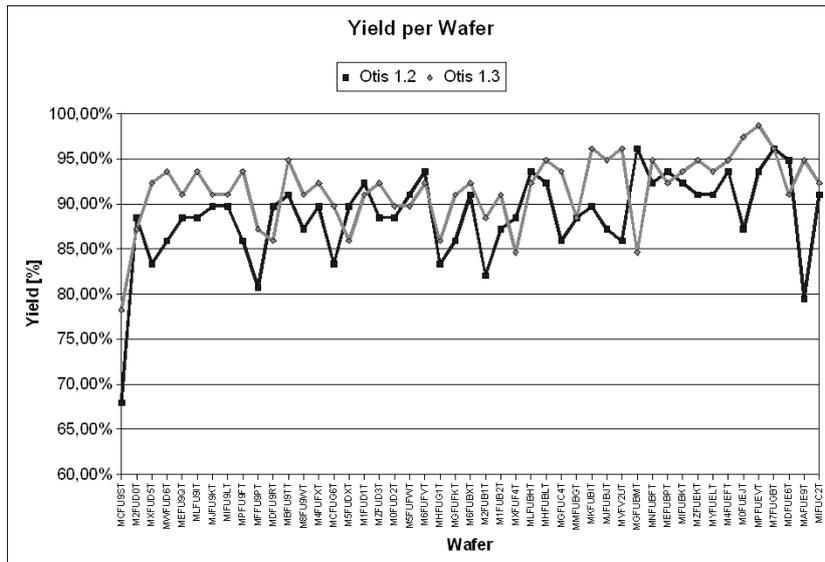


Figure 4: A figure caption