Wafer test of the Outer Tracker TDC-chip

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---------- Otis TDC chip ---------

The LHCb Outer Tracker

The LHCb Outer Tracker (OT) is a straw tube drift-chamber and consists of 3 stations. Altogether the Outer Tracker made up of 54.000 read out channels. Figure 1 shows an artist view of the OT detector.
In order to measure the drift times of the electrons in the straws, the OTIS chip was designed. It was developed at the ASIC laboratory of the University of Heidelberg.

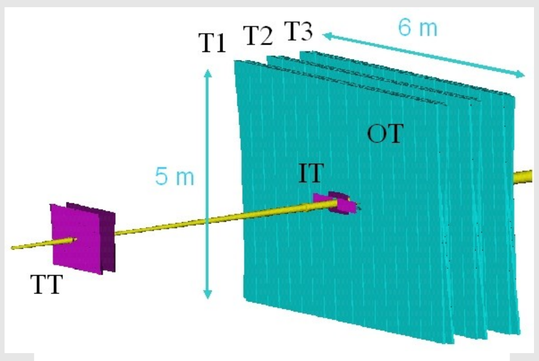


Figure 1: An artist view of the LHCb Outer Tracker

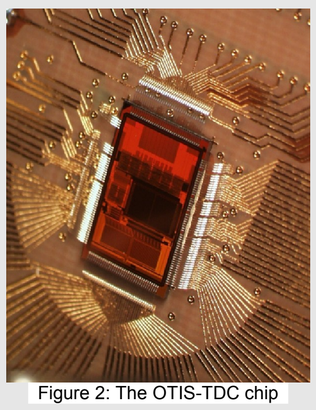


Figure 2: The OTIS-TDC chip

The OTIS-TDC chip

The Otis is a 32 channel time-to-digital-converter (TDC) chip. It is implemented in a 0,25 µm commercial CMOS process using radiation hard layout techniques.
The chip can be divided into three major components: the TDC core, the control algorithm and the pipeline memory and derandomising buffer. Figure 3 shows an schematic overview.

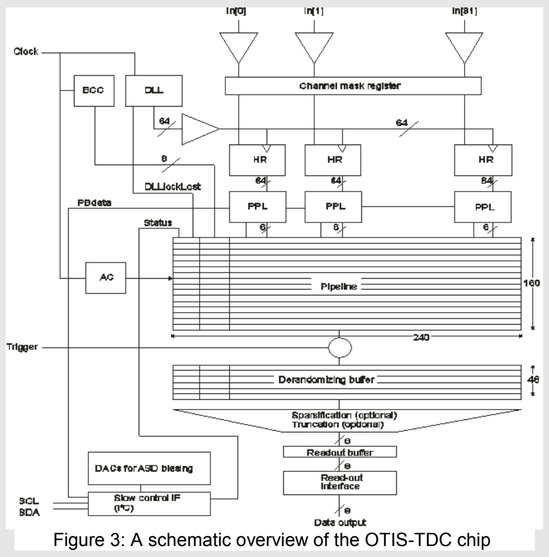


Figure 3: A schematic overview of the OTIS-TDC chip

The TDC core

The TDC core performs the drift time measurement, performed by a 64 stage delay lock loop (DLL). Therefore the clock cycle is divided into pieces of 390 ps length at the LHCb frequency (40 MHz).
If a channel is hit, the logic latches the clock position in the DLL into the corresponding 6 bit channel hit register. At each clock cycle this information is passed on to the pipeline register along with further status informations.

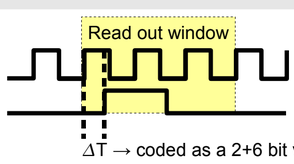


Figure 4: The drift time measurement principle

The control algorithm

The control algorithm prepares the data for read out. Two read out schemes are implemented. In the first mode (“encoded hitmask”) the logic searches for the first hit in each channel. Up to 3 bunch crossings (BX) are looked at. A second hit within the 3 BX is not transferred to the memory in this mode.
The second mode (“plain hitmask”) provides a multi hit capability. It first encodes, in which channel and BX a hit occurred. This hitmask is followed by the pure 6 bit drift time informations. Therefore several consecutive hits on the same wire can be read out with one trigger. Table 1 shows the data format of each mode.

The pipeline memory and derandomising buffer

The pipeline memory is build with dual ported SRAM cells with a dimension of 164x240 bit. Organized as a ring buffer, each line is stored for 4µs (164x25ns) in the memory awaiting the L0 trigger decision. After this time the information is overwritten by a new data set.
Up to three lines are copied into the derandomising buffer on a positive L0 decision. The buffer compensates for trigger rate fluctuations that may occur.

a)

Bit :	0 .. 31	32 .. 39	.....	280 .. 287
Data :	Header	Drift time ch 0	.....	Drift time ch 31

b)

Bit :	0 .. 31	32 .. 95	96 .. 103	....
Data :	Header	Hitmask	Drift time (1)	....

Table 1: Data format of the readout scheme.
(a) encoded hitmask, (b) plain hitmask

---------- The test setup ----------

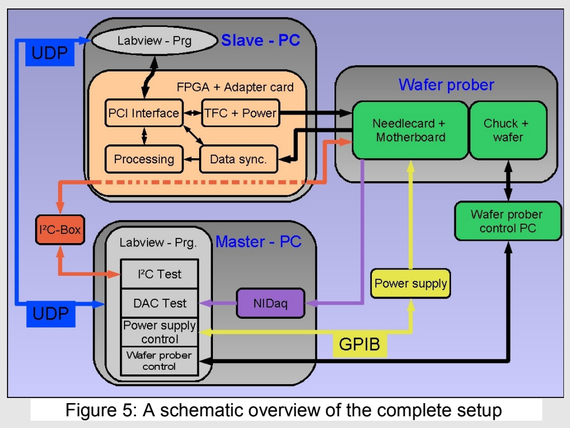


Figure 5: A schematic overview of the complete setup

The wafer test setup

The test setup consists of 3 components: the master PC, the slave PC and the wafer prober. The wafer prober is externally controlled with a third PC.
The master PC orchestrates the whole test procedure. It is running a LabView™ program. The main control loop calls four sub programs. The first one is a I²C interface to set and read the register of the OTIS chip. The second function is the readout of a DAC card for the test of the analogue voltages. Furthermore it can control the power supply via GPIB and talks to the wafer prober control PC to access a chip.
The slave PC was also running a LabView™ program which could access the FPGA card housing an Altera Stratix S25 chip. For a reliable test 144 MByte/TDC of data have to be taken. Therefore it was decided to implement all DAQ and analysing routines on the FPGA itself.

The FPGA firmware

The FPGA firmware includes four parts:

- TFC-control and Pulser
- Synchronization
- Histogram and error counter
- PCI interface

The TFC-control provides the clock, trigger and reset signals. The pulser generates a hit signal using the PCI clock which runs independent of the LHCb clock.
The synchronization part searches for Otis data in the data stream and prepares them for analysis. The complete data is also stored in a Fifo for debugging proposes.

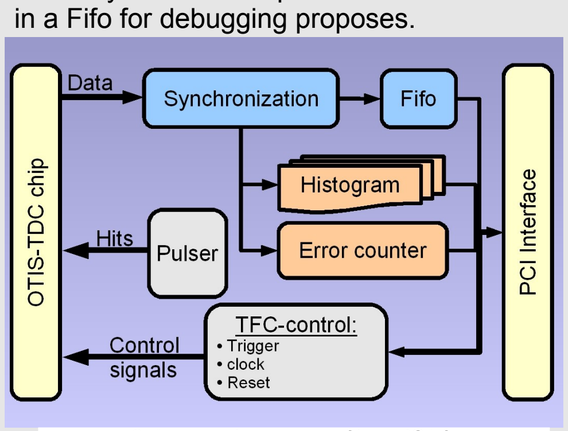


Figure 8: A schematic overview of the FPGA firmware

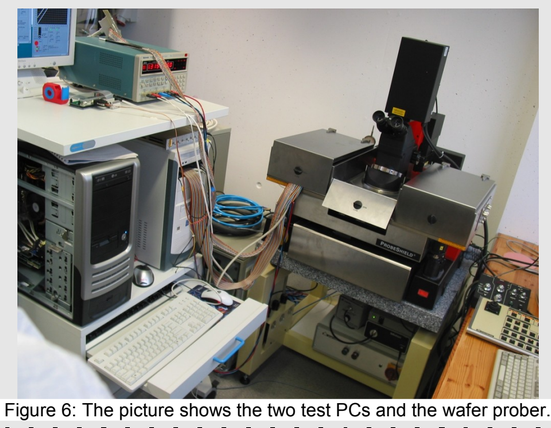


Figure 6: The picture shows the two test PCs and the wafer prober.

The test procedure

1) Access next chip and make contact
2) Switch on power of the needle card
3) Measure power consumption
4) Program and verify the register on the chip
5) Start the FPGA measurement
   a) Check header bits and data integrity
   b) Check all 32 data channel
   c) Time measurement on 4 channel
   d) provoke an error condition
6) Program and verify the register on the chip with a second setting
7) Set and measure ADC values of the chip
8) If one of the steps 3) to 7) fail, repeat them with a separation of the needle card and chip performed
9) Switch off power
10) Separate needle card and chip and go to 1)

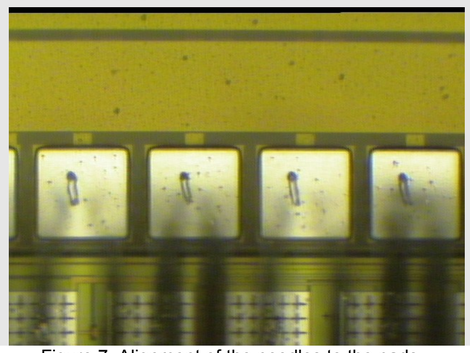


Figure 7: Alignment of the needles to the pads.

The histogram unit counts for all channel if it has been hit, performs a complete time measurement for one channel and looks at the integrity of the event counter. The header bits are checked and errors are counted.
The complete firmware is controlled and read out by the PCI interface.

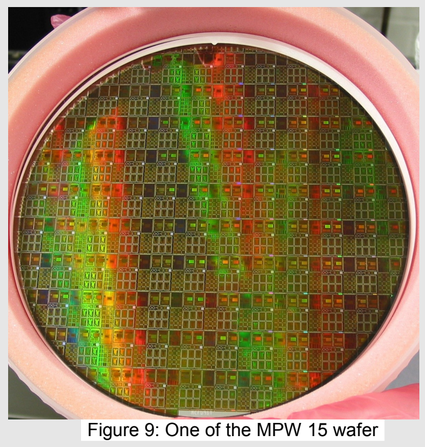


Figure 9: One of the MPW 15 wafer

---------- Otis TDC chip ---------

---------- The test setup ----------

---------- Test result ----------

Summary

The production wafer contained both Otis version 1.2 and 1.3 and was received in Heidelberg on *November 15th*. After a short start-up phase stable operation was reached. The test time of a working chip was reduced to 25s. For a faulty chip the testing time was 100s due to several repetition of test steps. A wafer was completed in about 2h.
During a test over 4.000.000 data sets (144 MByte) were analysed for a single chip. This was only possible by implementing the analysing tools on a FPGA. By using this strategy we were able to complete the whole batch of 47 wafer (7332 Otis chips) in just *2½ weeks.* The final Yield:

OTIS 1.3 ..... 91,5 %
OTIS 1.2 ..... 88,7 %

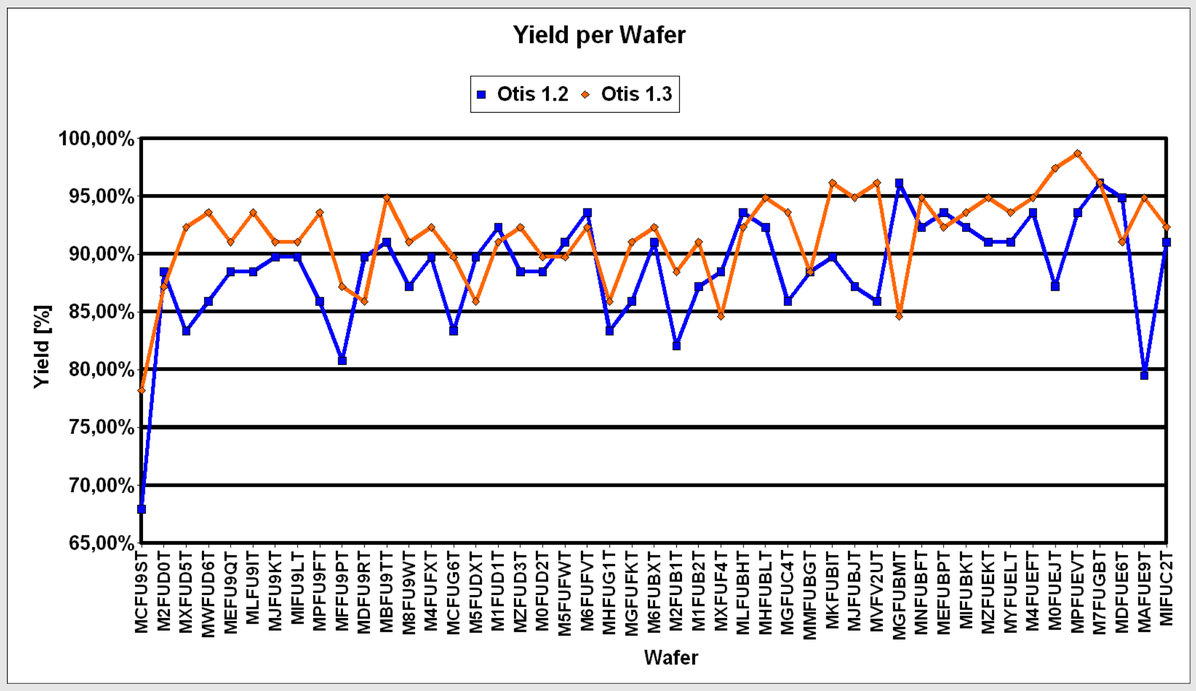
Observed errors

Time measurement: Measured time differential non linearity larger than 2 bins (780ps).
Threshold voltage: The ADC voltage differs more than 50mV from the expected value.
Dead channel: At least one channel receives no data.
Digital error: All errors in registers or data
Power consumption: A short circuit

The table below shows the distribution of error over the complete test:

	OTIS 1.2	OTIS 1.3
Time measurement	1,8%	1,9%
Threshold voltage	2,4%	0,8%
Dead channel	7,6%	4,5%
Digital errors	10,0%	7,2%
Power consumption	3,0%	1,3%

Often a faulty chip shows several of these errors at once



---------- Test result ----------