# Design and Test of the Off-Detector Electronics for the CMS Barrel Muon Trigger

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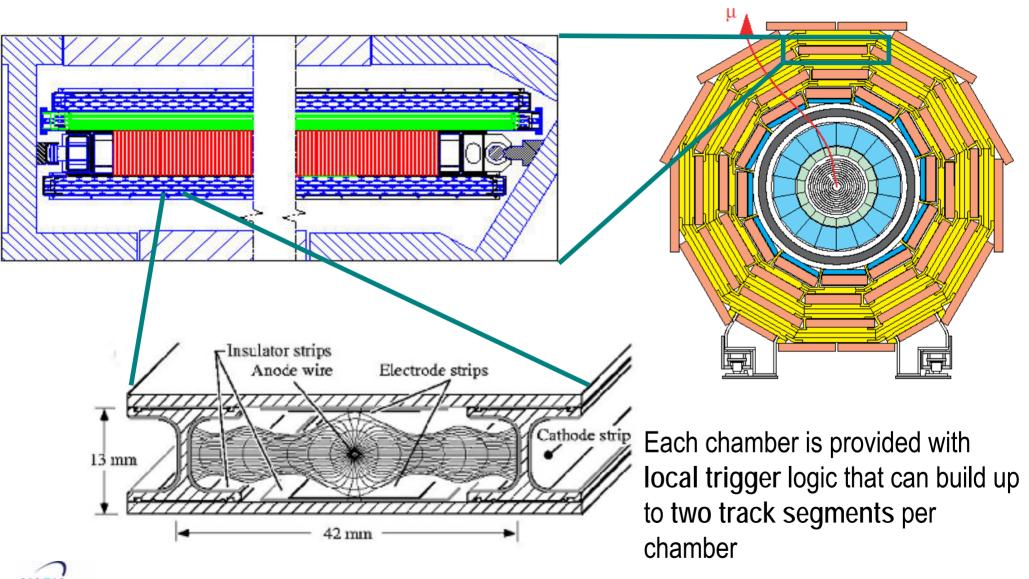
12th Workshop on Electronics for LHC and Future Experiments 25-29 September 2006, Valencia SPAIN



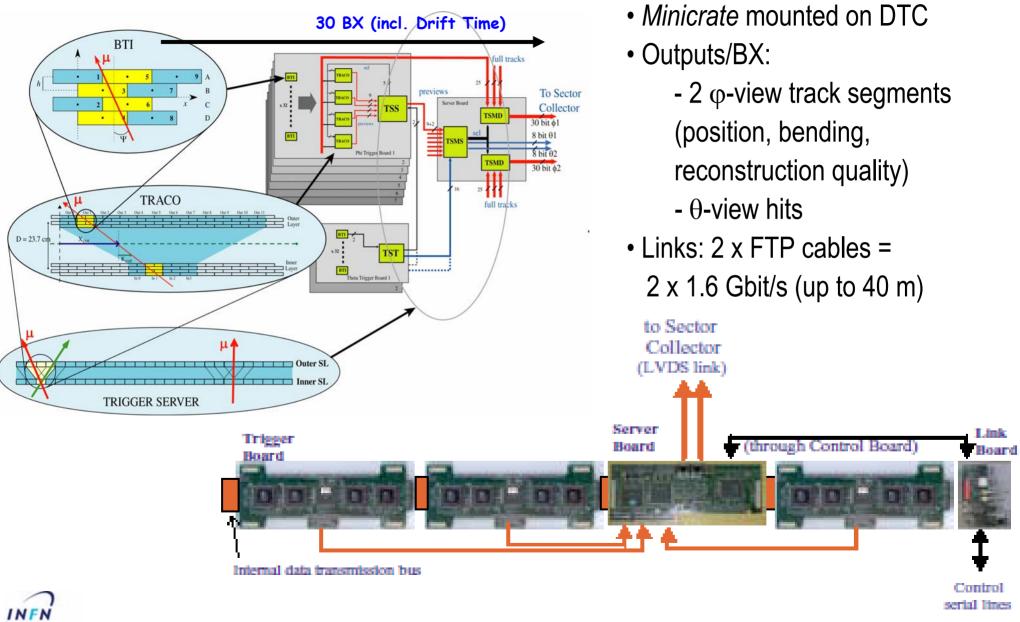
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### CMS Drift Tubes muon detectors

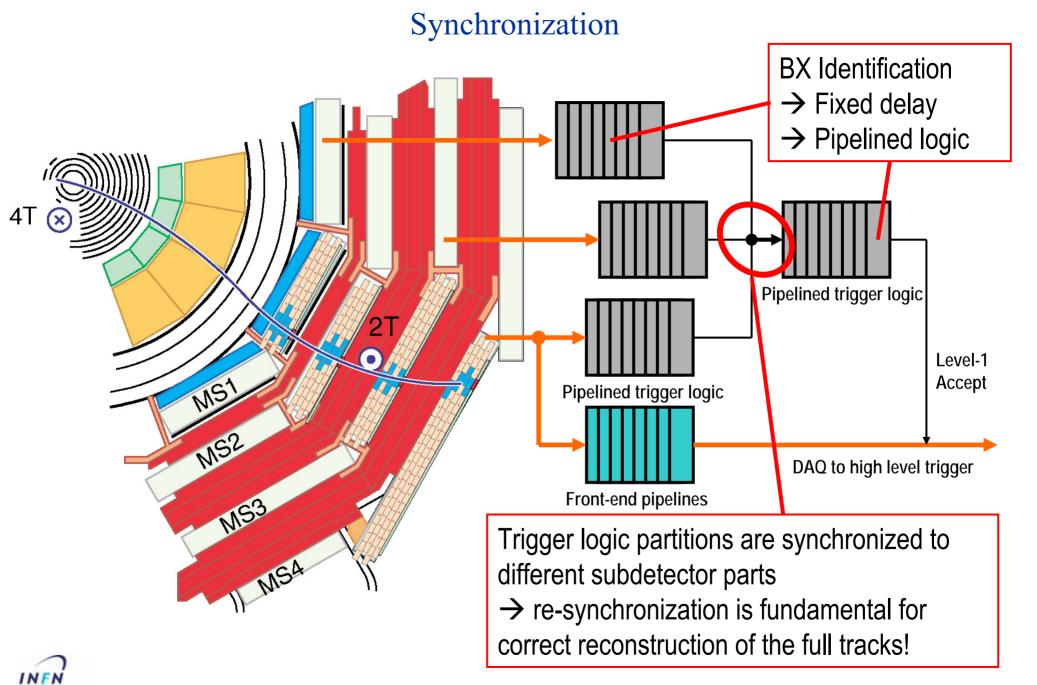
250 DT chambers in 4 concentrical stations, in 30° sectors, in 5 wheels



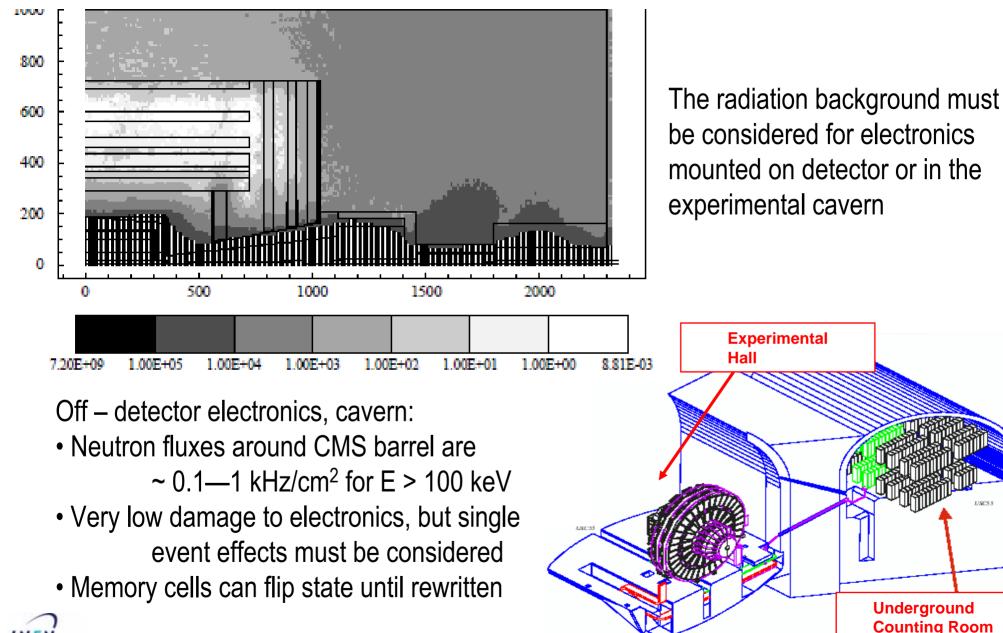
# DT Local trigger



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# Radiation tolerance



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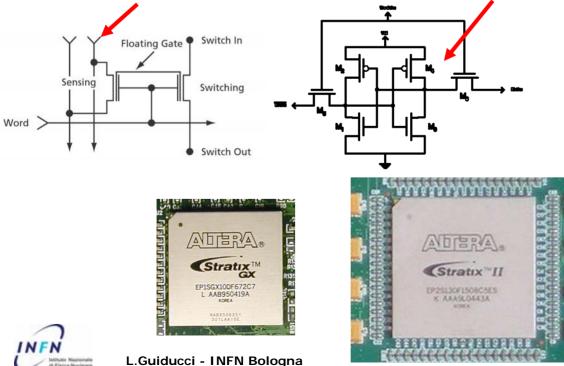
# Programmable devices technology

In the experimental cavern:



- Events due to neutron background may modify the FPGA configuration memory → change of device functionality
- ProAsicPlus FPGA from Actel
  - Configuration memory is FLASH-based
  - Embedded RAM (72 kbits) and configurable PLLs (2)

Flash cells are more robust than SRAM cells (~15 V for programming, smaller)



In the counting room:

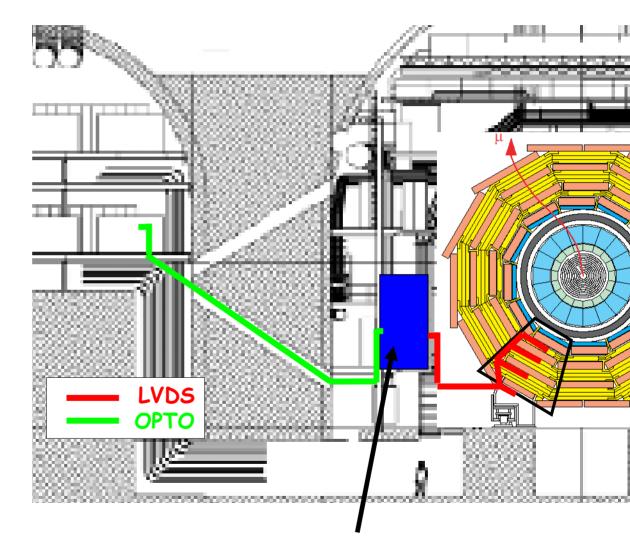
- No radiation issues
- Several SRAM-FPGA devices
  were chosen
- SRAM-FPGA market provides powerful optionals (embedded RAM, advanced I/O ...)

### Sector Collector system

• Located on detector towers, 60 SC boards (1/DT 30° sector)

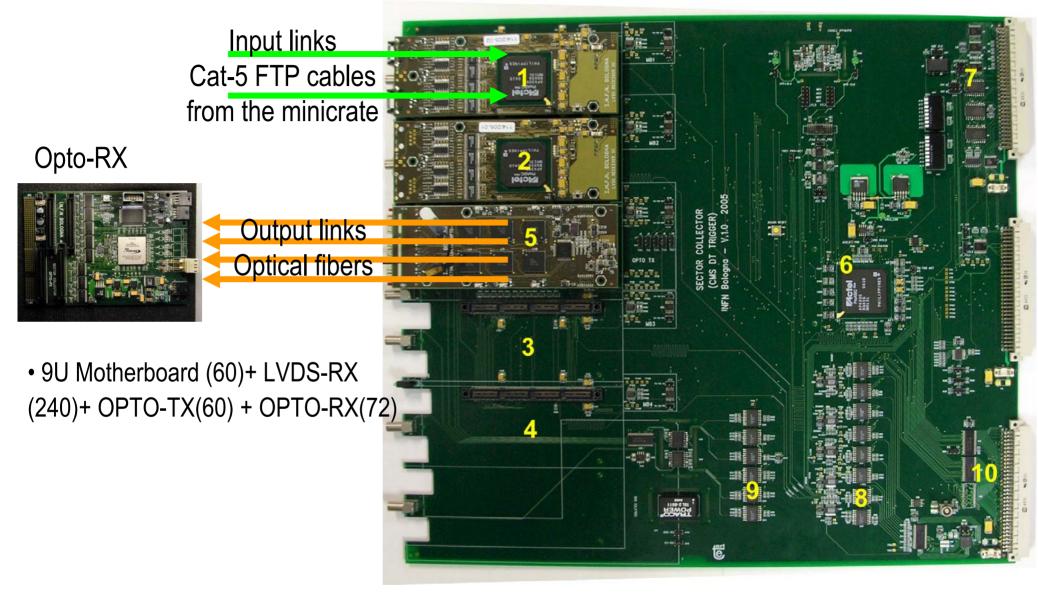
Main tasks:

- Synchronization of sector links
- Monitoring of data
- Sector-level trigger generation and distribution
- Local trigger data sent on optical fibers to the regional trigger electronics in the counting room (DT Track Finder, DTTF)

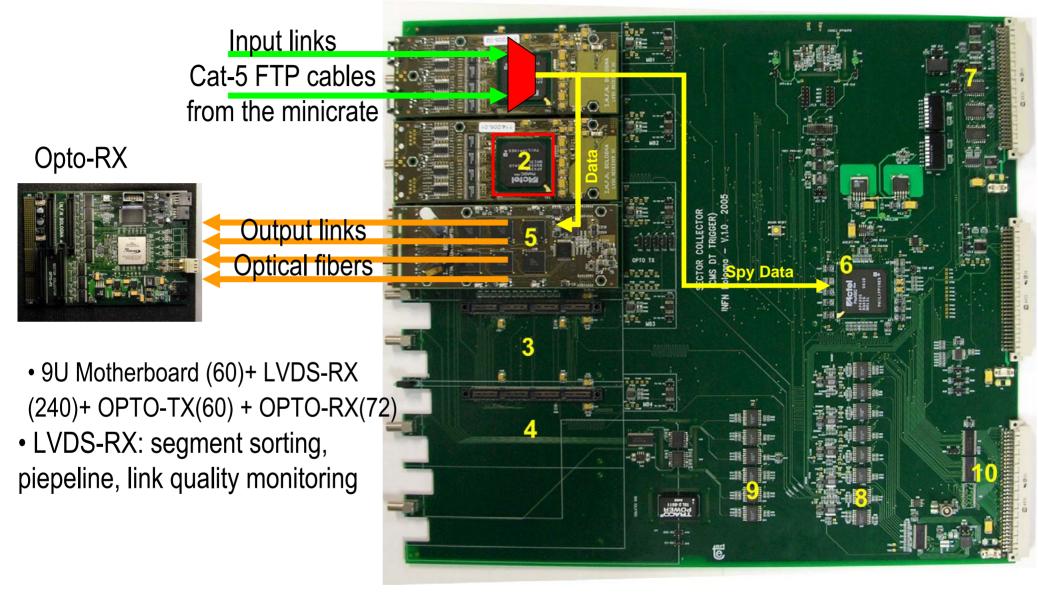


#### Sector Collector crates

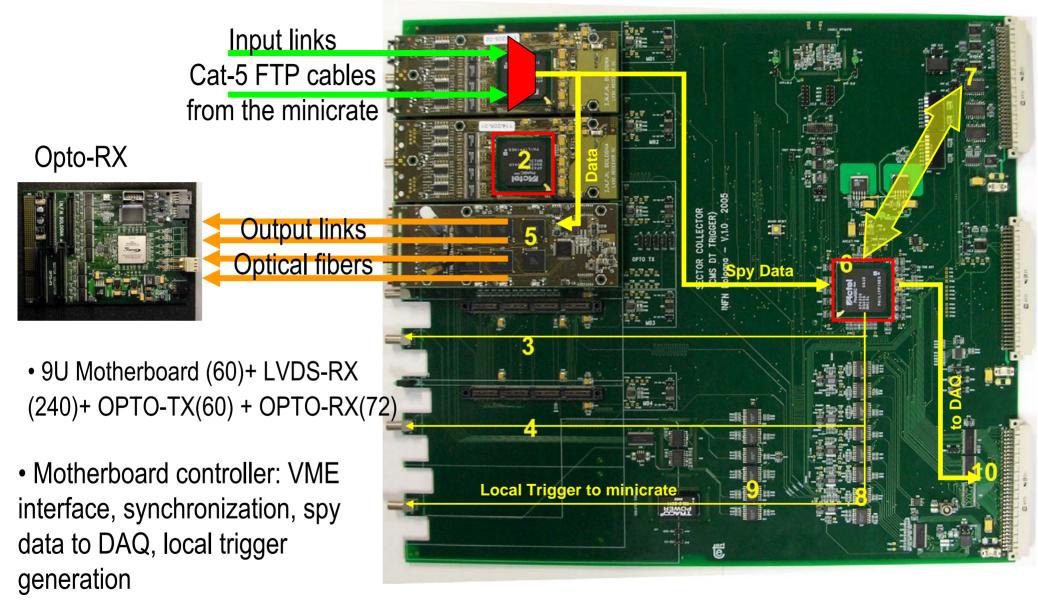




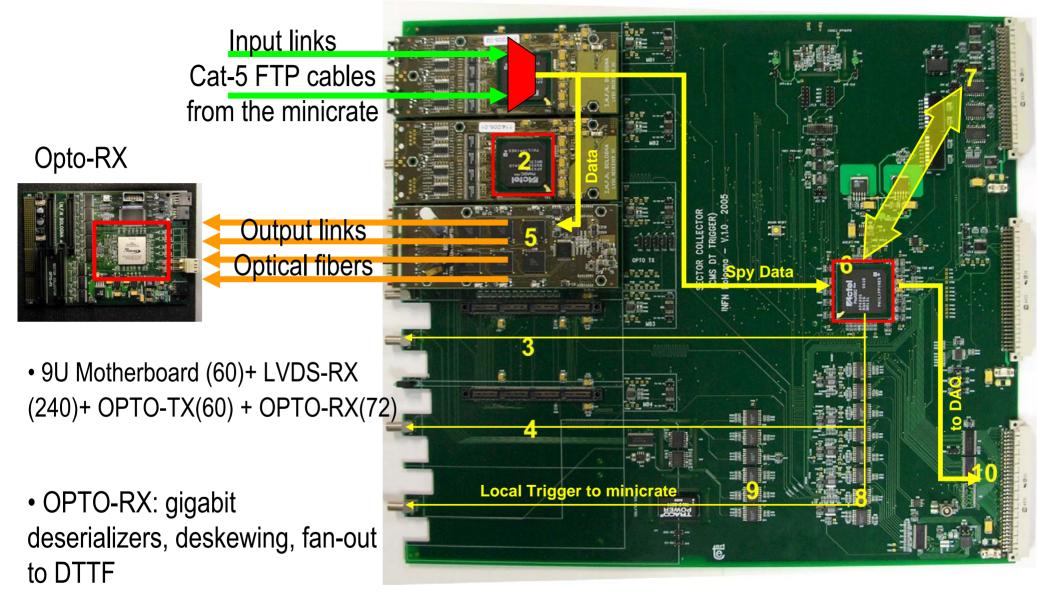


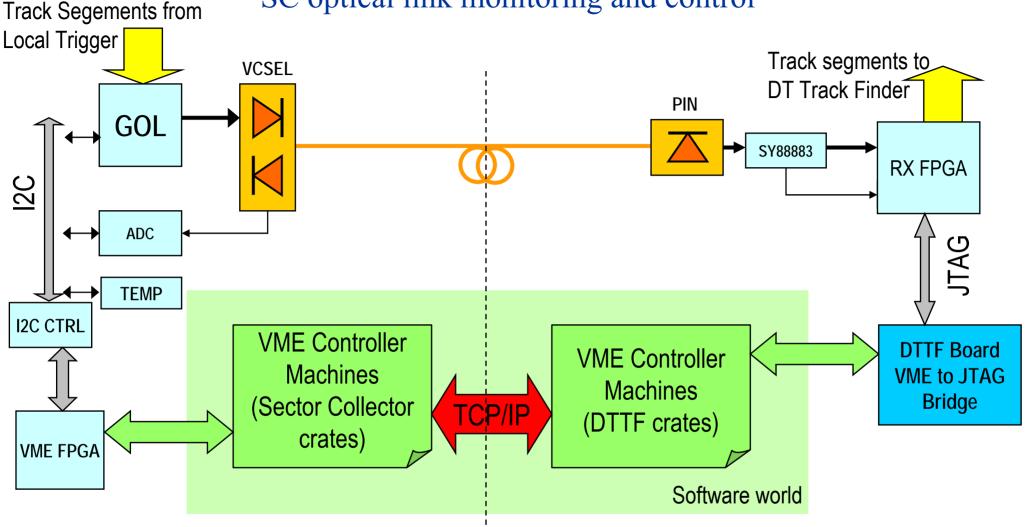










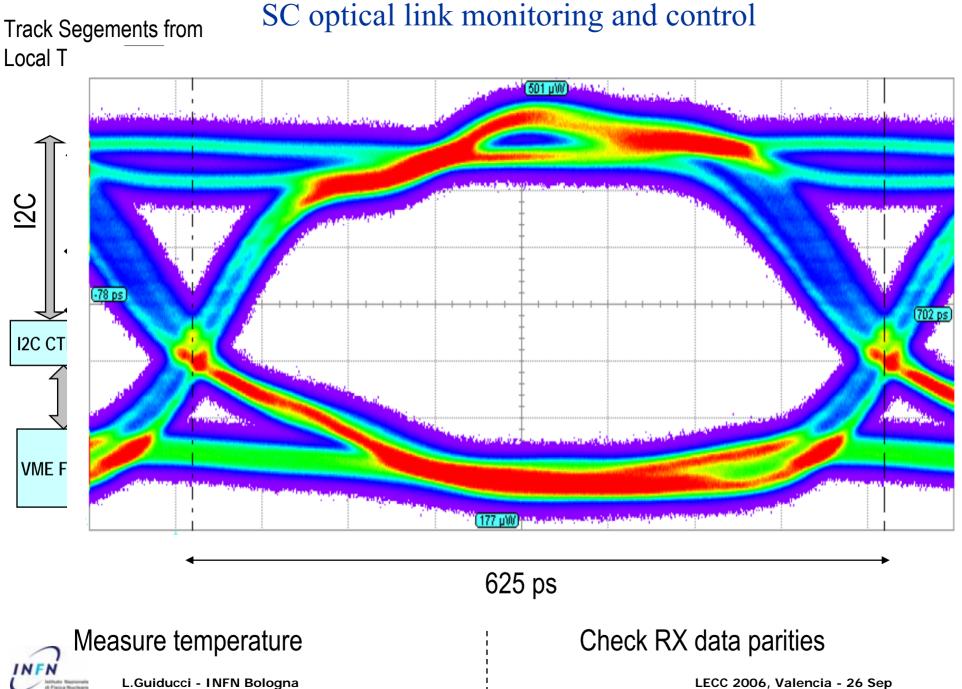


### SC optical link monitoring and control

Set GOL bias current Measure emitted light Measure temperature

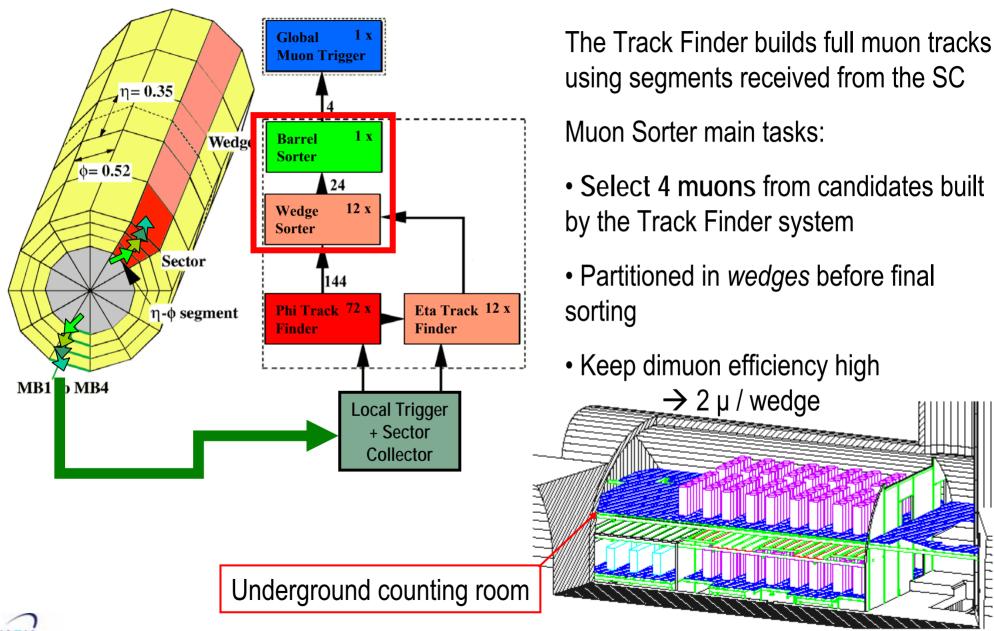
Check amplifier threshold condition Check RX frequency lock Check RX data parities

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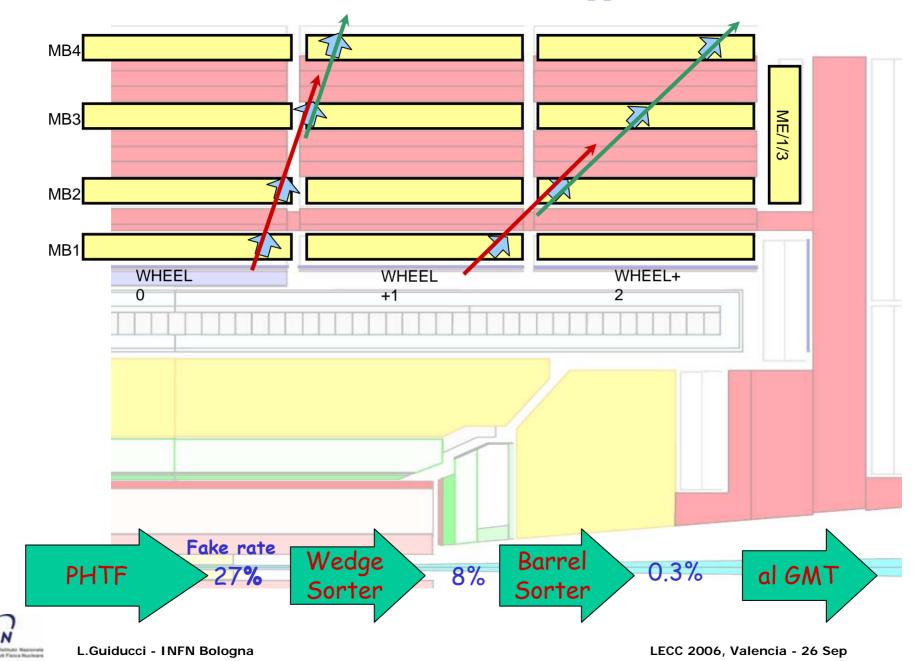
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# Muon Sorter

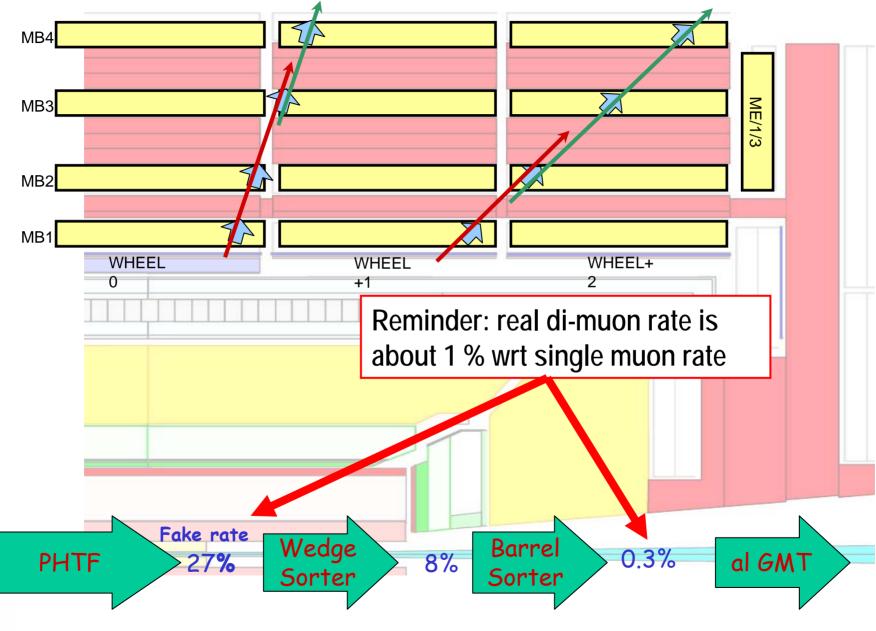


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### Muon Sorter – fake tracks suppression



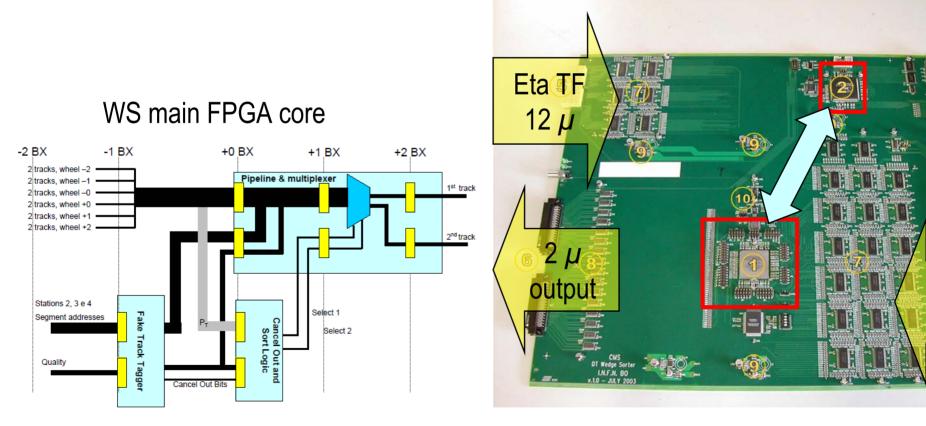
### Muon Sorter – fake tracks suppression



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# Wedge Sorter board

- VME 9U board
- 12 input, 2 output muon tracks (~ 500 bits I/O) in GTL+/LVDS
- Computational core on a single SRAM-FPGA (= low latency, simpler design)
- VME interface on a separate FPGA with bridge to main processor





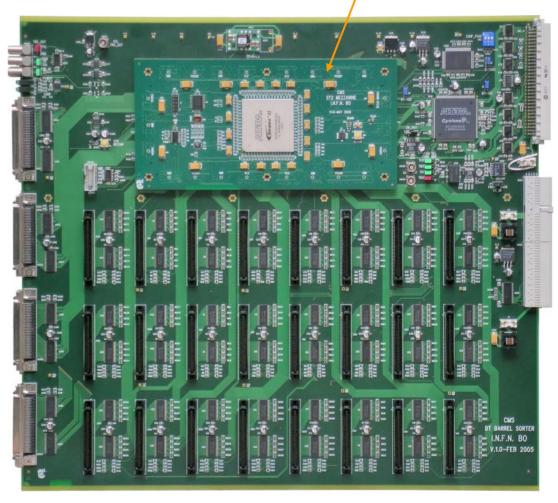
Phi TF

 $12 \mu$ 

### Barrel Sorter board

18 layers pcb

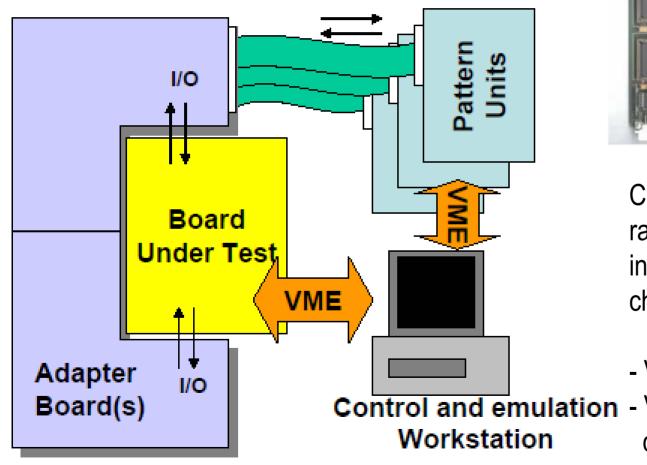
- VME 9U board
- 24 input, 4 output muon tracks (~ 1000 bits I/O) in parallel LVDS
- Computational core on a single FPGA (Altera StratixII 1508 pin) on mezzanine board
- VME interface FPGA with full speed bridge to main processor
- Full data spy system with direct VME access implemented on main FPGA
- Trigger output based on quality thresholds / pattern matching applied on track data



### Setup for dynamic tests

Pattern Unit is a VME testing device designed by CMS Bologna group: • 128 I/O • Up to 64k words

• Up to 100 MHz • Multi board setup





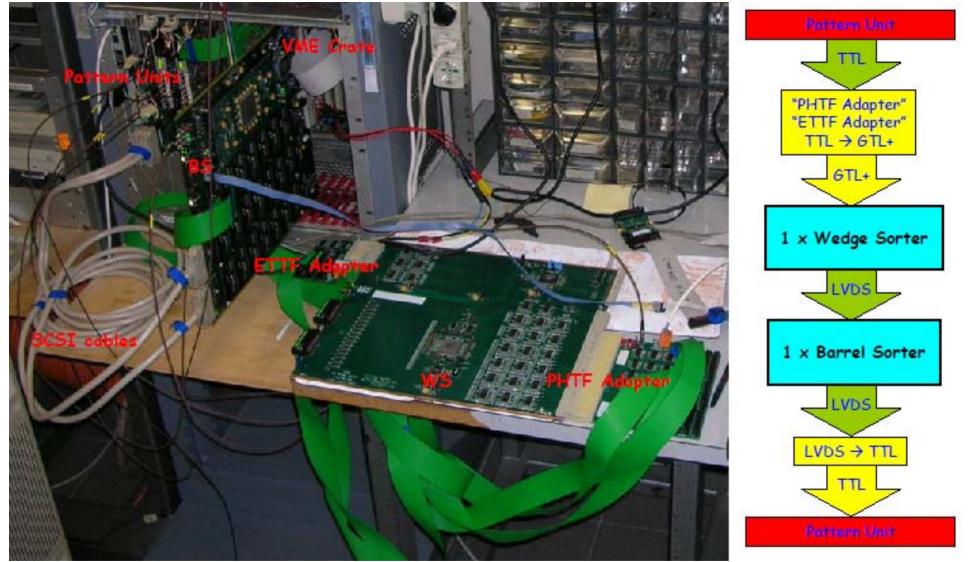
C++ software written to generate random data patterns, inject them into the board under test, and check the outputs

Verification of custom algorithms
 Control and emulation
 Verification of all board
 Workstation
 components and connections

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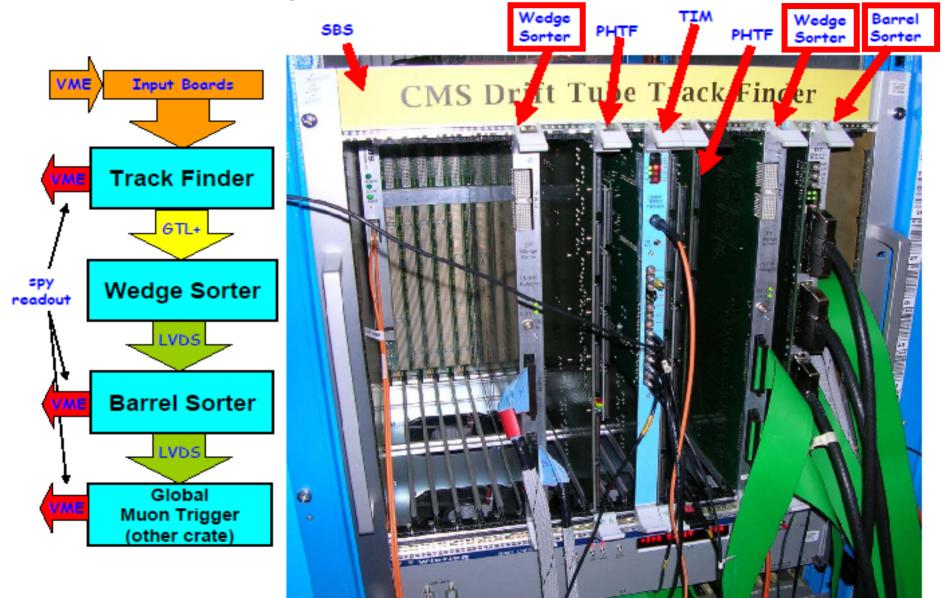
### Wedge—Barrel Sorter integration test setup



Several bugs (bad solderings, missing components) found and corrected

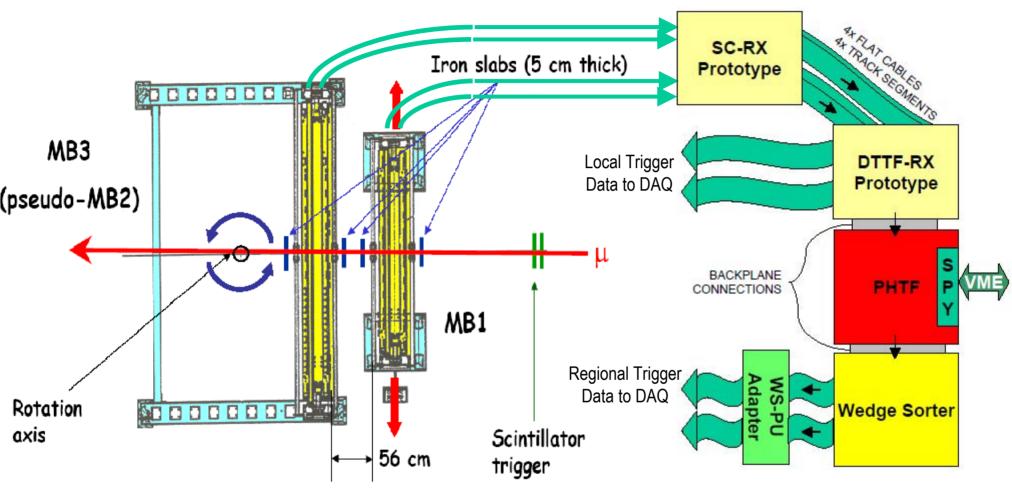


#### Integration test in Track Finder crate



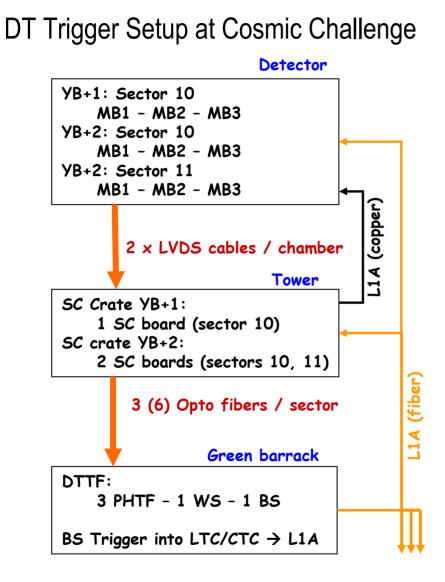


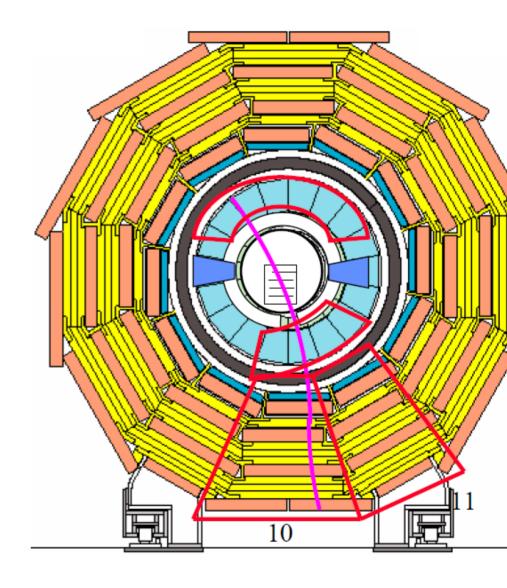
# Test Beam of the DT Muon Trigger



- Secondary muon beam with 25 ns bunched structure
- Chambers rotation and shift to emulate the bending in the magnetic field
- Off-detector electronics prototypes were effectively synchronized and readout

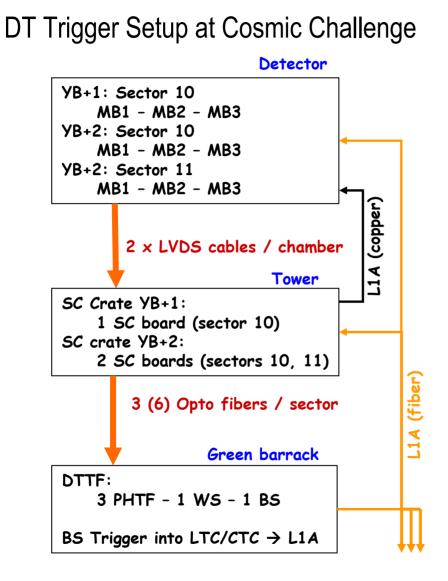
### CMS "Cosmic Challenge"

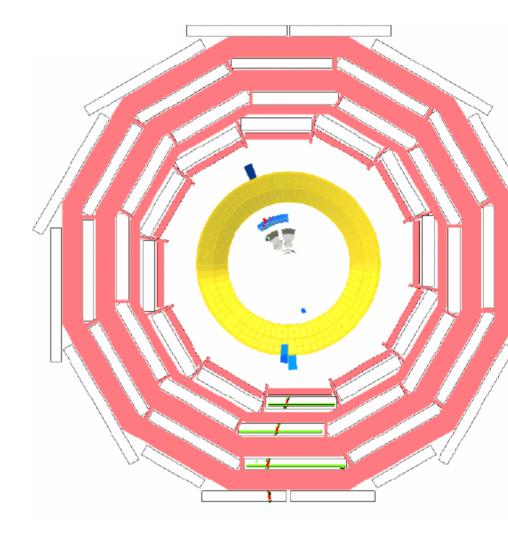






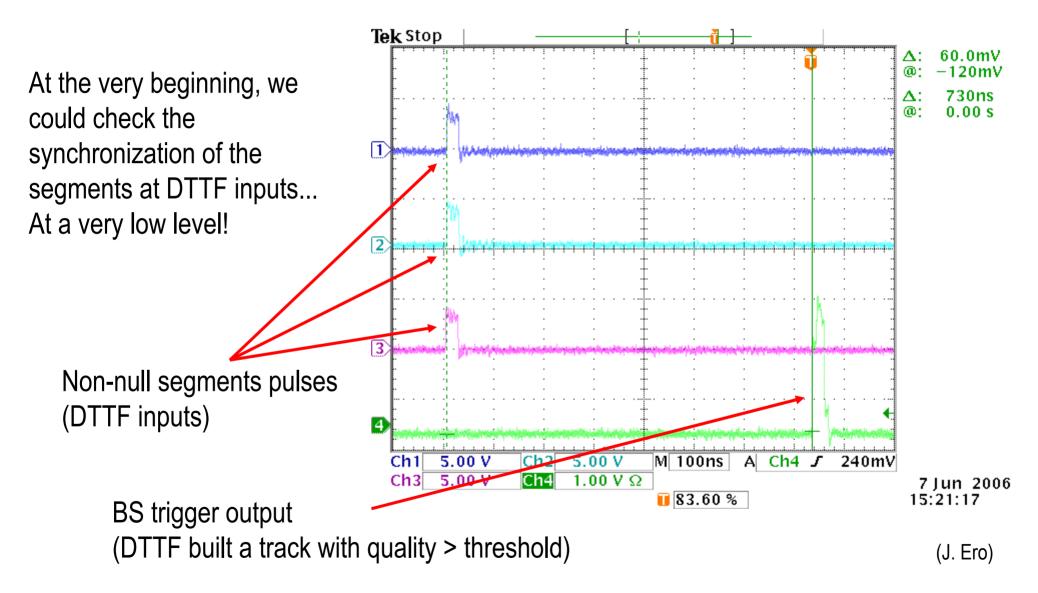
### CMS "Cosmic Challenge"



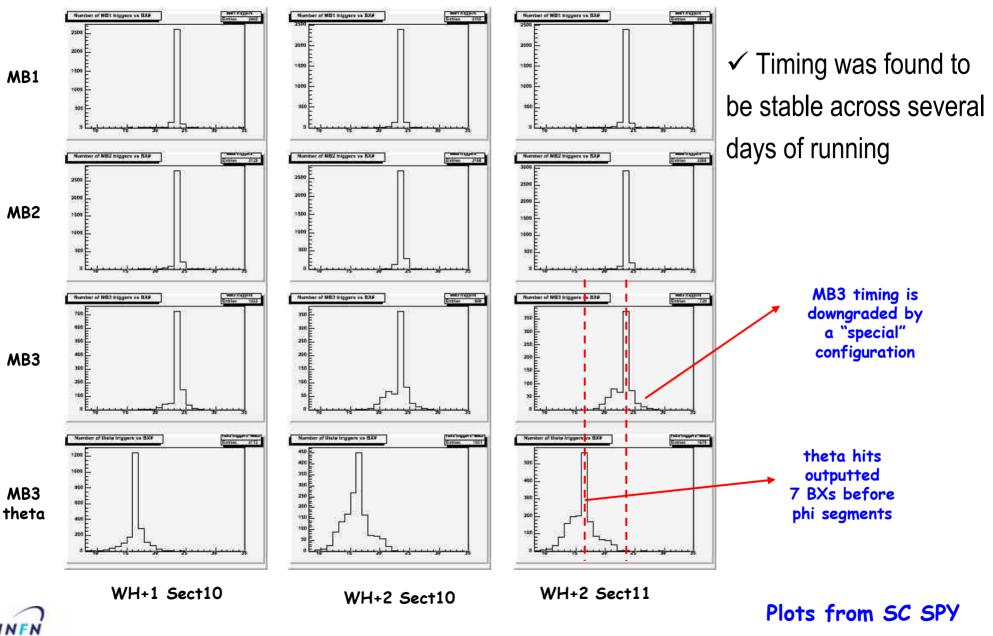




# SC synchronization – 1: scope



### SC synchronization – 2: spy data plots

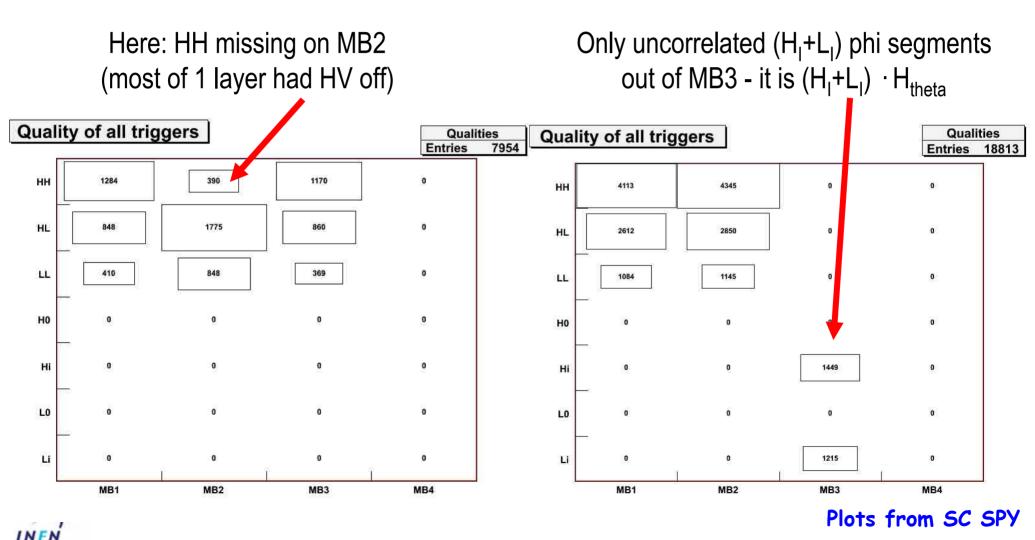


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# Monitoring with SC spy – trigger primitives quality

"Default" configuration: Only correlated (HH+HL+LL) segments

"Pointing" configuration:



# Summary

- The DT Sector Collector and Muon Sorter systems have been implemented with several FPGAs technologies
- Tools for remote monitoring and configuration have been developed and validated
- Exahustive dynamic tests of all the hardware have been used to validate the designs and the produced boards
- Integration tests validated the whole system architecture
- In CMS "Cosmic Challenge" in August 2006 a full slice of the CMS detector was integrated and run on cosmic muons
- A complete slice of the DT Trigger system was integrated and operated reliably and proved good stability, millions of cosmics were triggered
- During the Cosmic Challenge the spying and monitoring tools were extensively used to check on-line and quasi-automatically the system performance



### End....

### backup slides following



# LHC: cross sections and rates

- Start in 2007
- *pp* collider reaching  $\sqrt{s} = 14 \text{ TeV}$
- Design luminosity is  $L = 10^{34} \text{ cm}^{-2} \text{s}^{-1}$
- The total cross-section at this energy is about  $\sigma \approx 70 \text{ mb}$

corresponding to an interaction rate

~ 700 10<sup>6</sup> events/s

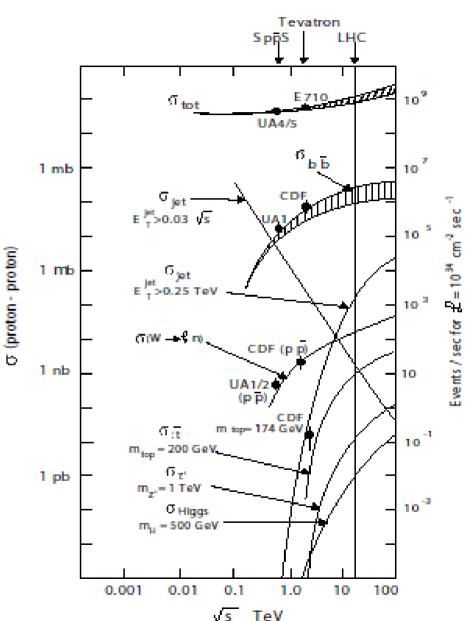
at a crossing frequency of

# 40 MHz

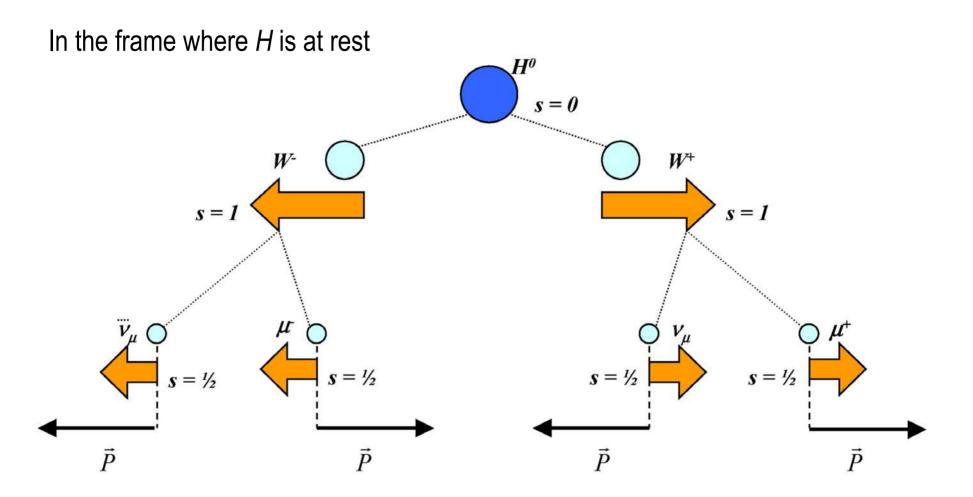
• Very good selectivity needed, i.e.

 $\sigma_{HiggsSM} \sim 1 \text{ pb}$ 

 $\rightarrow$  need a selectivity ~ 1:10<sup>11</sup>



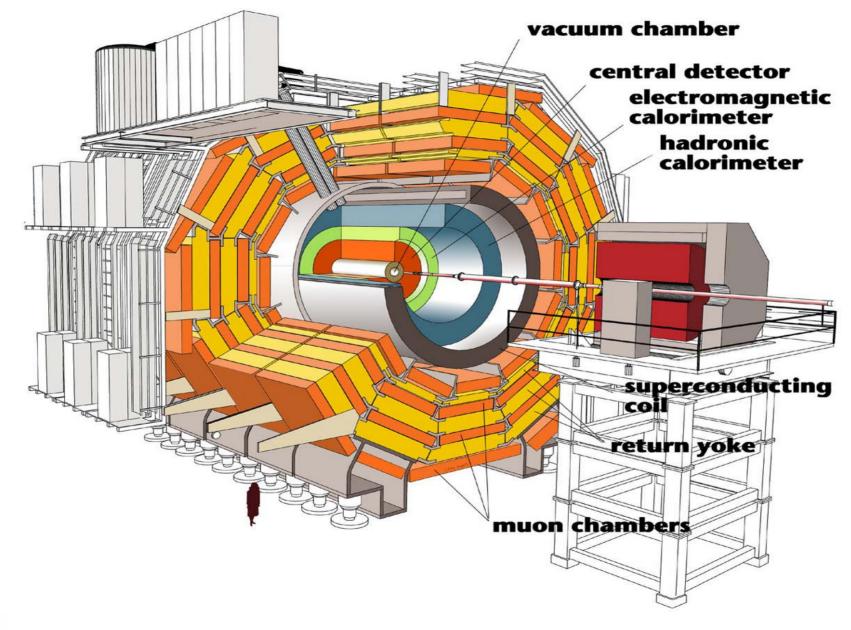
# Spin correlation



Definite elicity of neutrinos  $\rightarrow$  same direction of  $\mu$  momentum



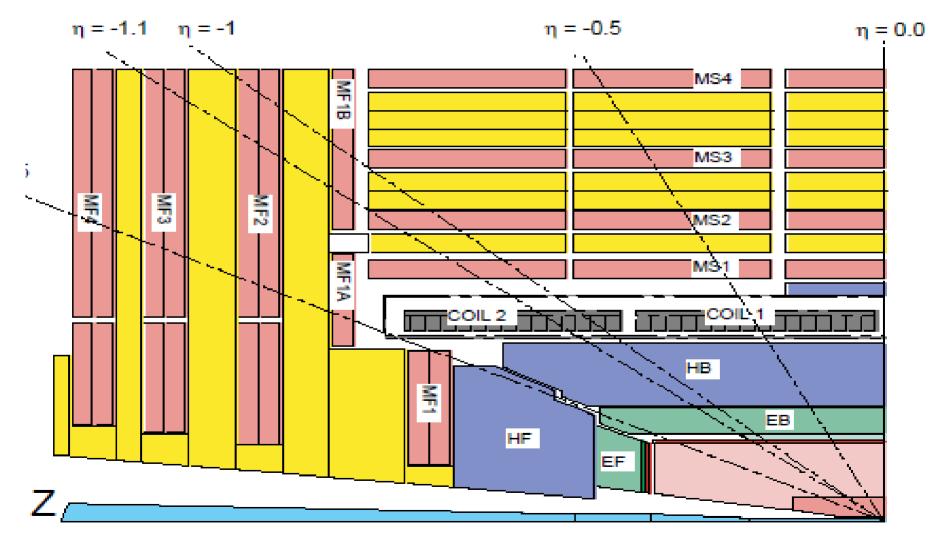
#### CMS detector





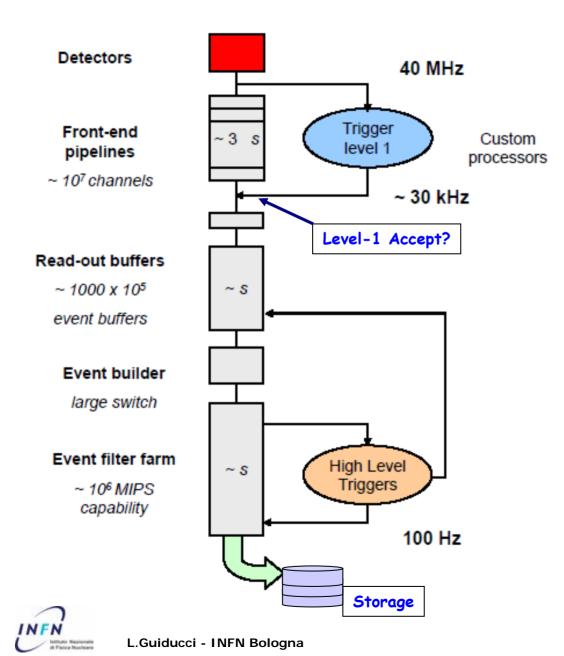
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#### Muon Detectors transverse view





# Trigger system overview

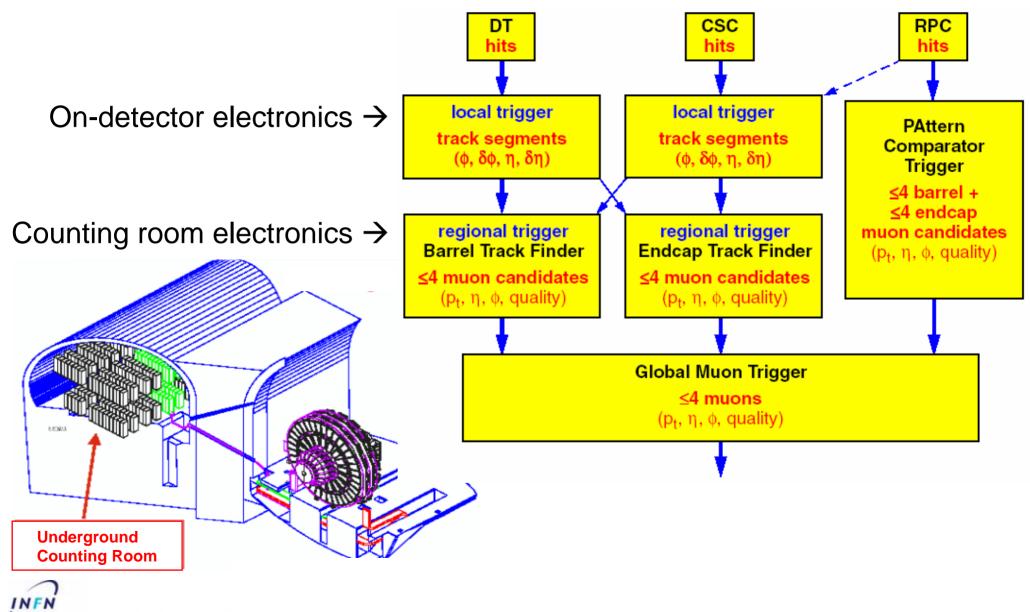


 On-line reduction from interaction rate (~700 MHz) to storage rate (~ 100 Hz)

Trigger chain based on 2 levels

- Level-1
  - $\rightarrow$  custom processors
  - $\rightarrow$  muon and calorimeters
  - → pipelined (sync. 40 MHz)
  - $\rightarrow$  no dead-time
  - $\rightarrow$  3.2 µs overall latency
- High level
  - $\rightarrow$  Software on CPU farm
  - $\rightarrow$  ~ s latency

# Level-1 Muon Trigger overview



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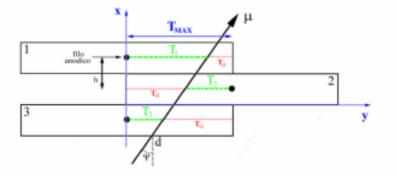
#### Meantimer

$$T_1 = \frac{1}{v_{drift}} \left( d + \frac{5}{2}h\tan\psi \right)$$
$$T_2 = T_{MAX} - \frac{1}{v_{drift}} \left( d - \frac{3}{2}h\tan\psi \right)$$
$$T_3 = \frac{1}{v_{drift}} \left( d + \frac{1}{2}h\tan\psi \right)$$

Thus,

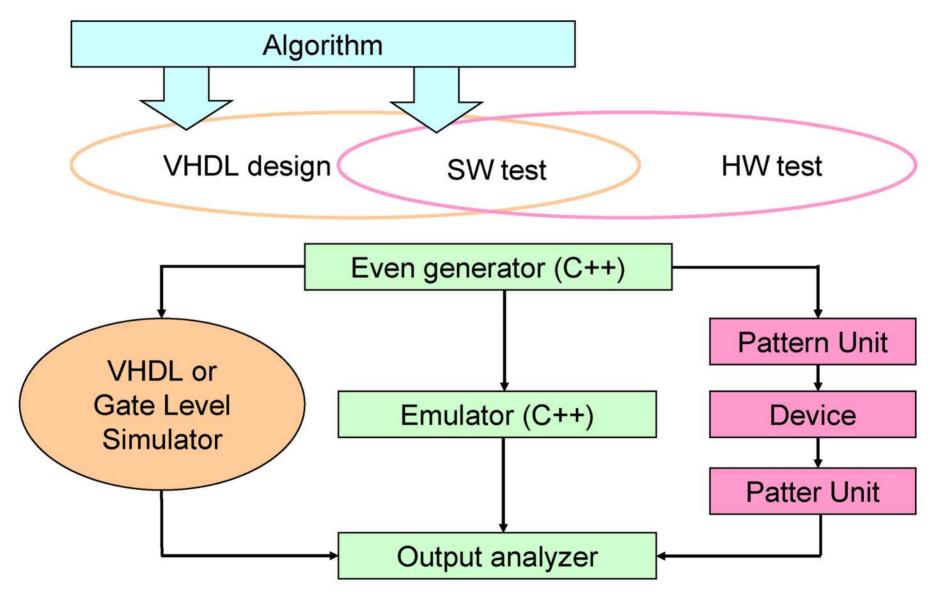
$$\frac{T_1 + 2T_2 + T_3}{2} = T_{MAX}$$

i.e. after a constant time  $T_{MAX}$  from the bunch crossing in which a muon originated, three hits from the muon track satisfy that alignment relation (see BTI in section 2.3.1). That means the muon parent BX can be unambiguously identified. However this technique imposes severe constraints



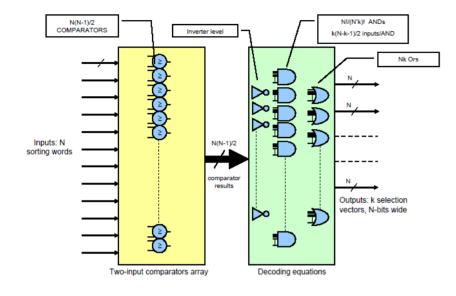


### Design Method



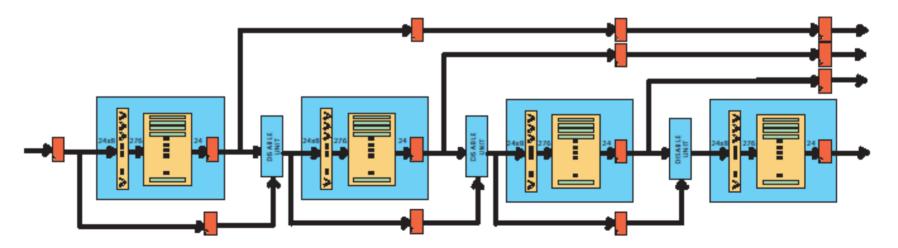


### Parallel Sorting Algorithms



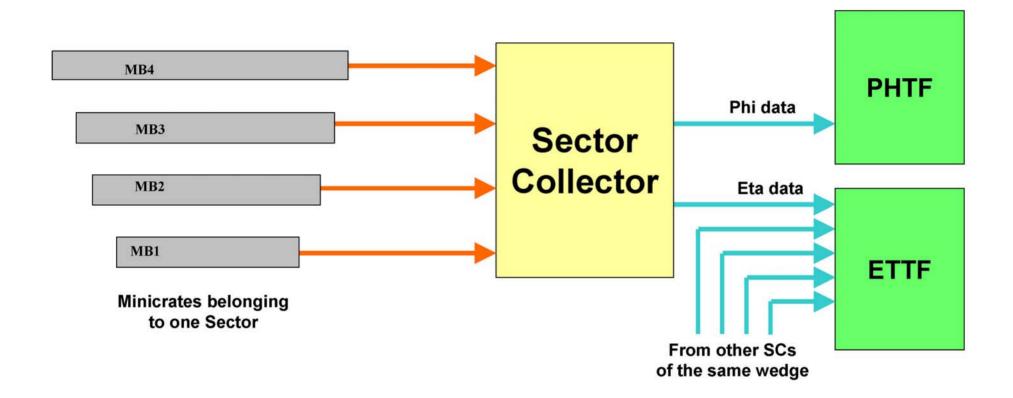
Fully parallel sorting: logic routing complexity increases with factorial dependence on the number of candidates to sort

Hybrid sorting: sequential usage of a (simpler) parallel sorting block



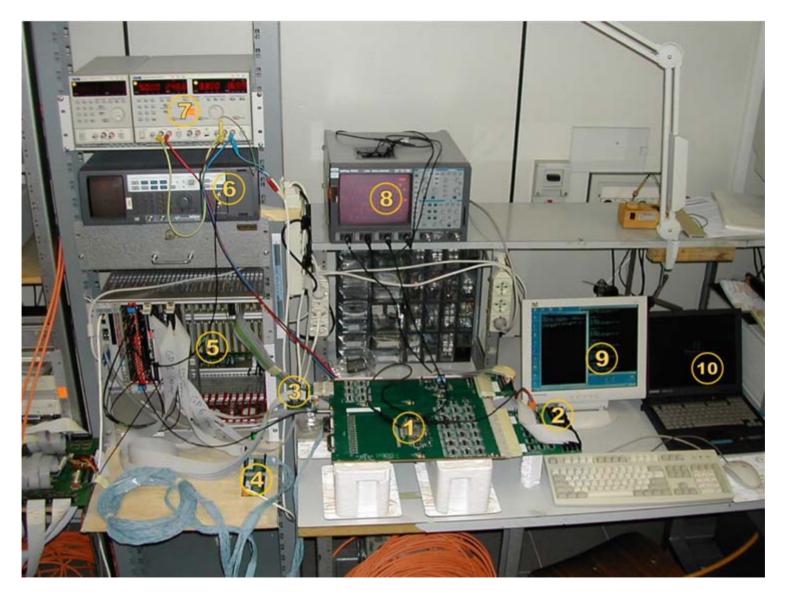


### Sector Collector Block Scheme



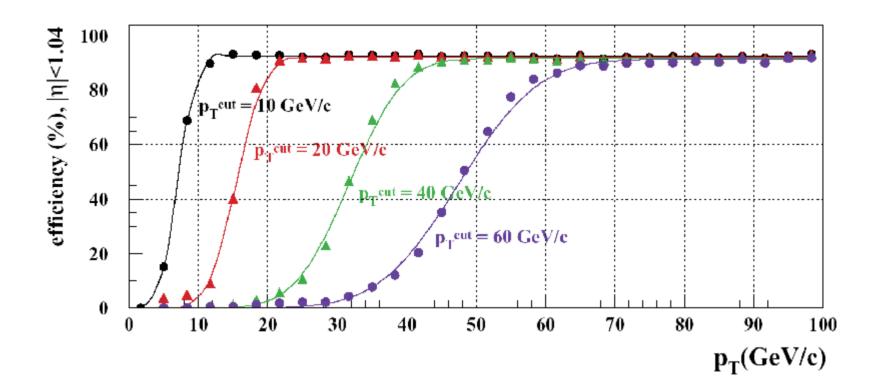


### Wedge Sorter stand alone test setup





#### Turn-on curves for several Pt cuts





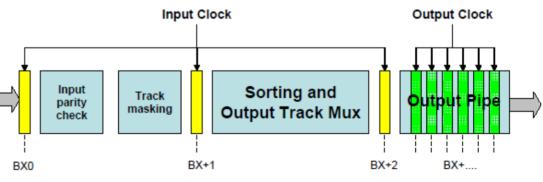
# Sector Collector – ProAsic firmware designs

Motherboard Controller

- VME interface
- Power control and monitoring of the RX- and TX- mezzanines
- Adjustment and monitoring of 8 different clock domains (4xRX, 1xTX, 1xDAQ, 2xinternal)
- Data quality is continuosly checked and reported to slow control
- Link state is monitored
- Spying of trigger data with several trigger sources
- 5 independent sector trigger outputs as logic of minicrate auto-triggers
- Optical transmission control (link resynchronization, status)

LVDS Receiver

- Input links status monitoring
- Data parity checks
- Sorting of track segments
- Output configurable pipeline for alignment with the other LVDS-RX of the sector



### Bit error rates from tests

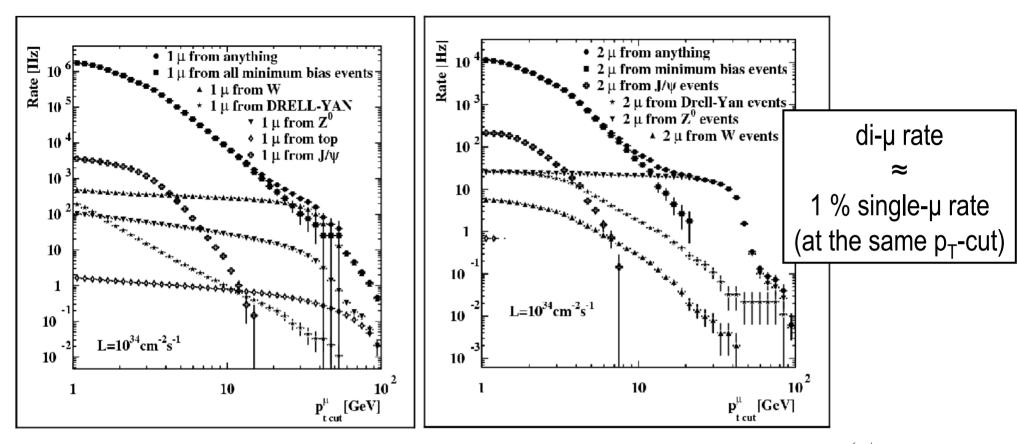
#### Binomial distribution, with large N (number of patterns) and no errors detected:

ER = - ln(1-CL)/N

Cable transmission tests	BER < 2 10 <sup>-12</sup>
Prototype boards tests	BER < 2 10 <sup>-9</sup>
Production boards tests	BER < 2 10 <sup>-6</sup>



### Expected muon rates



Interest in dimuon trigger:

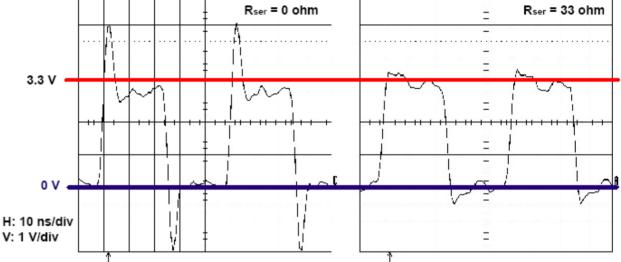
- Physics channels with dimuons in final state
- Several processes generate muons near in space

$$H \rightarrow ZZ^{(*)} \rightarrow 4 \ l$$
$$H \rightarrow WW \rightarrow l \ v \ l \ v$$
$$H, A, h \rightarrow \mu\mu$$

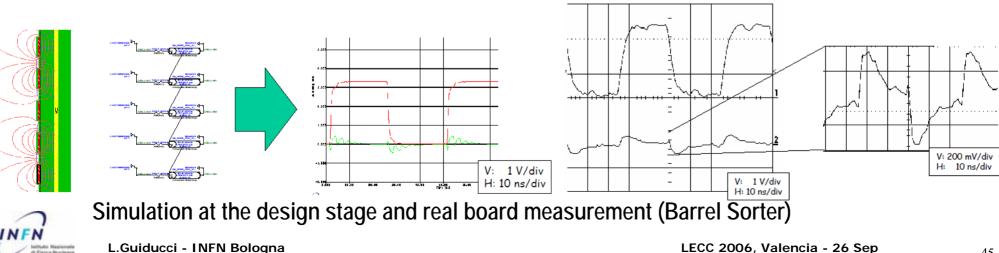
# Signal transmission issues

• On large boards, with long signal traces, signal transmission quality issues may generate sporadic bit errors

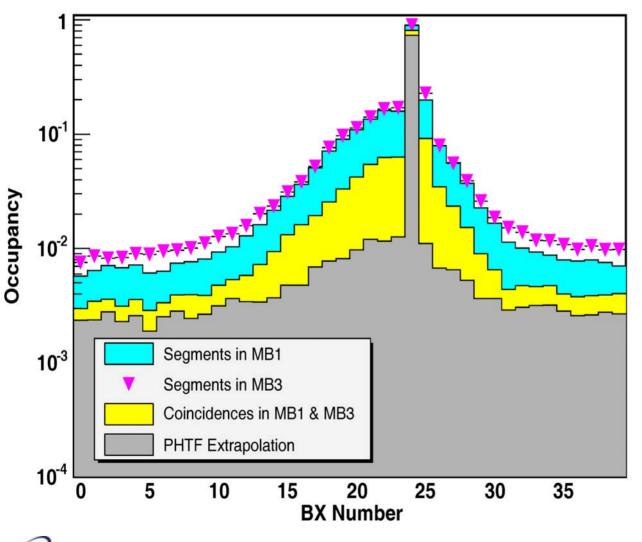
• Careful line termination removes signal reflections and improves transmission quality



• Lines in long and dense busses can be subjected to cross-talk problems



#### Test Beam – some result



Bunch crossing (BX) distribution of tracks found by DTTF

BX Identification:Out-of-time triggerssuppressed at < 1%</li>

• 99 % efficiency on high quality local trigger segments

• 94 % inclusive efficiency