Design and Test of the Off-Detector Electronics for the CMS Barrel Muon Trigger

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Abstract

Drift Tubes chambers are used in the CMS barrel for tagging the passage of high Pt muons generated in a LHC event and for triggering the CMS data read out. The *Sector Collector* (SC) system synchronizes the track segments built by trigger modules on the chambers and deliver them to reconstruction processors (*Track Finder*, TF) that assemble full muon tracks. Then, the *Muon Sorter* (MS) has to select the best four candidates in the barrel and to filter fake muons generated by the TF system redundancy. The hardware implementations of the Sector Collector and Muon Sorter systems satisfy radiation, I/O and fast timing constraints using several FPGA technologies. The hardware was tested with custom facilities, integrated with other trigger subsystems, and operated in a beam test. A test beam on a 40 MHz bunched beam validated the local trigger electronics and off-detector prototype cards and the synchronization tools. The CMS Magnet Test and Cosmic challenge in 2006 proved stable and reliable operation of the Drift Tubes trigger and its integration with other trigger systems and with the readout system. Constraints, design, test and operation of the modules are presented.

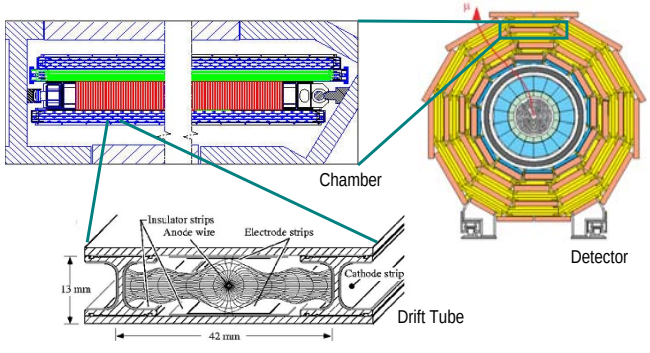

Figure 1: Schematic view of the DT detector

I. The Drift Tubes Muon Trigger

The aim of the muon system [1] is to provide a robust trigger, with bunch crossing assignment, identification and momentum estimation of the muons produced in the p-p collision in a wide Pt range. The system is embedded in the return yoke of the magnet, and the bending given by the magnetic field inside it is used to provide a Pt assignment for muon tracks. Drift Tubes (DT) detectors are used in the barrel region.

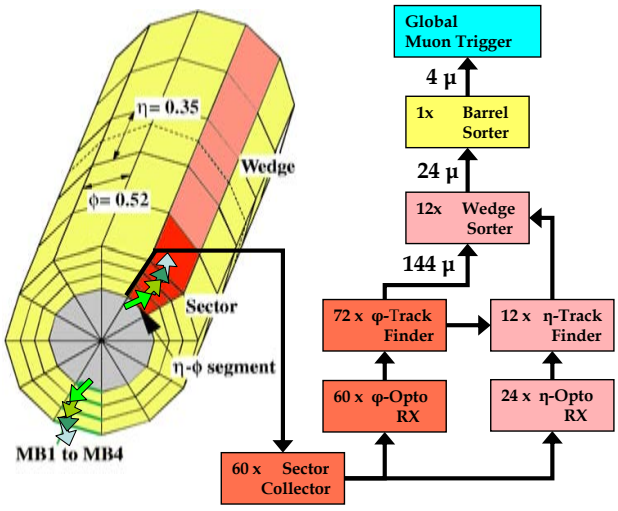

Figure 2: Left: sketch of the DT detector as it is partitioned for the off-detector electronics. Right: block scheme of the Sector Collector and regional trigger system.

The DT system is segmented in 5 *wheels* along the z direction, each about 2.5 m wide and divided into 12 azimuthal *sectors*, covering $\sim$30° each. A cross section of a wheel is shown in Fig. 1: DT chambers are arranged in 4 concentric cylinders - called *stations* - within each wheel, at different distance from the interaction point, and interleaved with the iron of the yoke. Each DT chamber is instrumented with staggered layers of drift tubes in the transverse (r, ϕ) plane and in the longitudinal (θ, z) plane and it is equipped with trigger electronics consisting of several modules. This *local trigger* electronics [2] is able to identify tracks crossing the station, assigning collision from which the particles originated [3] and the impact postion, together with the angle of the tracks with respect to the radial direction, providing a measument of the bending of the muon. As it is sketched in Fig. 2, local trigger data are sector-wise collected on the towers near to the detector by Sector Collector cards where the timing from different channels is adjusted to account for time of flight and cable lengths. One sector is linked by one SC card, thus 60 SC boards are needed. Segments are sent to the underground counting room using optical links and delivered to the *regional trigger* where Track Finder cards run an extrapolation and matching algorithm in order to build full muon tracks and to measure their transverse momentum [4]. In the right part of Fig. 2 a block scheme of the regional trigger is shown: the numbers of modules are shown inside each block, while near to the connecting arrows the maximum number of muons that are

processed at each step is shown. The colors help understanding how the system is partitioned: each Track Finder module operates on one sector of the DT detectors and the large number of muon tracks (up to 144) that can be potentially found is analyzed wedge- and barrel-wise by the Muon Sorter cards, that run a ghost suppression algorithm and finally sort up to four muon candidates from the whole barrel.

In the following sections, details about implementation, test and integration of the Sector Collector and Muon Sorter systems will be given.

II. The Sector Collector

The Sector Collector (SC) is a VME 9U board installed on tower crates, near to the CMS detector itself [6]. Its main task is to collect from one sector of the DT detector the local trigger data, received in high-speed (480 Mb/s) LVDS [5], and trasmit them on optical fibers to the counting room.

A. Receiver cards

The SC design has been split in several sub-units. In Fig. 3 a picture of a receiver mezzanine is shown. This mezzanine can receive the trigger data from one chamber, performing the deserialization and some data processing and monitoring. On the right side, the FTP cables are connected. The numbers help identifying the main components: cable equalizers (1), deserializers (2) and a flash-based FPGA ProAsicPlus from Actel (3). A flash-based FPGA was chosen due to its intrinsic radiation hardness (with respect to a SRAM-based FPGA), since the SC boards will be installed in the undergroun experimental room, where low-energy neutrons may flip SRAM configuration bits leading to functionality interrupts [7]. Flash configuration memory is more robust to low energy ionization events in the silicon, ensuring an interruption-free operation [8, 9].

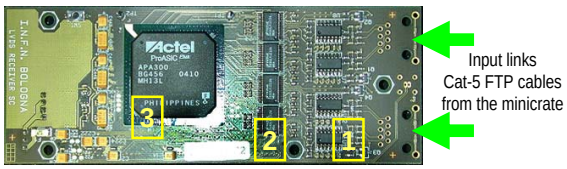

Figure 3: The LVDS receiver mezzanine. The main components are labelled with numbers (see text).

The FPGA on the receiver mezzanine has several tasks: it checks the data integrity, through deserializers status monitoring and data parity calculation; it sorts the highest quality ϕ segment if more than one is received at the same bunch crossing; it handles test features that are useful to synchronize the system and to test the connections with the main board.

B. Optical transmission card

The data from each receiver mezzanine are fan-out to the host motherboard (Fig. 6), where an optical transmission mezzanine is plugged. A picture of the optical transmission card is shown in Fig. 4. The main components are a clock filtering and fanout circuit based on a QPLL [10], and six GOL chips serializing data at 1.6 Gb/s using the Gigabit Ethernet protocol [11]. The serialized data are sent to the undeground counting room over multimodal fibers ($\sim$ 70 m) at 850 nm using VCSELs from Honeywell. Fig. 5 the *eye pattern* seen on the receiver board after electrical conversion, together with measurements of the eye opening that allow the bit error rate from the signal shape to be estimated less than 3×10^{-14}.

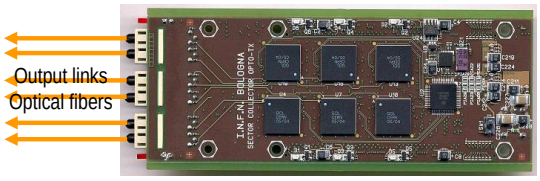

Figure 4: The optical transmission mezzanine.

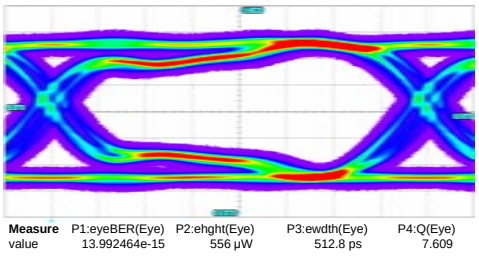

Figure 5: The eye pattern seen on 1.6 Gb/s serialized data.

C. SC Motherboard

In Fig. 6 the SC motherboard is shown. Only receivers mezzanines for the MB1 and MB2 chambers and the optical transmission mezzanine are plugged in this picture. The device indentified by (6) is a further ProAsicPlus device, called controller chip, that implement the VME interface of the board and several bridges to other interfaces. A JTAG chain [13] connects the receiver mezzanines FPGAs, while a I2C interface allows the GOL chips to be monitored and configured, as well as current limiters, temperature sensors and laser monitoring to be accessed. The synchronization of the system is monitored accessing parity error counters and controlling clock phases using independent delay lines (8, 9). A spy system is implemented on the controller chip. Each receiver mezzanine sends to the controller chip a subset of the trigger data flow that is written on FIFO buffers. The spy data allows the timing of the triggers from the (r, ϕ) and (θ, z) planes of the DT chamber to be monitored, together with the quality of the local track segments. The FIFO write process can be controlled by central triggers (level-1 accept) or by a self-generated trigger, expressed as a logic function of single chamber triggers. The spy data can be sent to the DT readout electronics [12] through a dedicated inteface

(10) or accessed locally through VME.

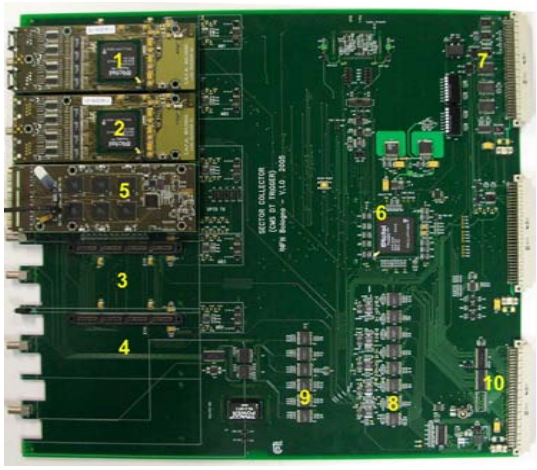

Figure 6: The motherboard, only LVDS receiver mezzanines for MB1 and MB2 and opto transmission mezzanine are plugged.

D. Optical receiver card

In Fig. 7 a picture of the optical receiver board is shown. The main components are labelled by numbers: PIN diodes and amplifiers converting the optical power into electrical signals (1); a FPGA (Altera StratixGX) hosting embedded deserializers, which also checks the data integrity (2); and output buffers, delivering parallel data to the corresponding $\phi(\eta)$-Track Finder [14] board (3). In The main FPGA is designed with a custom JTAG interface, driven by the corresponding Track Finder board, to access internal status information about the data integrity and to drive test modes. The same boards are used for the $/phi$ and the η parts of data, with the main FPGA firmware built in two versions.

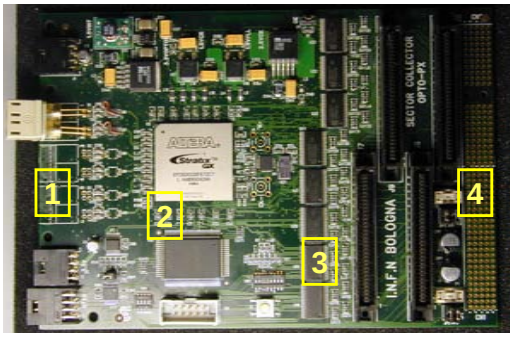

Figure 7: The opto receiver board. The main components are labelled with numbers (see text).

III. The Muon Sorter system

As it is shown in Fig. 2 the Muon Sorter is split in two consecutive processing steps, performed by the Wedge Sorter modules and by a single Barrel Sorter board. All boards are VME 9U, where the interfaces and the main processing units have been designed using S-RAM FPGAs [6].

A. The Wedge Sorter

Each Wedge Sorter receives up to 12 muon candidates from the Track Finder modules operating on the five sectors of a wedge, and selects the two "best" candidates, with an overall I/O of about 450 parallel signals at 40 MHz. A picture of the board is shown in Fig. 8. Two FPGAs from Altera are used to implement the VME interface of the board (Acex1k FPGA, 2) and the main computational part (Apex20k FPGA, 1).

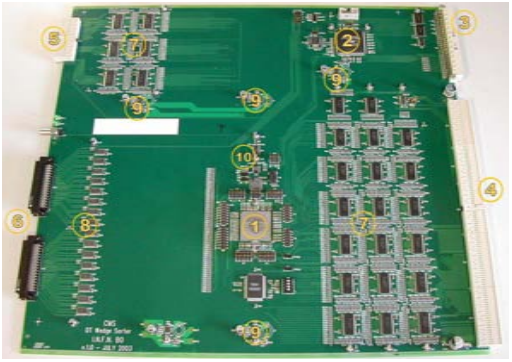

Figure 8: The Wedge Sorter board.

On the latter, a ghost busting algorithm is able to identify if consecutive track finder modules delivered two copies of the same physical track, to reduce the rate of these "false dimuon" events. An example of false dimuon reconstruction is shown in Fig. 9, where a longitudinal section of the muon system is shown: the two muons cross consecutive sectors, and both are reconstructed twice by independent Track Finder processors [15]. Using information about the segments used to build the tracks, the ghost busting algorithm identifies common segments and cancels the worst quality (i.e., built with less and outer segments) track of each pair [16]. The sorting algorithm is fully parallel, and can sort the two "best" tracks (highest reconstrucion quality, highest transverse momentum) out of twelve input tracks in less than 50 ns.

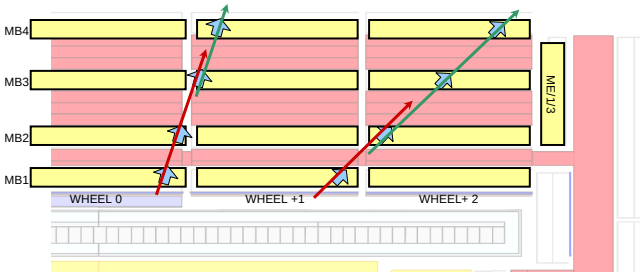

Figure 9: Example of fake track generation by the partitioning of the Track Finder system. A longitudinal section of the the muon detectors is shown.

B. The Barrel Sorter

Outputs from 12 Wedge Sorter are sent in parallel LVDS on twisted pair cables to the Barrel Sorter board, which is shown in Fig. 10.

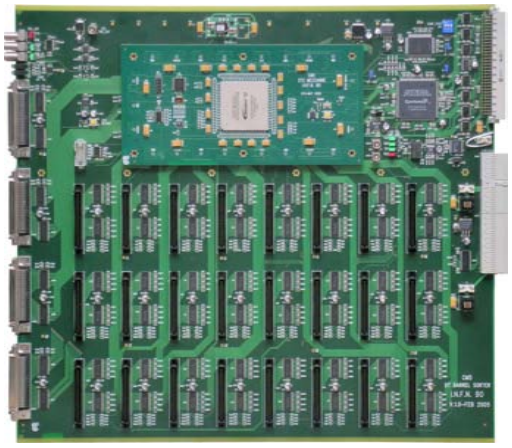

Figure 10: The Barrel Sorter board.

This board performs the final ghost busting and selection over the full sample of 24 muon candidates from the previous stage, with an impressive parallel I/O of about 900 bit at 40 MHz (∼36 Gb/s). Also in this board, two FPGAs are present: a VME interface, implemented on an Altera Cyclone, with a full VME speed parallel bridge to the main FPGA, an Altera StratixII in a 1508 pin BGA package, mounted on a mezzanine board. The main processing unit performs the ghost busting and sorting within 75 ns. To satisfy this latency requirement a mixed parallel/serial approach was chosen for the sorting algorithm, with an internal pipeline running at twice the I/O frequency (i.e., at 80 MHz). Moreover the main FPGA contains FIFOs with VME access to spy the full I/O of the trigger data. The device can also drive an external trigger, based on programmable conditions, like thresholds on track qualities.

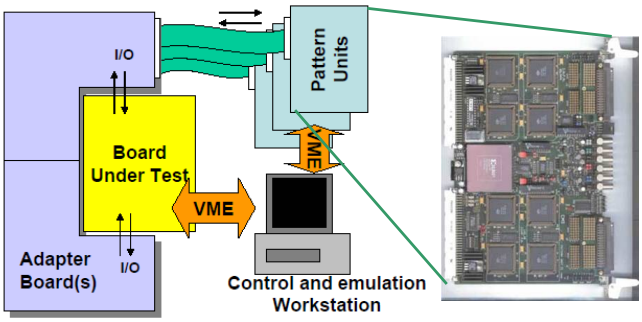

Figure 11: Sketch of a generic test bench: a workstation controls a VME system with Pattern Units, that are itnerfaced to the device under test by adapter boards. On the right, the picture of a Pattern Unit.

IV. Test of the Electronics

The produced electronics, both at the prototyping and at the final production stages, undergo severe tests to verify the functionalities. The tests are both stand-alone, to qualify the single card, and integrated, to check a more complex chain of several modules.

A. Stand-alone tests

In the left side Fig. 11, the sketch of a stand alone test bench is shown. The approach shown in the picture has been followed in all the test benches that validated prototype and production boards. The key component of this test bench is the *Pattern Unit* (PU), shown in the right side of the figure. This is a custom VME 6U I/O board, based on FIFO memories and provided with a VME interface, able to receive/drive up to 128 I/Os at up to 100 MHz [17]. These cards can be run in parallel, allowing to run workstation-controlled tests of devices at their full speed injecting millions of random or specific patterns. For this purpose, adapter boards are built, in order to match the form-factor or the electrical standard of the device under test. On the workstation an emulator is run, in order to verify bit by bit the response.

B. Integration tests

Stand-alone test benches can then be mixed both in hardware setup and in software emulation in order to perform integration tests, i.e. to test a complete Sector Collector system or to test the WS to BS connection. The spy tools embedded in the designed FPGAs are useful in integration tests and in real life operation. In Fig. 12 the integration of Track Finder and Muon Sorter test setup is shown. On the left side, a block diagram shows the data flow. VME Test Boards inject data in the Track Finder boards, and the data flow thorughout the system is spied at several levels up to the last module.

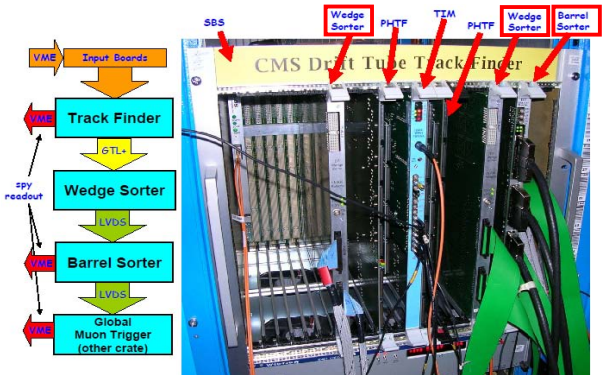

Figure 12: DTTF-WS-BS integration test.

V. CMS Cosmic Challenge

The CMS detector, currently being assembled at surface, was intensively tested with cosmic muons during the first magnet test runs. This "Magnet Test and Cosmic Challenge" (MTCC) setup is shown by the event display reported in Fig. 13.

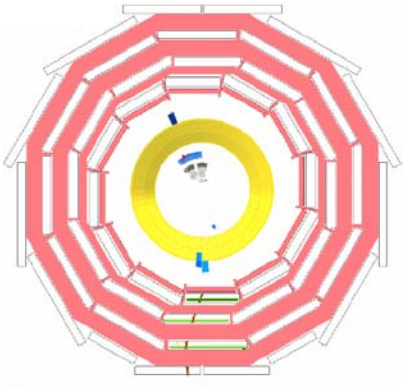

Figure 13: MTCC event

A full "slice" of the CMS experiment was integrated: three sectors of DT detectors were synchronized and triggered cosmic muons, with the readout system including calorimeters and the trackers. The DT trigger was generated by the Barrel Sorter board, on which a quality threshold was applied to tracks built by the Track Finder. In the event shown, a muon (bended by the magnetic field inside the superconducting solenoid and in the yoke iron) was triggered by the DT detectors, in the lower part of the detector; the track can be backward followed to see that also HCAL, ECAL and the Trackers had hits. The DT trigger chain was based on three sectors of the detector, using the three inner chambers on each sector. In Fig. 14 some plots from the Sector Collector spy system are shown. Each plot shows the number of track segments found versus the segment bunch crossing number. On each column, the plots from the three chambers of one sector (i.e., one Sector Collector board) are shown. This kind of data allows the relative synchronization of the different detector partitions to be checked quickly and reliably.

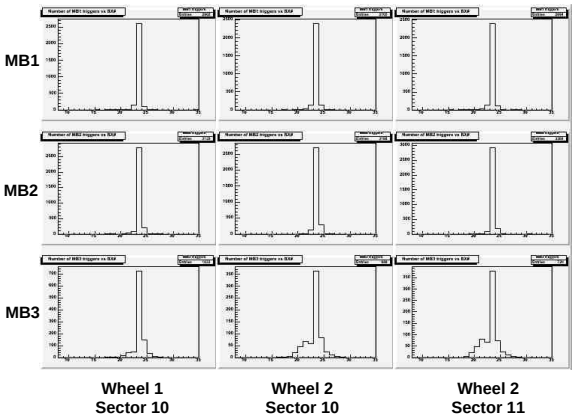

Figure 14: 3 sectors x 3 chambers synchronization plots from MTCC (SC SPY).

VI. Summary and conclusions

A general overview of the CMS DT muon detectors and trigger system was given. The main tasks and design features of several off-detector components of the trigger electronics were described with some implementation details. The electronics is based on custom FPGA designs, implementing the trigger algorithms and useful test and data spy features. The modules were tested in their working conditions using setups based on custom I/O units. Integration tests and the CMS Magnet Test and Cosmic Challenge were the final integration test bench that proved the correct and reliable operation of the DT trigger system.

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