

Time Resolution of a Few Nanoseconds in Silicon Strip Detectors Using the APV25 Chip

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Abstract

The APV25 front-end chip for the CMS Silicon Tracker has a peaking time of 50 ns, but confines the signal to a single clock period (=bunch crossing) with its internal “deconvolution” filter. This method requires a beam-synchronous clock and thus cannot be applied to a (quasi-) continuous beam. Nevertheless, using the multi-peak mode of the APV25, where 3 (or 6,9,12,...) consecutive shaper output samples are read out, the peak time can be reconstructed externally with high precision. Thus, off-time hits can be discarded which results in significant occupancy reduction. We will describe this method, results from beam tests and the intended implementation in an upgrade of the BELLE Silicon Vertex Detector.

I. INTRODUCTION

In today’s high energy physics experiments, silicon strip detectors are typically used to measure particle tracks thanks to their good spatial resolution. The original detector signal also provides very precise timing, but this information is lost with the common architecture of a shaping front-end amplifier with a single sampling point. However, preserving the time information can be essential for tracking in future experiments with high particle density and frequency, such that detected hits can unambiguously be associated to each other and to a certain point in time, thus allowing to discard all hits which do not belong to the event of interest. Such a procedure would allow significant reduction of data on-line, and hence ease computing, storage and off-line efforts.

The potential application of a silicon strip detector with time information ranges from upgrades of existing systems to new detectors such as the ILC. In particular, this work was performed in the framework of the BELLE experiment at KEK (Tsukuba, JP). Its present Silicon Vertex Detector (SVD2) [1] is facing the limits imposed by the slow front-end amplifier with a shaping time of 800 ns, which causes an occupancy of about 10% in the innermost layer at the present luminosity of about $1.6 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$.

II. THE APV25 FRONT-END CHIP

The APV25 [2] was developed for the CMS experiment at the LHC. It is manufactured in a $0.25 \mu\text{m}$ CMOS process and tolerates up to 100 MRad of radiation. The APV25 is designed for operation at 40 MHz with a default shaping time of 50 ns (adjustable between 35 ns and 200 ns) and has an analog pipeline of 192 cells depth for each of the 128 input channels, where sampled values of the shaper output are stored at the beam synchronous clock frequency of 40 MHz.

A “deconvolution” analog pulse shape processor [3] (switched capacitor filter) is included on the chip which creates

a weighted sum of three consecutive samples. This results in a narrowed output pulse which is (ideally) just a single clock wide, and hence the measured signal can unambiguously be assigned to a certain bunch crossing of the clock synchronous LHC beam. This gain in time resolution is traded off against a higher noise figure.

The “deconvolution” method requires shaper output sampling (APV25 clock) which is synchronous to the bunch crossings, as it is the case at CMS. In other experiments with a (quasi-) continuous beam such as BELLE, this feature does not work, since the APV25 sampling is always clock-synchronous and also its trigger input is synchronized internally. However, the APV25 also offers the functionality to read out three consecutive samples without processing. By repeatedly sending a trigger pulse in this “multi-peak” mode, one can read out up to 30 consecutive samples of the shaper output, spaced by the clock period of 25 ns.

III. PEAK TIME DETERMINATION

Peak time and amplitude can be obtained by applying a fit function to the sampled shaper output values. Fig. 1 shows a typical event with twelve samples, where two different fit functions were applied: The function

$$v_{\text{out}} = A \frac{t}{T_p} e^{-\frac{t}{T_p}}, \quad (1)$$

denoted “Exp fit”, is the output of an ideal CR-RC shaper with the shaping time T_p , but the actual output slightly deviates from this waveform, particularly in the rising edge and the tail. Hence, another fit was performed with the waveform obtained by internal calibration of the APV25, where the measured points were connected with cubic splines (“IntCal fit”), which yields better fit results.

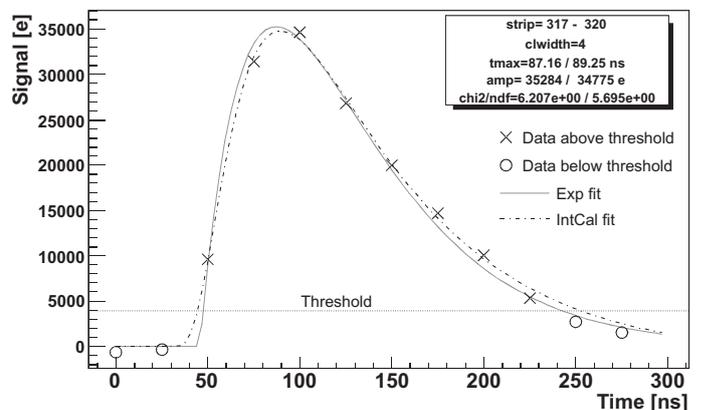


Figure 1: Sampled shaper output values with two different fit functions applied. See text for details.

The actual shaping curve depends on the capacitive load at the input (i.e. the detector geometry) and the bias settings of the front-end amplifier, which can be adjusted in a wide range. Thus, the waveform can be tuned to achieve shaping times between 35 and 200 ns. Clearly, this has implications on power consumption, signal-to-noise and achievable timing precision. All results shown here were performed with the default shaping time of 50 ns for which the APV25 was designed.

IV. TEST SETUP

Two different detector modules were built for studying the peak time finding. Both use double sided silicon detectors designed for BELLE SVD upgrades. The “UV striplet” [4] type is a candidate for the innermost part of the SVD3 which is a conceptual design for Super BELLE. It has short strips (10 mm) arranged at an angle of 45° against the edge. The strips on the opposite side are rotated by 90° to achieve stereo measurement. The thickness of this sensor is $300 \mu\text{m}$, and it has AC coupled strip implants with $51 \mu\text{m}$ readout pitch on both surfaces. On the p-side, an intermediate floating strip is located between each pair of readout strips, while the n-side readout strips are enclosed by an “atoll” type p-stop. Fig. 2 shows one side of the sensor-hybrid assembly with four APV25 chips on each side.

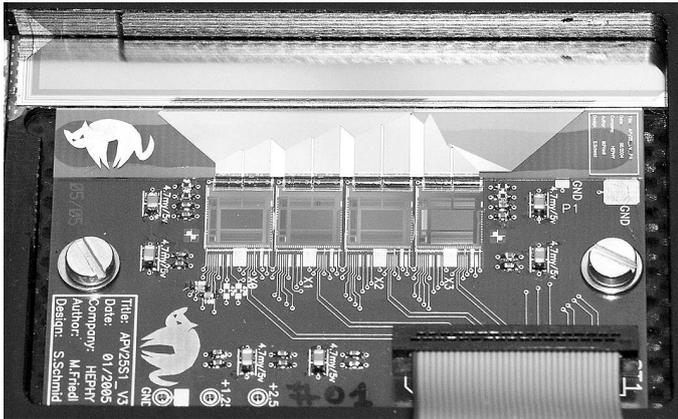


Figure 2: One side of the “UV striplet”-APV25 front-end assembly. The opposite side is an exact mirror image hidden by the support structure.

The other module is based on a bigger silicon detector (“DSSD”) which is very similar to the existing SVD2.0 and will be used in the intermediate SVD2.5 upgrade. Its dimensions are $80 \times 28 \text{ mm}^2$ with a thickness of $300 \mu\text{m}$. The p-side has long and dense strips ($51 \mu\text{m}$ readout pitch), while the n-side contains the same number of strips which are consequently short and wide ($152 \mu\text{m}$ readout pitch). Both sides are equipped with floating intermediate strips, and again “atoll” p-stops are used on the n-side.

The BELLE SVD consists of ladders composed of one or more sensors read out from the short edge which is also the boundary of the detector acceptance. Thus, the p-side readout is trivial because its strips are all accessible on the short edge. For the n-side however, there is no such option. The traditional solution is to use a fanout (or double metal layer) at an angle of

90° against the strips to guide each strip to the short edge. The length of the resulting lines ranges from (almost) zero to the full length of the sensor, thus introducing a considerable additional capacitance which increases the noise figure. It becomes even worse when concatenating two (or more) sensors.

In order to avoid this problem, a novel approach was chosen for the arrangement of the readout chips on the n-side. Those are mounted on a thin double-layer flex circuit which sits on top of the silicon sensor. A thin layer of Rohacell [5] is put between sensor and flex-hybrid for thermal and electrical insulation. The APV25 chips are thinned to $100 \mu\text{m}$ to minimize the material budget and carbon fiber pipes are used as a support structure and for cooling. The pitch adapter between sensor and the APV25 inputs is a part of the flex circuit. Since this technology requires a certain feature size, the lines are arranged on both layers of the flex in an alternating way. Fig. 3 sketches the cross-section of the module assembly.

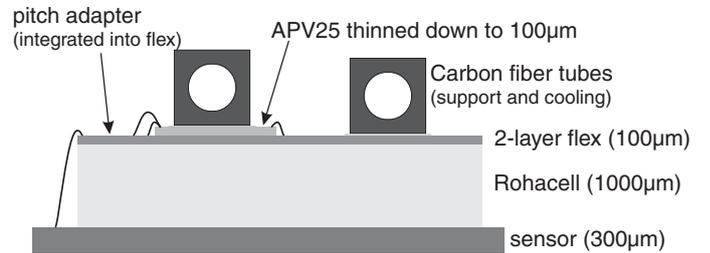


Figure 3: Schematic cross-section of the flex-hybrid module (drawing has different scales in x and y directions).

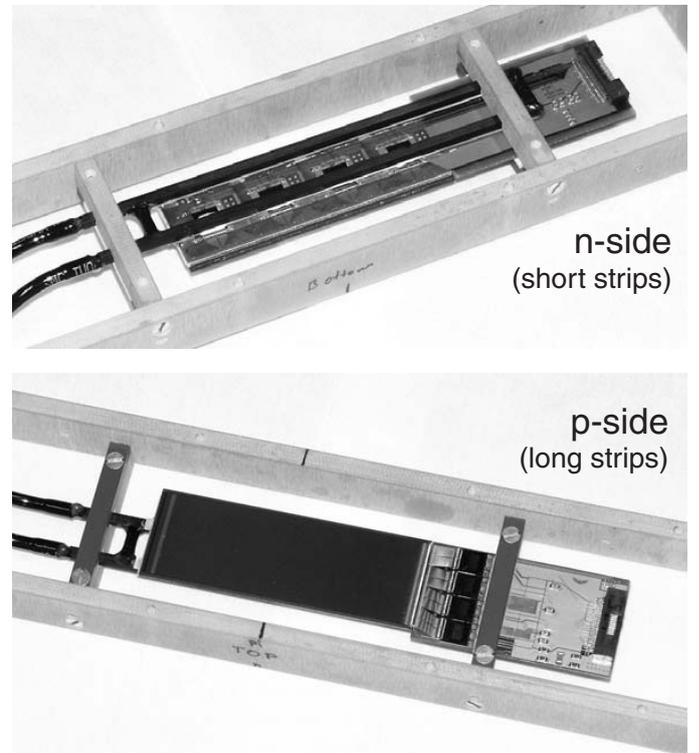


Figure 4: The two sides of the flex-hybrid module.

Fig. 4 shows photographs of the real module. While the n-side flex-hybrid is mounted on the sensor as described above, the p-side is read out from the side in a conventional way using the same type of flex-circuit, such that it could be put on top of the adjacent sensor in case of long ladders,

The detector modules were controlled and read out by the home-made “APVDAQ” system, consisting of a repeater board and a VME module for each hybrid. A floating power scheme is adopted on the repeaters, where the front-end local ground is connected to the bias voltage of the corresponding detector side. This method requires floating power supplies for each side and the translation of signals for both control and data, which is performed with optocouplers in case of slow signals (I2C and reset) and capacitors for fast signals (clock, trigger, analog data).

Since we measure several samples along the shaper output waveform, the data processing requires additional steps compared to the standard single-sample procedure. Analysis starts with the usual pedestal subtraction, common mode correction and zero suppression algorithms independently for each time slice. Then, a “clump finding” procedure is applied which is the extension of cluster finding in the space-time domain to determine contiguous hit blocks. The clump signals are summed up for each time slice, resulting in a curve as shown in fig. 1. Finally, a fit is applied to each curve, returning amplitude and time information.

V. EXPERIMENTAL RESULTS

The UV striplet module was tested in beams at KEK in April 2005 and four months later at PSI (Villigen, CH), where the DSSD module was also tested in August 2006.

The depletion voltages of the sensors were obtained by CV measurements and found to be 65 V for the UV striplet and 46 V for the DSSD sensors, respectively. A bias voltage scan in the KEK beam test confirmed the CV result for the UV striplet sensor. Throughout the tests described here, a bias of 80 V was applied to the sensors, which is the standard value used in the BELLE experiment and ensures full depletion.

The APV25 chips were operated at 40 MHz which was completely unrelated to the particle beam. Since the APV25 only accepts clock-synchronous triggers, a jitter of ± 12.5 ns, corresponding to the width of one clock cycle, is introduced by the synchronization of the scintillator/photomultiplier trigger signal. In order to obtain a reference time, the distance between the unsynchronized trigger and the next clock edge was measured by a TDC. The flat distribution of measured TDC values confirms the independence of beam and clock.

The “IntCal fit” (see section III.) returns two parameters, peak amplitude and peak time. By histogramming the fitted amplitudes, one gets the signal distribution which perfectly fits to a Landau shape, convoluted with a Gaussian component to account for electronic noise and (dominantly) intrinsic detector fluctuations [6]. Fig. 5 shows the signal distributions for both p- and n-sides of the UV striplet detector.

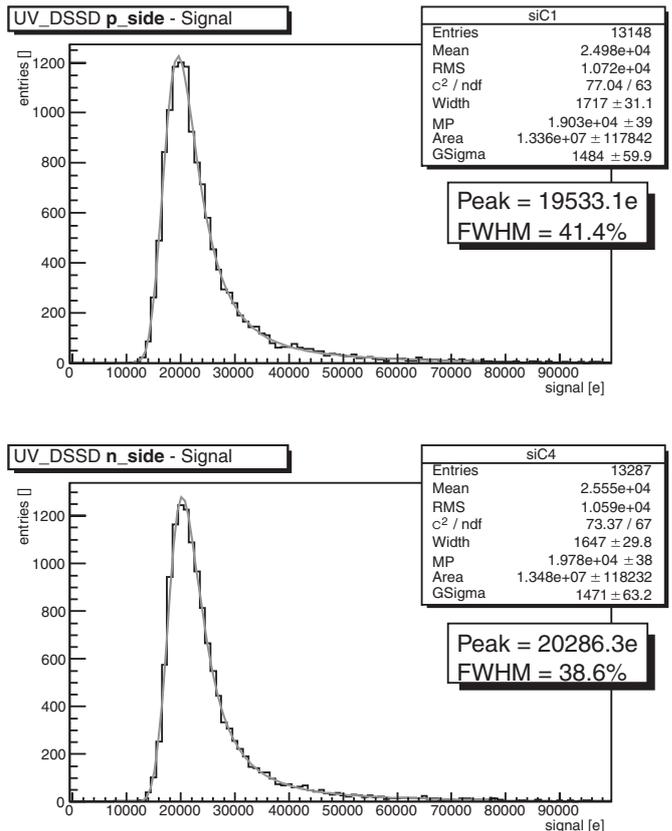


Figure 5: Signal distributions for p- and n- sides of the UV striplet detector at perpendicular incidence, fitted by a convolution of Landau and Gauss. The APV25 internal calibration was used to convert the ADC scale into charge.

Fig. 6 shows the correlations between TDC measurement and fitted peak time as well as the residual distributions (error) for both p- and n-sides of the UV striplet detector. An RMS resolution of 2.2 and 1.6 ns was obtained, including the uncertainty of the scintillator/photomultiplier which is estimated to be about 1 ns.

These measurements were performed at a cluster signal-to-noise of 25. Obviously, the precision of the time finding method strongly depends on that number. A preliminary analysis of the DSSD module, which has longer strips than the UV striplet sensor and thus higher capacitance and noise, returns a cluster signal-to-noise of 14 and 19 for p- and n-sides, respectively. The RMS residuals for the time measurement become 3.9 and 2.3 ns which is consistent with simulation.

Since each particle creates a signal that is read on both p- and n-sides, correlations between those measurements are another indicator of the quality. Fig. 7 shows the relations obtained with the UV striplet module at perpendicular beam incidence, where a linear fit was applied to determine the associated error. For the signal, the offset was fixed at zero, obtaining a slope slightly higher than one, which can be attributed to the different detector layout on p and n sides, regarding floating strips and p-stop, respectively. For the fitted peak time, the slope was held at unity, while the intercept was returned by the linear fit. The offset in the fitted peak time reflects the difference in the clock phase for p- and n-sides, which stems from the clock distribution scheme

used in the KEK beam test and was confirmed by direct measurement at the front-end.

The RMS residual of the signal correlation is in the same

order of magnitude as the Gaussian component in the signal fit, while the fitted peak time error matches with the individual measurements against the TDC. Hence we conclude that the method works fine and yields reasonable results from the statistical point of view.

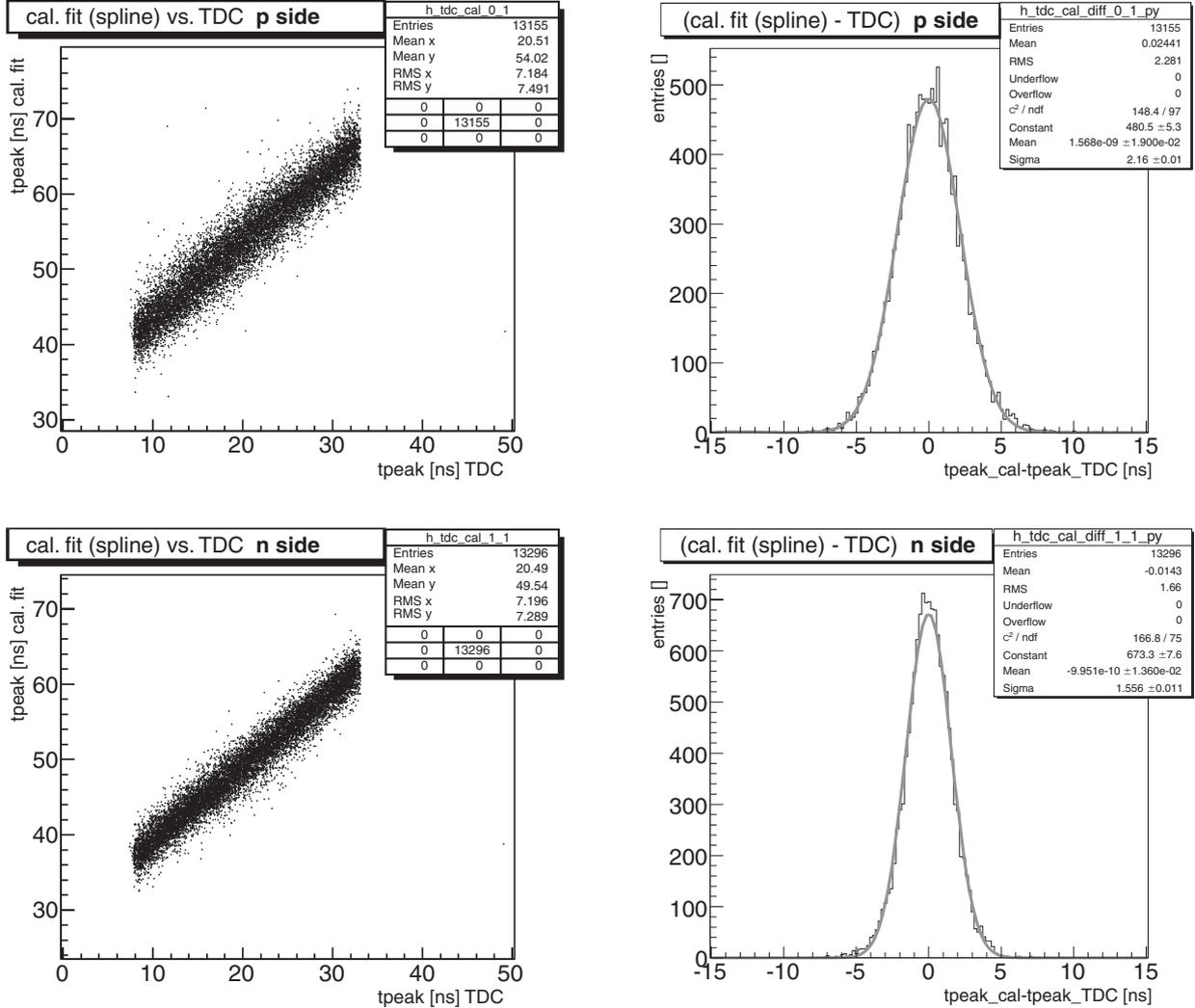


Figure 6: Top row: p-side. Bottom row: n-side. Left column: Correlation between TDC and fitted peak time (offsets are arbitrary). Right column: Residual distribution (error) of the fitted peak time. See text for details.

VI. FUTURE IMPLEMENTATION

Using a numeric fit for each hit is useful for the analysis of a beam test, but not feasible for real-time processing in an experiment with a large number of channels and hits. Hence, we will replace the fitting algorithm by a look-up table which can be implemented in an FPGA. It has been shown that the timing information is essentially contained within three samples around the peak which reduces both readout and processing effort.

The amplitudes of the three samples around the peak will be combined to form the address of the look-up table (RAM array). Each memory cell contains peak time, amplitude and a quality value that specifies their reliability (similar to the χ^2 value of a fit). In parallel, the trigger timing will be measured with a TDC. No matter whether a numeric fit or a look-up table is used, the peak time measurement is not exact due to noise, hence a cer-

tain tolerance has to be allowed depending on the quality value. The internal calibration feature of the APV25 can be used to fill such a look-up table, where timing and amplitude are specified and sample triplets are measured.

The FADC processor module for an upgrade of the BELLE Silicon Vertex Detector is being developed. This board does not only digitize incoming APV data, but also performs pedestal subtraction, a two-pass common mode correction, and zero suppression (sparsification). Finally, the timing of hits will be determined by a look-up table as described above.

Several variants of such a look-up table, all compatible with the FPGAs used for processing, were evaluated by simulation and compared to the fit method. Only minor differences were observed between the implementations, and the deviation from the fit results was negligible compared to the required precision in all cases.

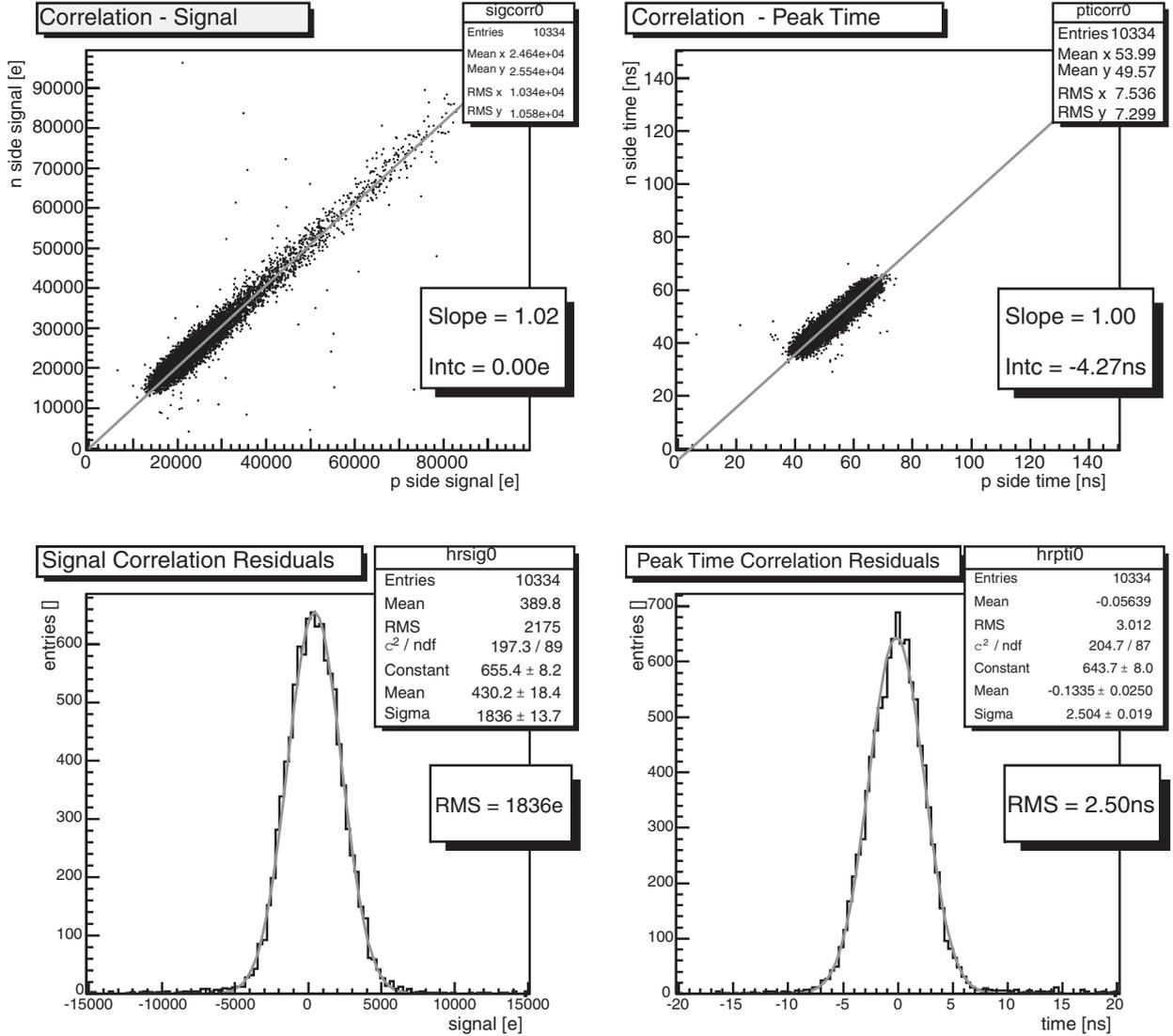


Figure 7: Correlations for signal and fitted peak time obtained at perpendicular incidence. See text for details.

VII. SUMMARY

The APV25 front-end chip can preserve the timing information of silicon detector signals, either by using the built-in “deconvolution” circuit, or by reconstructing the shaping curve from multiple sampled points. Using the latter method, a time resolution of about 2 ns RMS was obtained in a beam test with the UV striplet sensor at a cluster signal-to-noise of 25. Measurements performed on the DSSD sensor with longer strips returned an RMS error of 3.9 ns at a cluster signal-to-noise of 14. Correlations between p and n sides show a spread consistent with that obtained by independent measurements. In the SVD2.5 upgrade of the BELLE Silicon Vertex Detector, this method will be implemented using FPGAs with look-up tables to determine the hit timing on-line. With that information and the trigger time, which will also be measured as a reference, hits can be associated to each other and off-time background can be discarded, allowing a high trigger rate with significant on-line data reduction.

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