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ABSTRACT

The APV25 front-end chip for the CMS Silicon Tracker has a peaking time of 50ns, but confines the signal to a single clock period (=bunch crossing) with its internal deconvolution filter. This method requires a beam-synchronous clock and

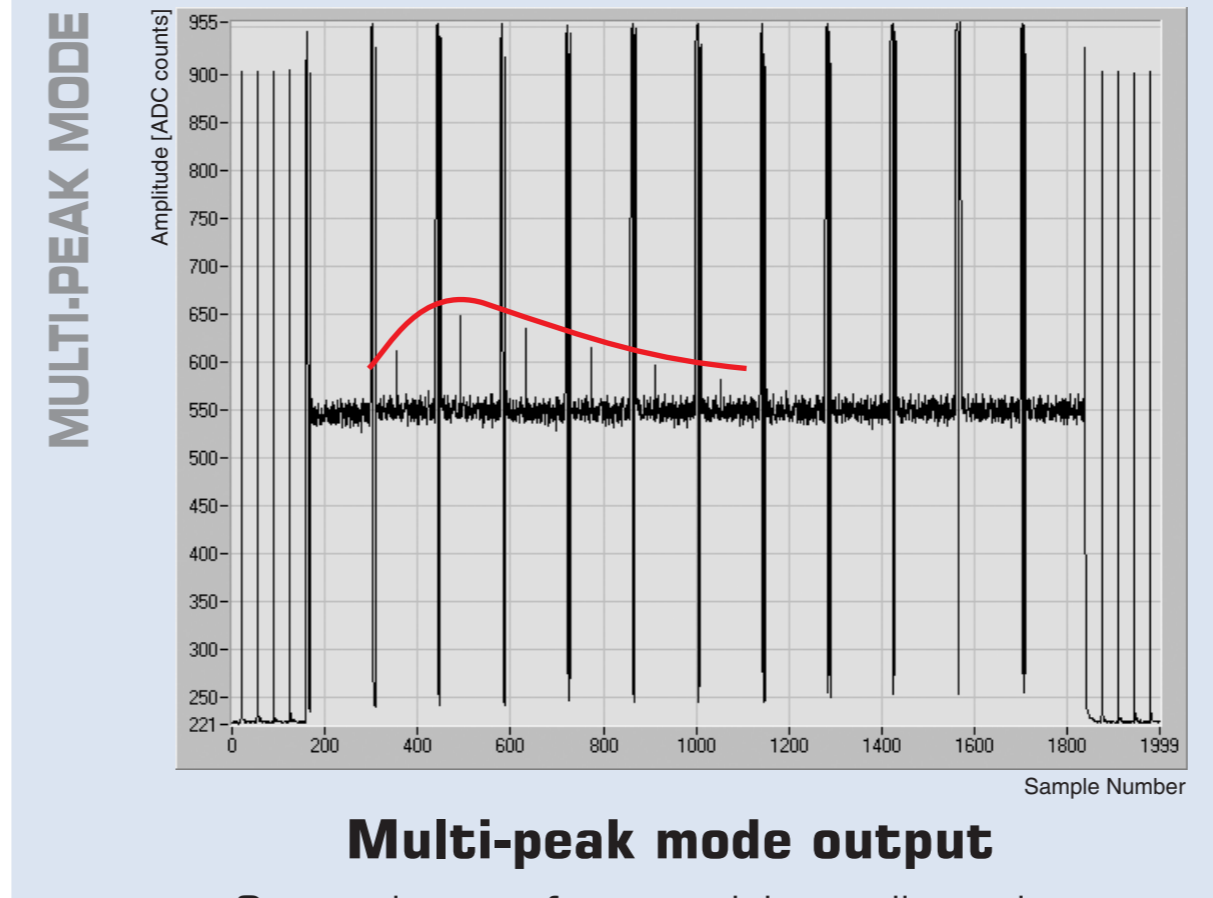
thus cannot be applied to a (quasi-) continuous beam. Nevertheless, using the multi-peak mode of the APV25, where 3 (or 6,9,12,...) consecutive shaper output samples are read out, the peak time can be reconstructed externally with high precision.

Thus, off-time hits can be discarded which results in significant occupancy reduction. We will describe this method, results from beam tests and the intended implementation in an upgrade of the BELLE Silicon Vertex Detector.

APV25

APV25 Front-End Chip Features

- 40MHz operation
- 128 channels
- 192 cell deep analog pipeline
- 50ns shaping time (adjustable between 30 and 400ns)
- Modes: Peak / Deconvolution / Multi-peak
- 0.25µm CMOS process
- Radiation tolerance > 100Mrad
- Low noise: 250e+36e/pF (peak), 400e+60e/pF (deconvolution)



BEAM TEST RESULTS

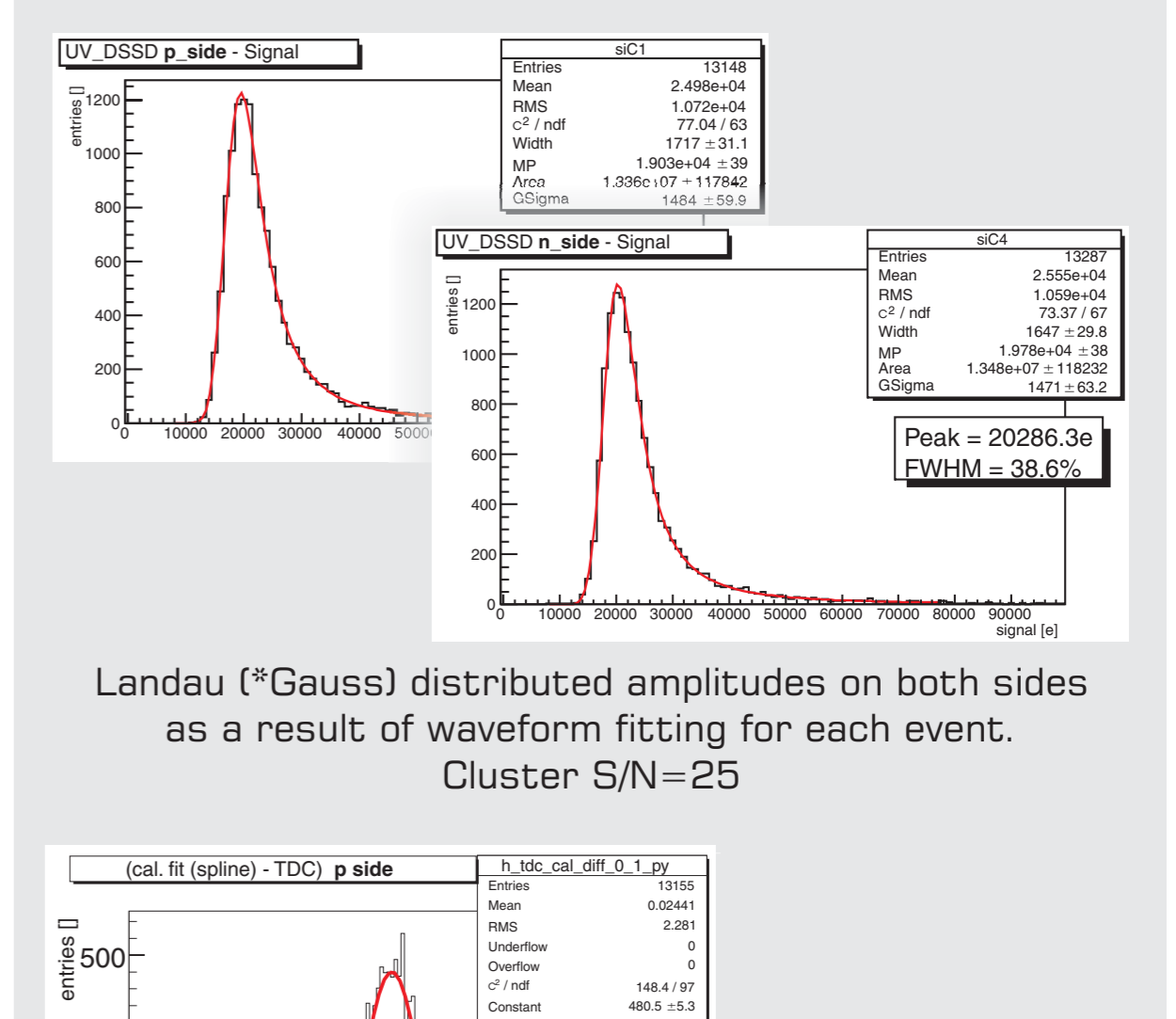
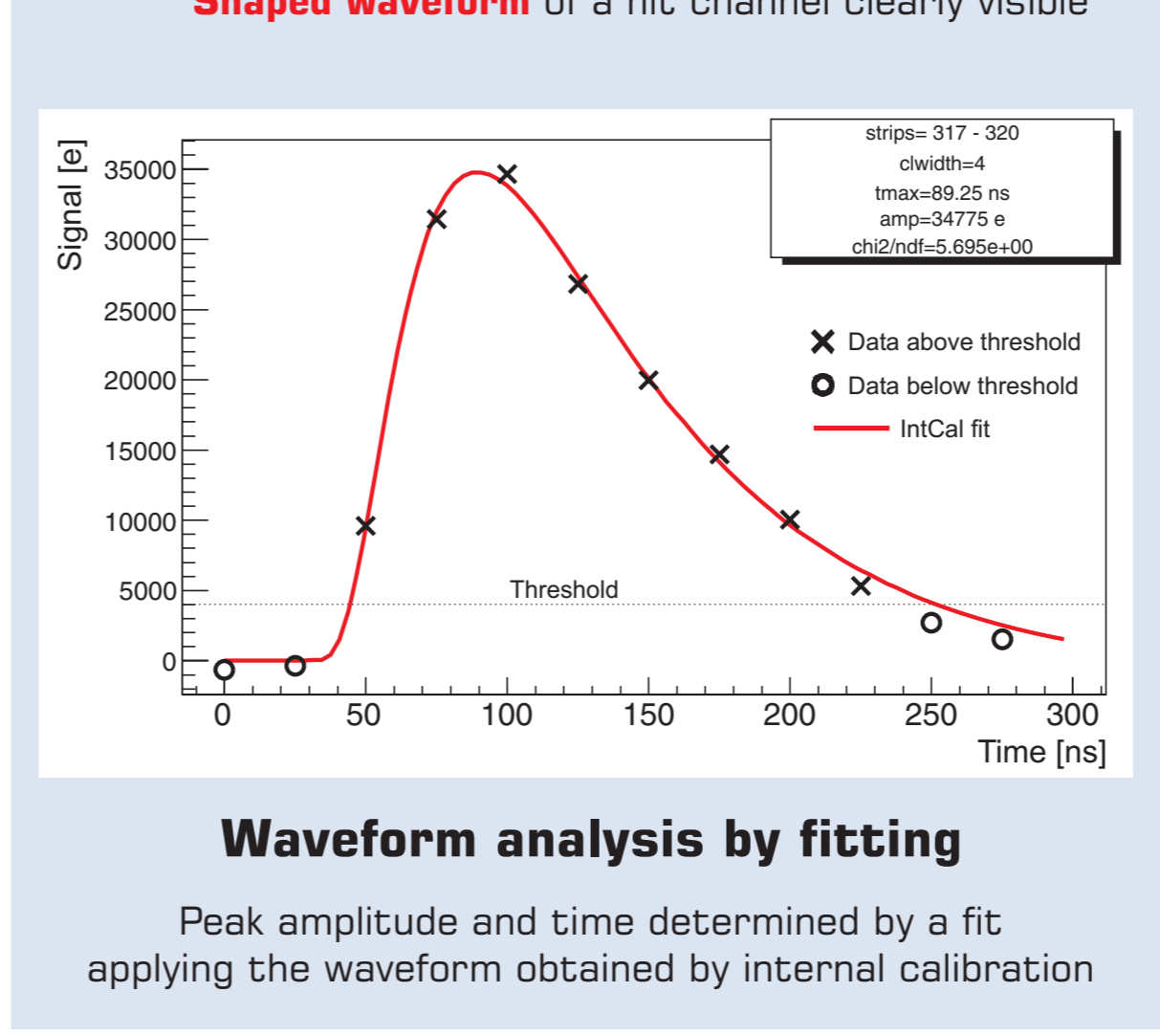
Double-sided sensor with APV25
UV-triplet sensor read out by 4 APV25 chips on each side (only p-side is shown here); used in beam tests

DECONVOLUTION

Weighted sum of 3 consecutive samples
 $d_i = 0.4463 p_{i-2} - 1.4715 p_{i-1} + 1.2131 p_i$

The curve shows the normal shaper output (peak mode) obtained by a progressive scan. The same procedure can be applied in deconvolution mode, resulting in a narrower curve which is virtual because the deconvolution is a time-discrete procedure performed on samples spaced by the clock period (25ns).

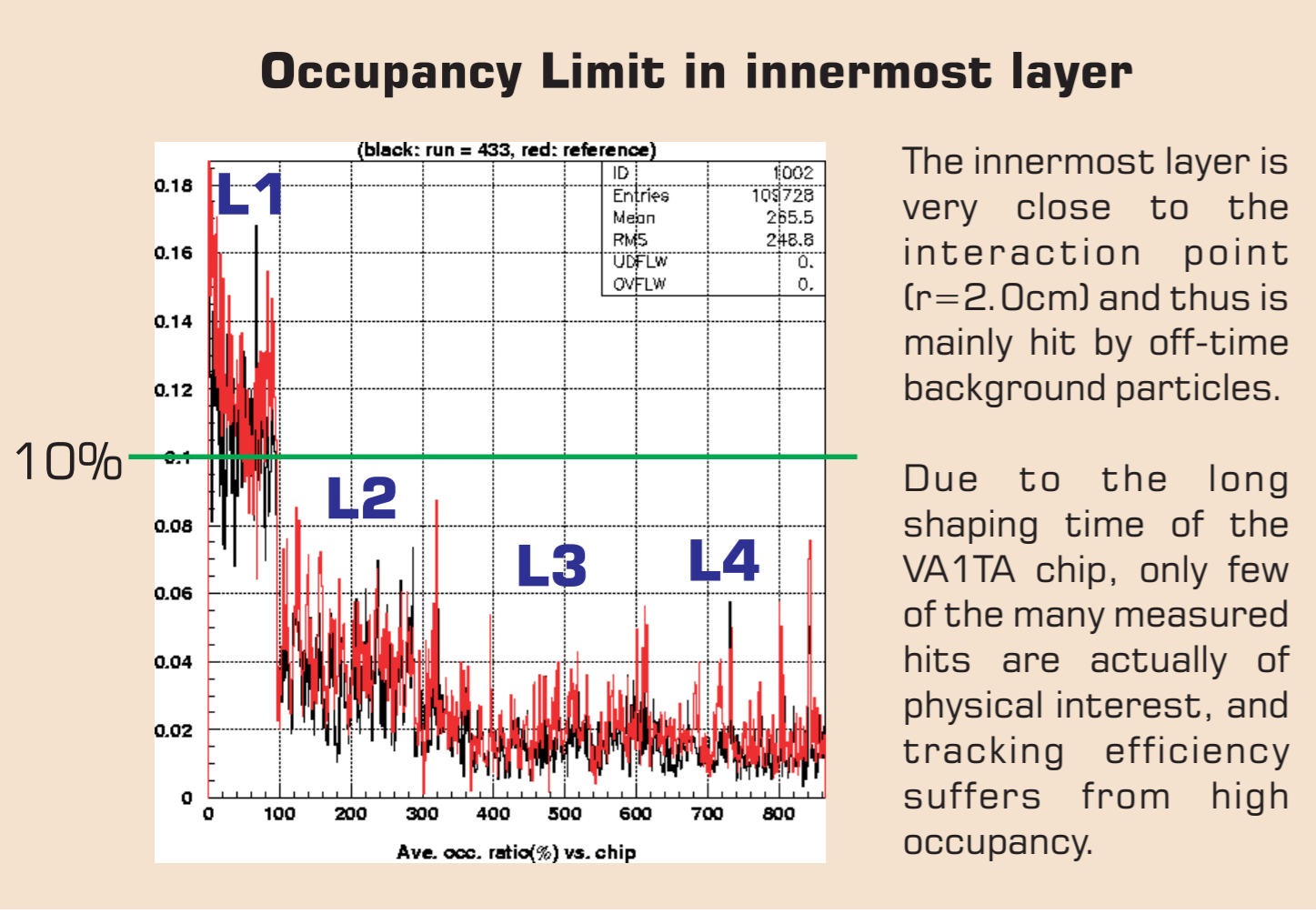
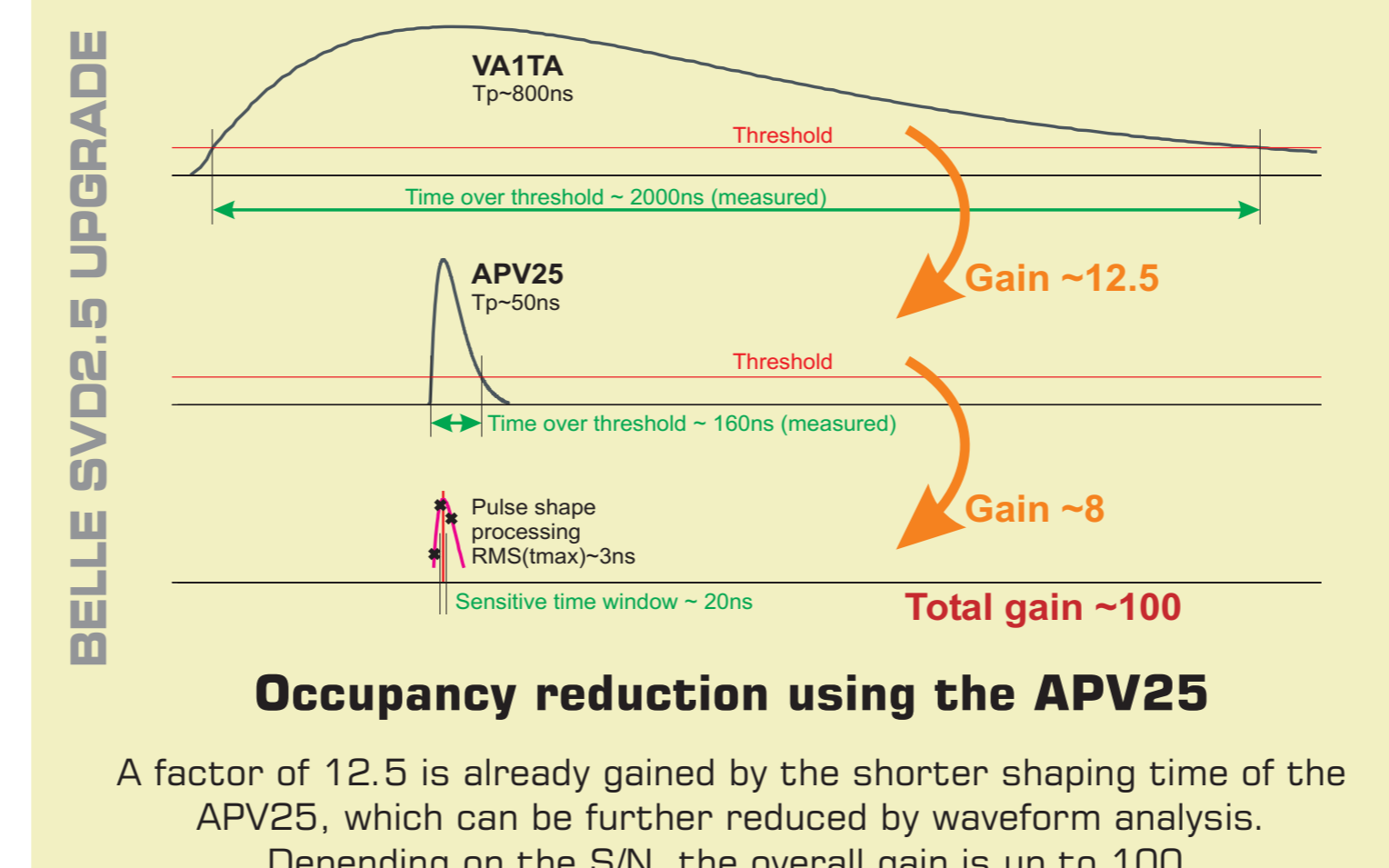
The deconvolution method requires clock synchronous particle signals (i.e. beam)! Thus, it cannot be applied with a quasi-continuous beam such as in BELLE.



BELE SILICON VERTEX DETECTOR

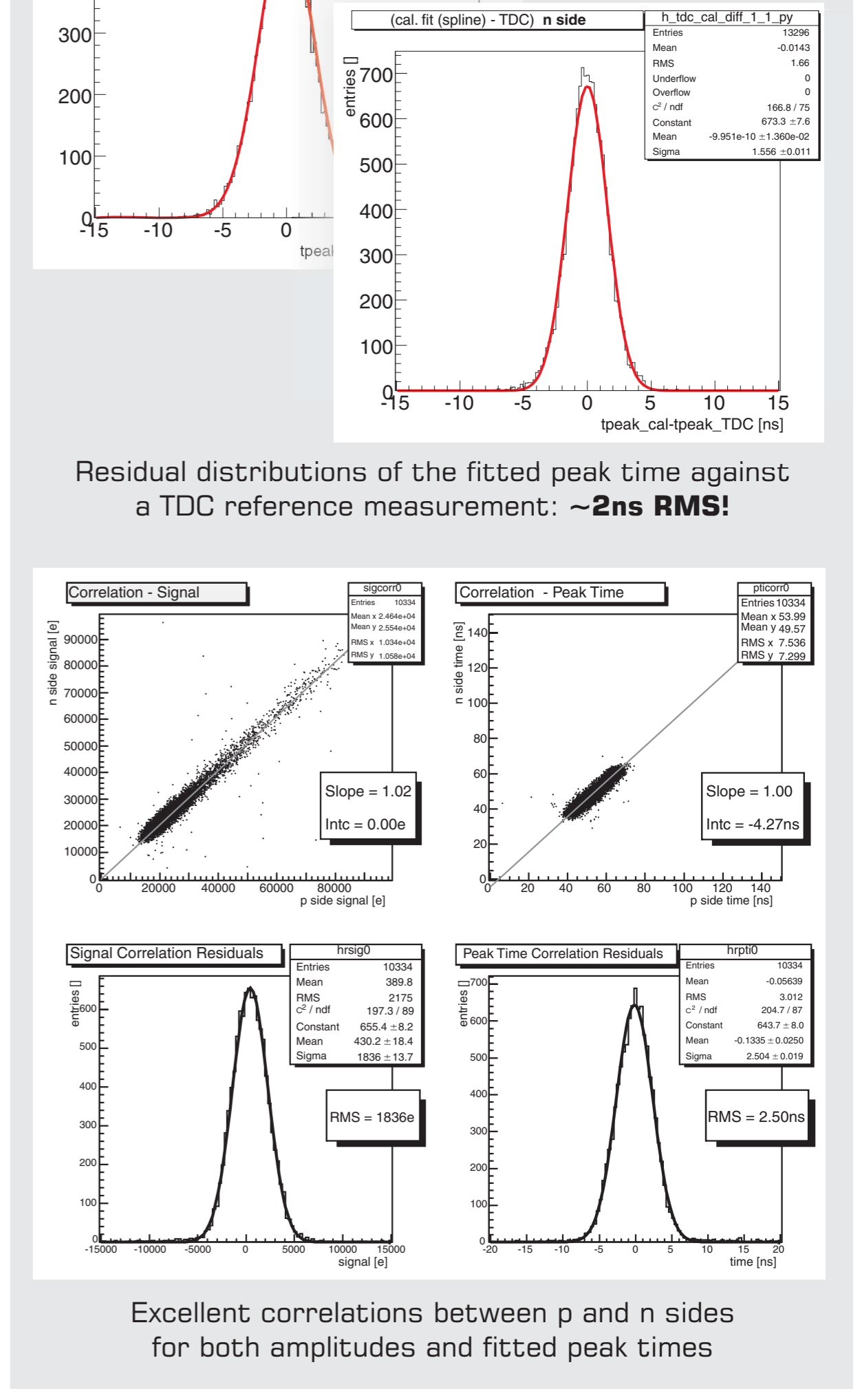
Silicon Vertex Detector SVD2.0

- Double-sided sensors: 246
- Radii: 2.0...8.8cm
- Active area: 0.5m²
- Readout channels: 110592
- Front-end chip: VA1TA (~800ns shaping time)



DAQ for BELLE SVD2.5

The inner layers 1 and 2 will be replaced with APV25 readout, hence two different DAQ paths will coexist. The CMS Pixel FED is modified for use as FADC with pulse shape processing (using Altera FPGAs) in BELLE.



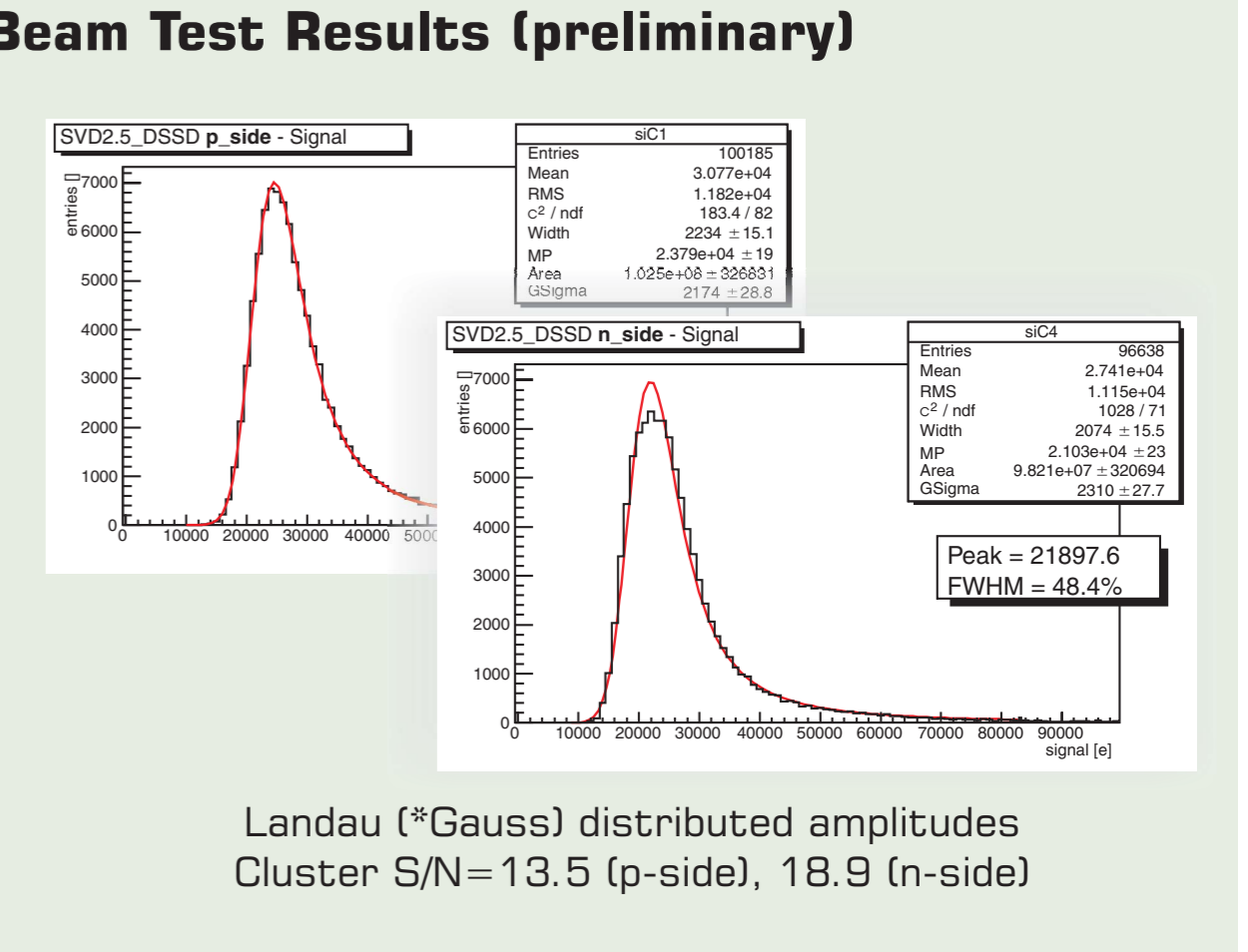
BELE SVD2.5 PROTOTYPE

Thinned APV25s on top of sensor

In order to achieve good S/N (i.e. low capacitance) we mounted APV25 chips directly on the detector using a 2-layer flex "hybrid" circuit and Rohacell for insulation. The APV25 chips are thinned to 100µm to minimize the radiation length budget. Carbon fiber tubes are used for support of hybrid and sensor and cooling of the APV25s.

Beam Test Results (preliminary)

This module was successfully tested in a beam recently; analysis is in progress. Lower S/N was found due to higher capacitance as expected. The preliminary time resolution, measured against a reference TDC, is 3.9 (p-side) and 2.3 (n-side) ns RMS.



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