Contribution ID: **40** Type: **Poster**

Time Resolution of a Few Nanoseconds in Silicon Strip Detectors Using the APV25 Chip

Wednesday 27 September 2006 16:20 (25 minutes)

The APV25 front-end chip for the CMS Silicon Tracker has a peaking time of 50ns, but confines the signal to a single clock period (=bunch crossing) with its internal deconvolution filter.
This method requires a beam-synchronous clock and thus cannot be applied to a (quasi-) continuous beam. Nevertheless, using the multi-peak mode of the APV25, where 3 (or 6,9,12,…) consecutive shaper output samples are read out, the peak time can be reconstructed externally with high precision. Thus, off-time hits can be discarded which results in significant occupancy reduction.
We will describe this method, results from beam tests and the intended implementation in an upgrade of the BELLE Silicon Vertex Detector.

Summary

The APV25 is a low-noise, radiation-hard front-end readout chip made in a 0.25um CMOS process, designed for beam-synchronous operation at 40MHz in the CMS Experiment at LHC. Each of its 128 input channels features a 192-cell analog pipeline as well as a switched capacitor filter where the weighted sum of three consecutive samples is calculated.
Using this deconvolution circuit, the preamp/shaper transfer function is essentially undone in a numeric way, which leads to just a single non-zero output value (25ns wide) compared to the shaper output which is approximately 160ns wide. Hence, it is possible to unambiguously identify the bunch crossing from which a particle originated.

If the APV25 clock and the bunch crossings are not synchronous, e.g. in case of a quasi-continuous beam, this method fails.
However, the APV25 can also be operated in a multi-peak mode where still three consecutive samples are stored in the pipeline with each trigger, but the deconvolution filter is turned off and all three samples are read out. By applying several triggers spaced by 75ns (minimum trigger distance), up to ten triplets (=30 consecutive samples) can be read out, which represent the shaper output waveform.

In order to reconstruct peak time and amplitude, a fit can be applied to each event. This method was successfully demonstrated with APV25 data obtained in beam tests and resulted in an RMS time resolution of approximately 2ns at a cluster signal-to-noise ratio of 25.

The innermost layer of the BELLE Silicon Vertex Detector at KEK (Tsukuba, JP) currently suffers from high occupancy in the order of 10%, which stems from the fact that its VA1TA readout chip has a shaping time of about 800ns. In summer 2007, an upgrade is planned for the two inner layers where the silicon sensors essentially remain the same, but the readout will be done by APV25 chips.
Its faster shaper already reduces the occupancy by a factor of 12.5 (not exactly the ratio of shaping times due to deviations from the ideal CR-RC shape). By using the proposed peak time finding method, comparing the hit timing to the trigger time and discarding off-time hits, another factor of up to 8 (depending on the S/N ratio) can be gained. Hence, the projected occupancy will be well below 1% in the current environment, allowing headroom for future luminosity increase.

Obviously, a fit applied to each hit is not suitable in an experiment. Hence, we developed lookup tables which fulfill the same purpose, perform almost equal to the fit function, but much faster, and are very easy to implement in FPGAs.

Finally, we will also present the VME-based data processing boards which are called “FADCs” but actually do much more than just digitization. Several Altera FPGAs perform channel re-ordering, pedestal subtraction, a 2-pass common mode correction, hit finding (zero suppression) and time finding on the APV25 data. All functions are pipelined, such that the modules are dead-time free. Since the signals are sparsified on the module, the output data rate is considerably reduced compared to transparent readout.

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Session Classification: Poster sessions