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FEC-CCS:

A common Front-End Controller card  
for the CMS detector electronics.

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12<sup>th</sup> Workshop on Electronics  
for LHC and Future Experiments

*Valencia, September 25-29, 2006*

Kostas Kloukinas  
CERN PH/MIC-DG



# Outline



- FEC-CCS Design Architecture
- Sub-system integration phase
- Production Testing
- Summary



# Front-End Control System Overview

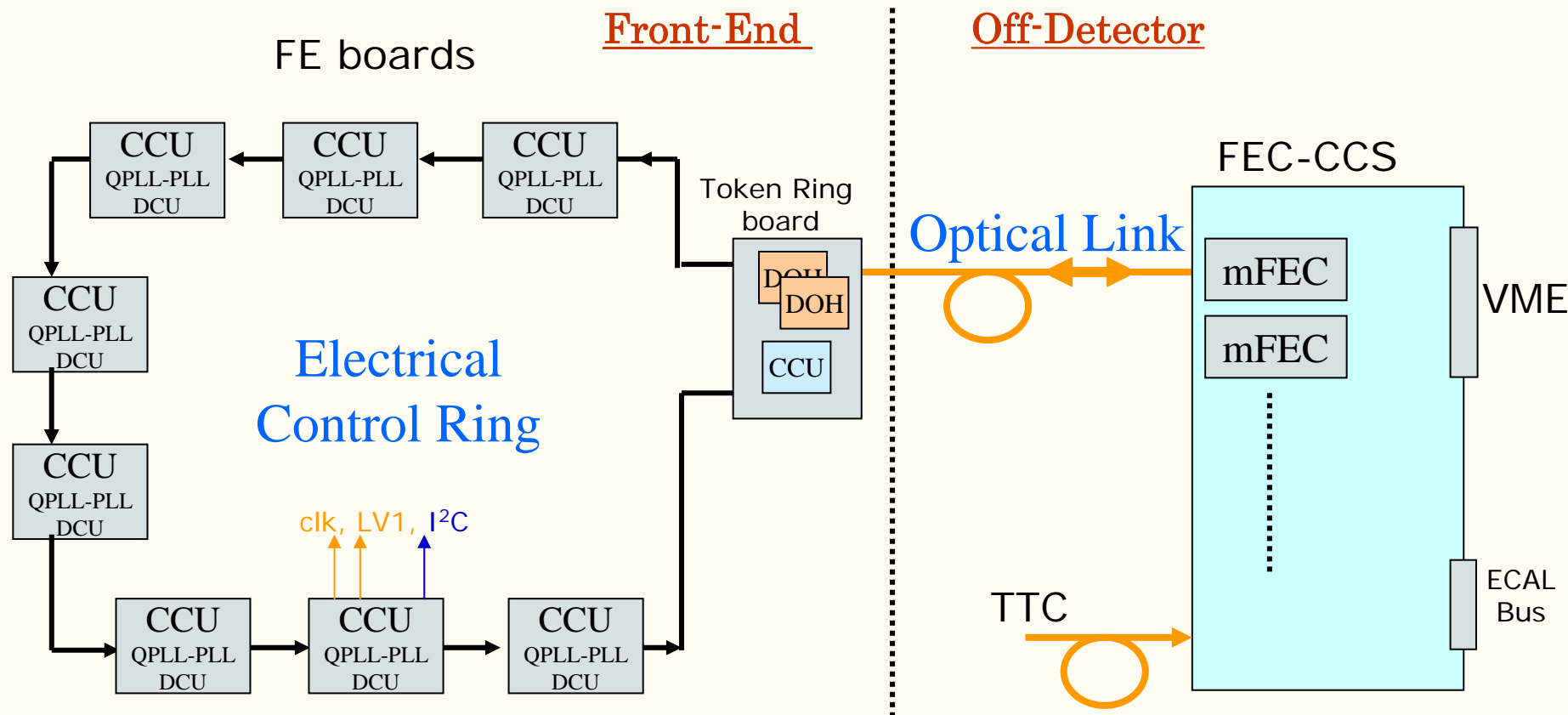


## ■ Main Functionalities:

- Establish control bi-directional links with the Front-End chips.
  - Setup/configure FE chips.
  - Read back status information from FE chips and monitor detector environmental parameters.
  
- Distribute Fast Timing signals to the Front-End chips
  - 40MHz LHC clock
  - Trigger commands



# Front-End Control System Overview



## A common CMS Front-End Control System

- TRACKER
- ECAL
- Preshower
- PIXELS
- RPCs
- TOTEM



# CMS FEC-CCS System



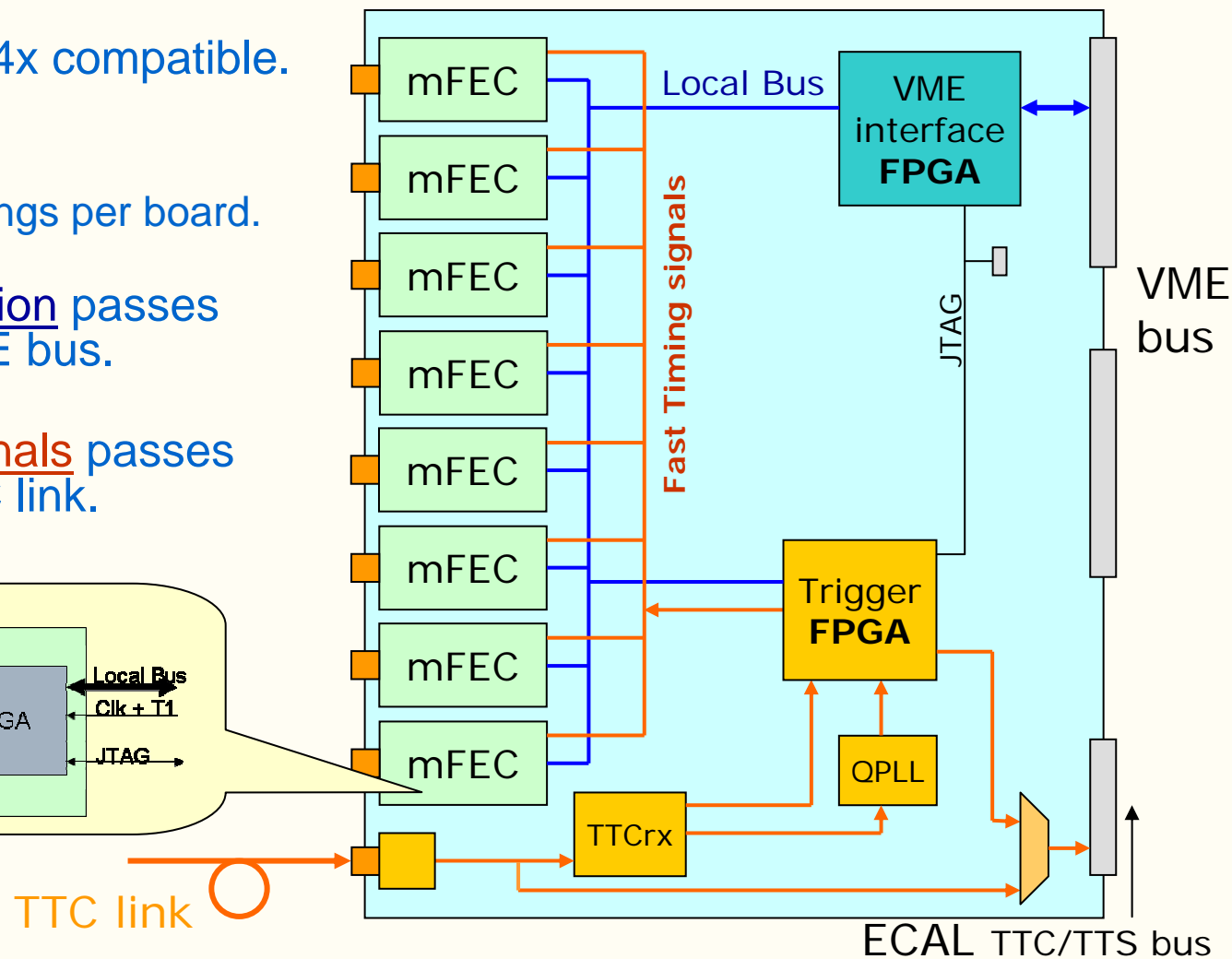
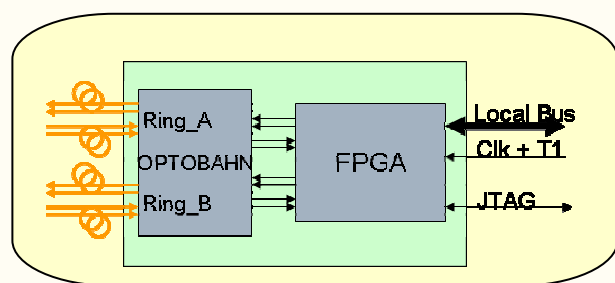
- A common Front-End controller card for the CMS sub-systems.
  - Advantages:
    - Minimize design effort and production cost.
    - Maximize system maintenance and support services.
  - Requirements:
    - Accommodate the differences of the CMS sub-systems architectures.
    - Modular design.
    - Flexibility.
    - Conform to the CMS VME electronics specifications.
  - The VME FEC-CCS card primary users
    - TRACKER : FEC (Front End Controller)
    - ECAL : CCS (Clock & Control System)



# FEC-CCS Block Diagram

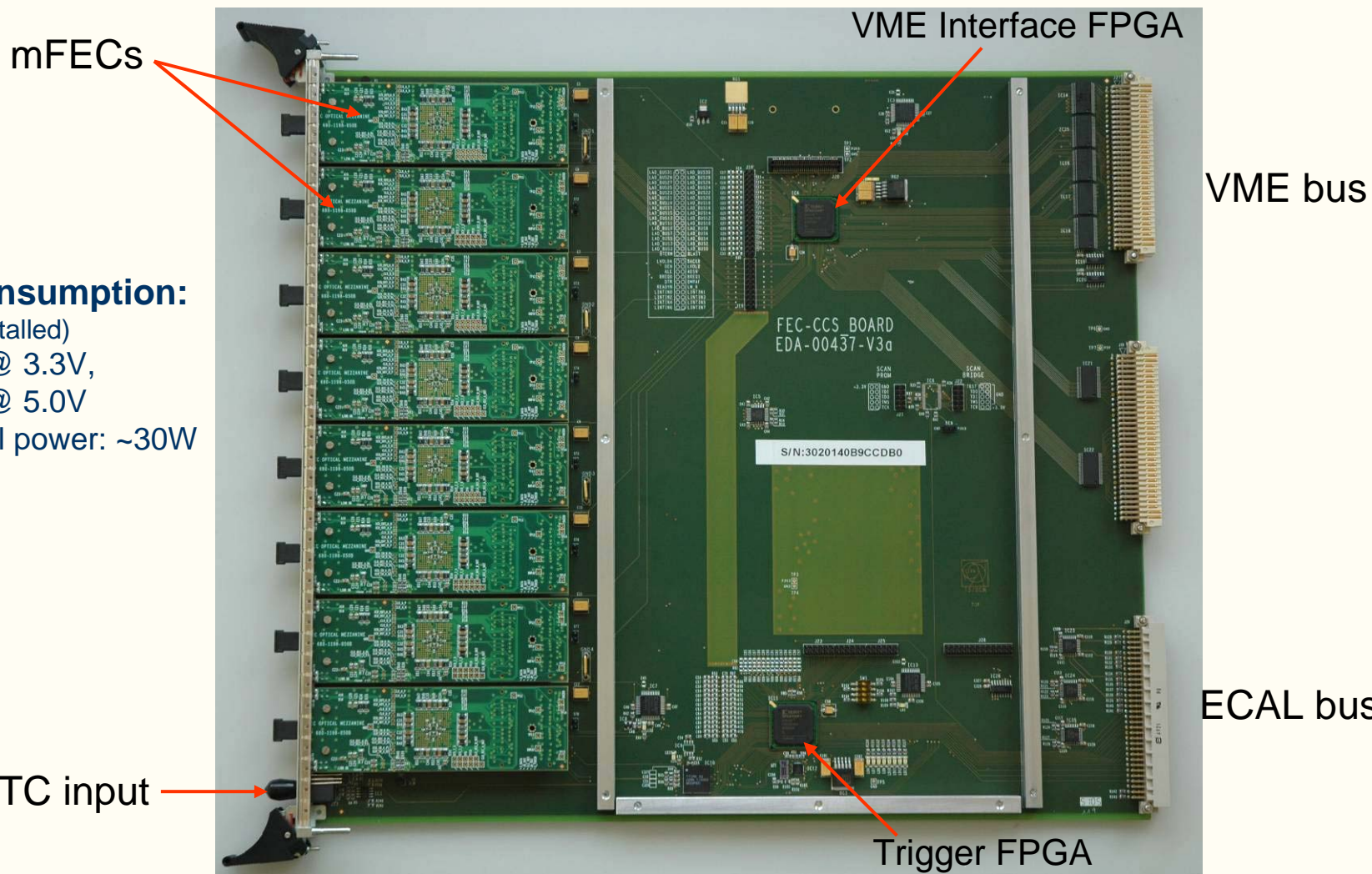


- VME 9U, VME64x compatible.
- Modular design:
  - 1 ~ 8 control rings per board.
- Control information passes through the VME bus.
- Fast Timing Signals passes through the TTC link.





# The FEC-CCS Card



## Power consumption:

(8 mFECs installed)

- 7A @ 3.3V,
- 1A @ 5.0V
- Total power: ~30W

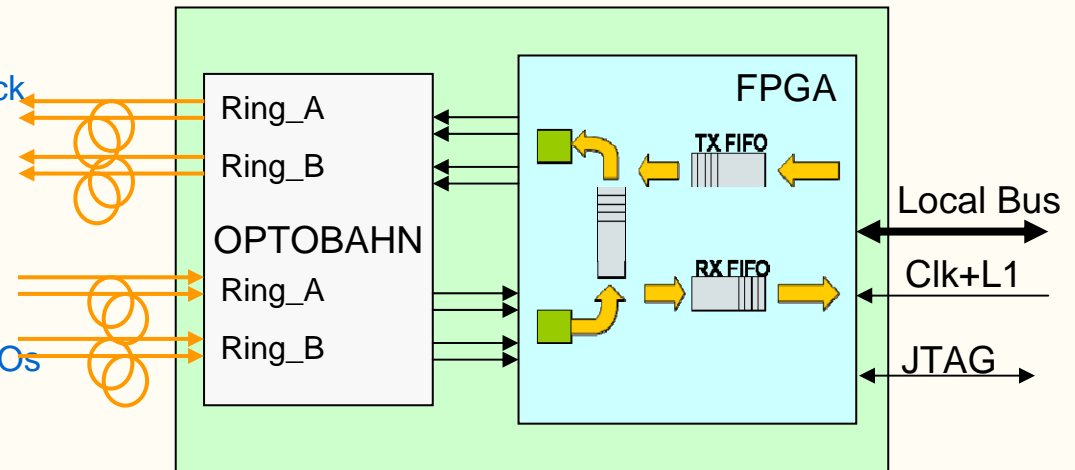


# The mezzanine FEC (mFEC)



## mFEC Functionality

- Token Ring Controller
- Data Link synchronized to the LHC clock
- Data Link raw throughput: 40Mbps.
- Trigger Commands encoded on the clock line.
  - 100 (LV1A)
  - 110, 101, 111
- Dual Rings for redundancy
- Local Bus interface through TX/RX FIFOs



## Local Bus

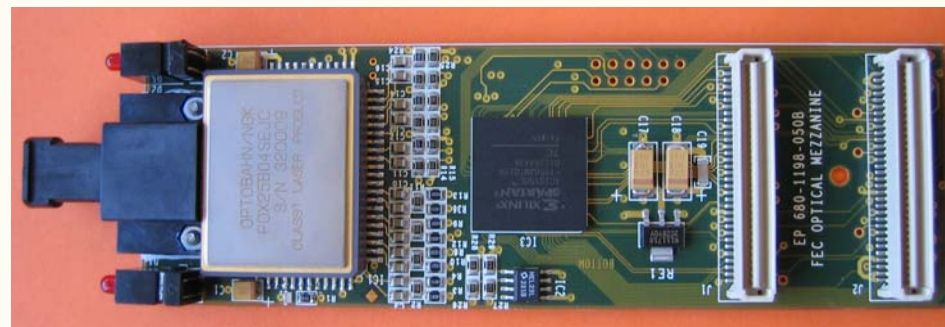
- 40 MHz, 32 bit multiplexed.
- 4 bit geographical address.
- 16 words address space .

## JTAG port for Firmware upload

- Firmware resides on the carrier board.
- No configuration Jumpers.

## Can be plugged onto different types of carrier boards

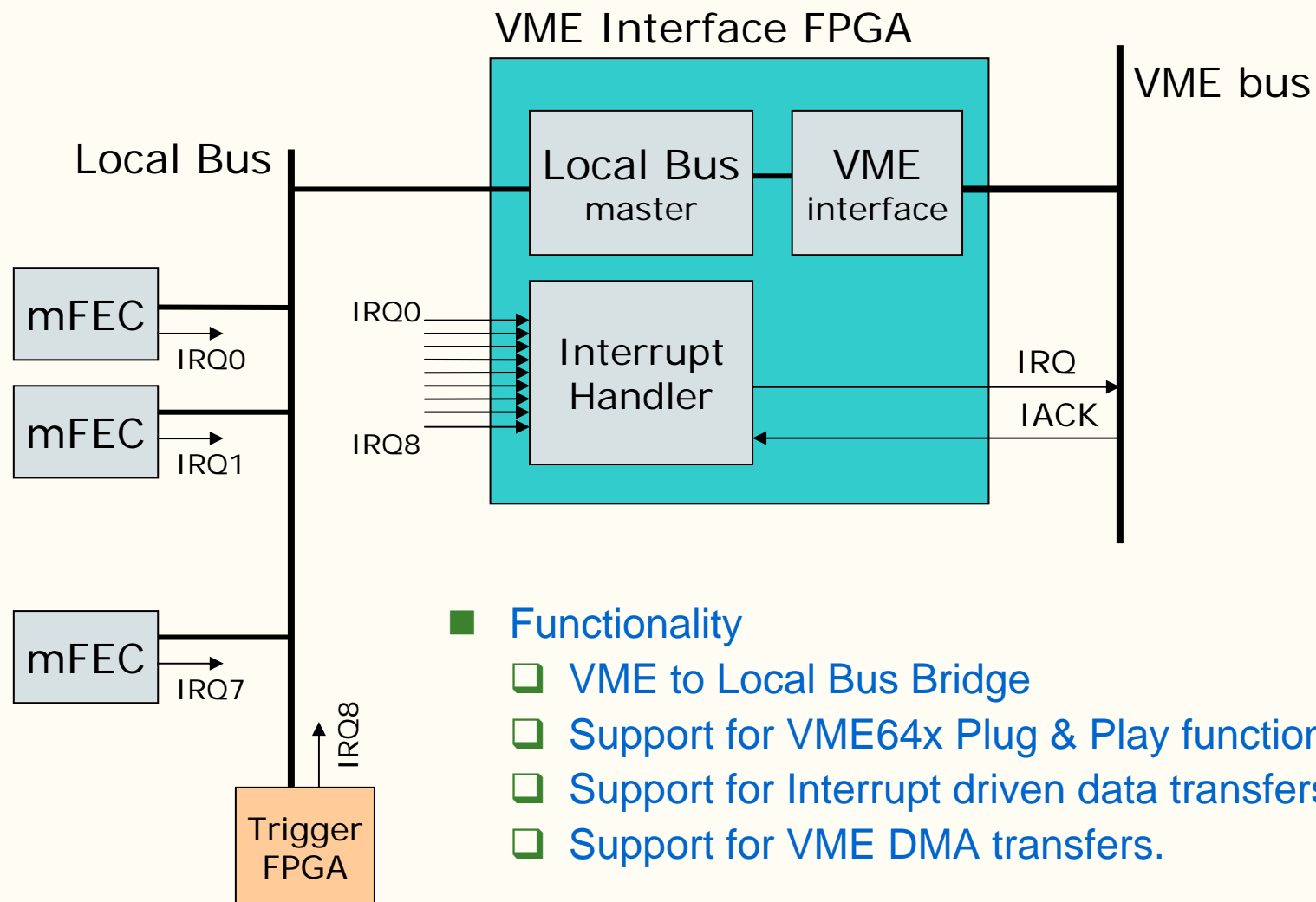
- VME FEC-CCS cards
- PCI carrier cards







# VME Interface FPGA





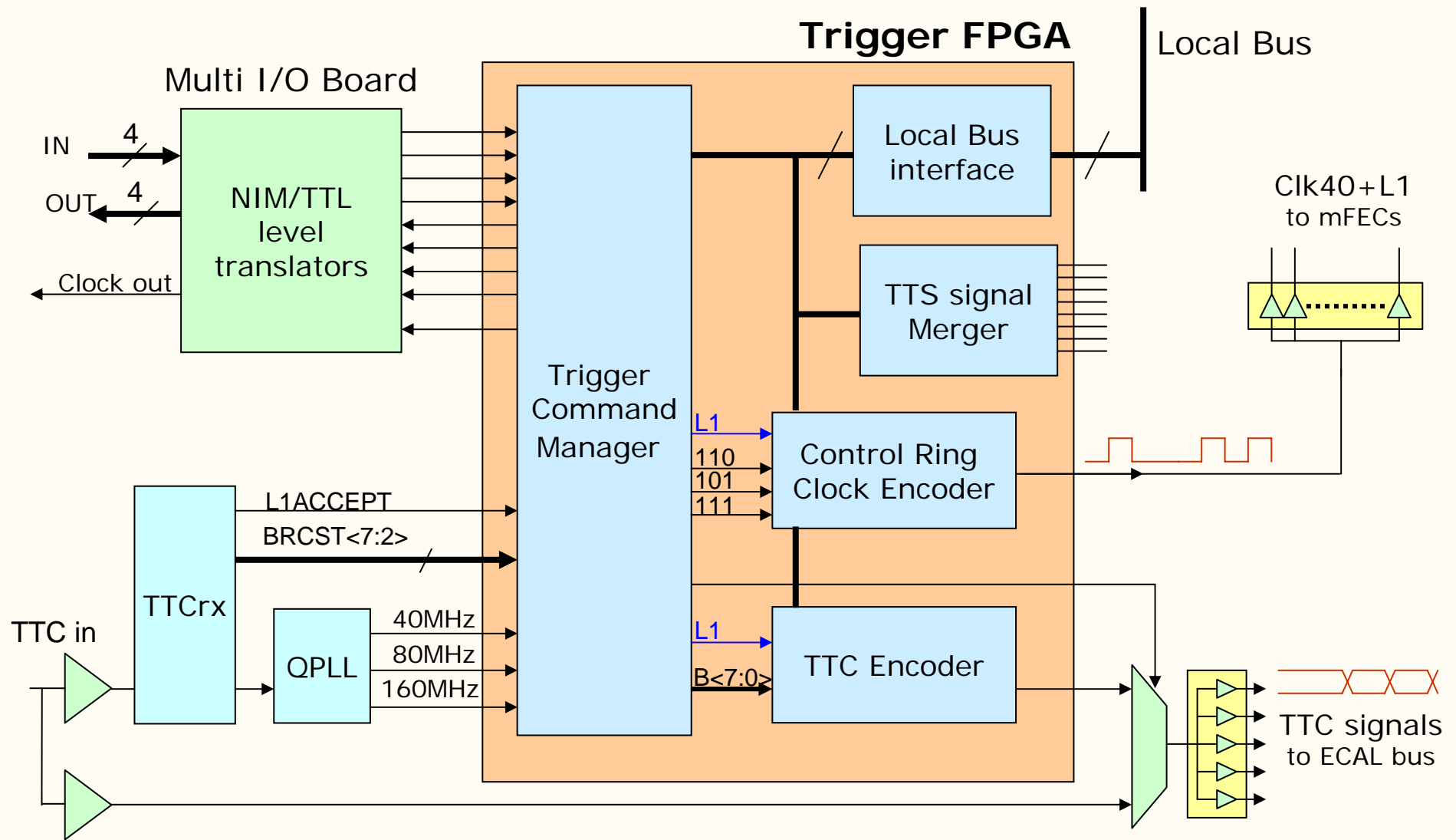
# Fast Timing Functionalities



- **Distribute Clock & Trigger Commands to the FE electronics.**
  - Mapping of TTC B-channel commands to Control Ring Trigger Commands.
  - Monitoring of incoming TTC B-channel commands.
  - Masking of individual TTC B-channel commands.
  
- **Generate a local 40MHz clock in the absence of the TTC signal.**
  - Automatic selection of *Remote/Local Modes*.
  - User programmable *Forced Local Mode*.
  
- **Generate Local Trigger Commands**
  - To support debugging during system integration & commissioning.
  - To support the operation of stand alone setups (without TTC system).
  
- **Provide support for the ECAL special TTC/TTS bus and functionalities**
  - TTC signal fan-out to the DCC & TCC VME modules.
  - TTS signal fan-in from the DCC & TCC VME modules.
  
- **Interface with external equipment via NIM I/O signals.**



# The Trigger FPGA

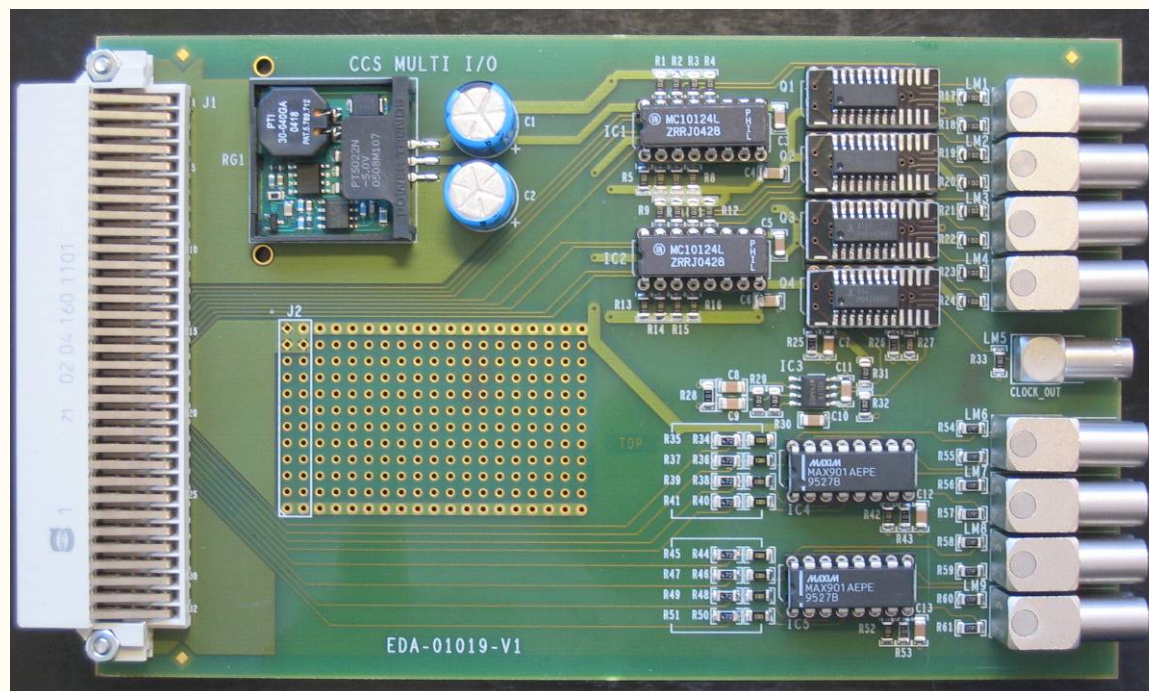




# FEC-CCS Multi I/O board



VME RJ2 connector



NIM I/O

4 Inputs

1 clock out

4 Outputs

- Provides synchronization with external equipment.
- 3U Rear VME Backplane Transition Board
- Connects on VME RJ2 connector.



# Trigger Command Manager



## ■ Mapping of TTC B-channel commands to Control Ring Trigger Commands

TTC B-Go channels for the FEC-CCS VME board

B-Go ch.	TTC Brcst<5:2>	Command	TRACKER		ECAL		Preshower		PIXEL		RPCs	
			T Ring	Function	T Ring	Function	T Ring	Function	T Ring	Function	T Ring	Function
	0000	Not Used										
1	0001	BC0			101	BC0	101	BC0				
2	0010	Test Enable	110	APV_CALIBRATE	111	Monitoring	111	CalPulse				
3	0011	Private Gap										
4	0100	Private Orbit										
5	0101	ReSync	101	RESYNC	110	ReSync	110	ReSync	101	ResetTBM		
6	0110	HardReset	101	APV_RESET								
7	0111	Reset Event Counter							111	ResetROC		
8	1000	Reset Orbit Counter								Send		NOT IN USE
9	1001	Start										
10	1010	Stop										
11	1011	Free1							110	CalSync		
12	1100	Free2										
13	1101	Free3										
14	1110	Free4										
15	1111	Free5										
<b>TTCrx signal</b>												
	L1ACCEPT		100	L1	100	L1	100	L1	100	L1		NOT IN USE

- Control Ring Trigger Command Assignments are not common for all the subsystems.
- The decoding of these commands by the Front-End ASICs is hardwired.

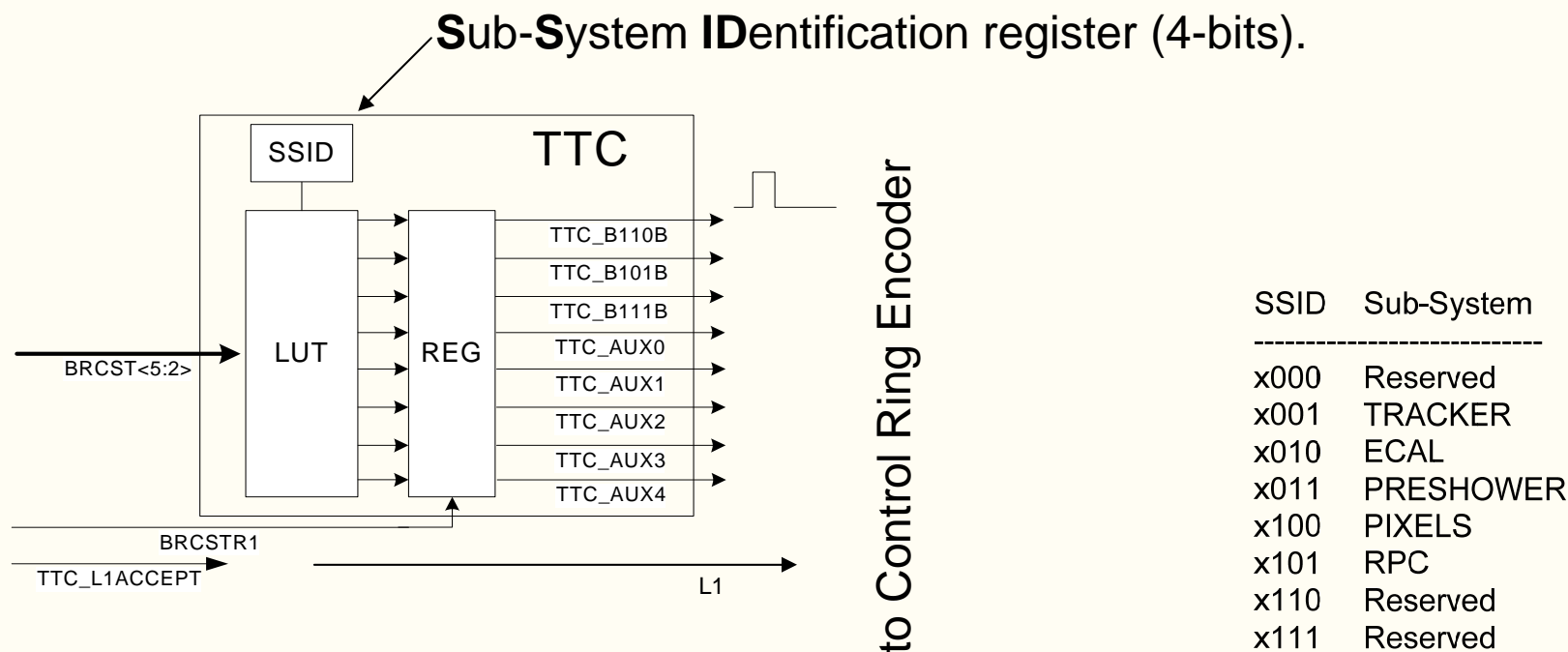


# Trigger Command Manager



## ■ Solution:

- Mapping of TTC B channel commands to Control Ring Trigger Commands can be done using a LUT in the Trigger FPGA.





# FEC-CCS card Trigger Latency

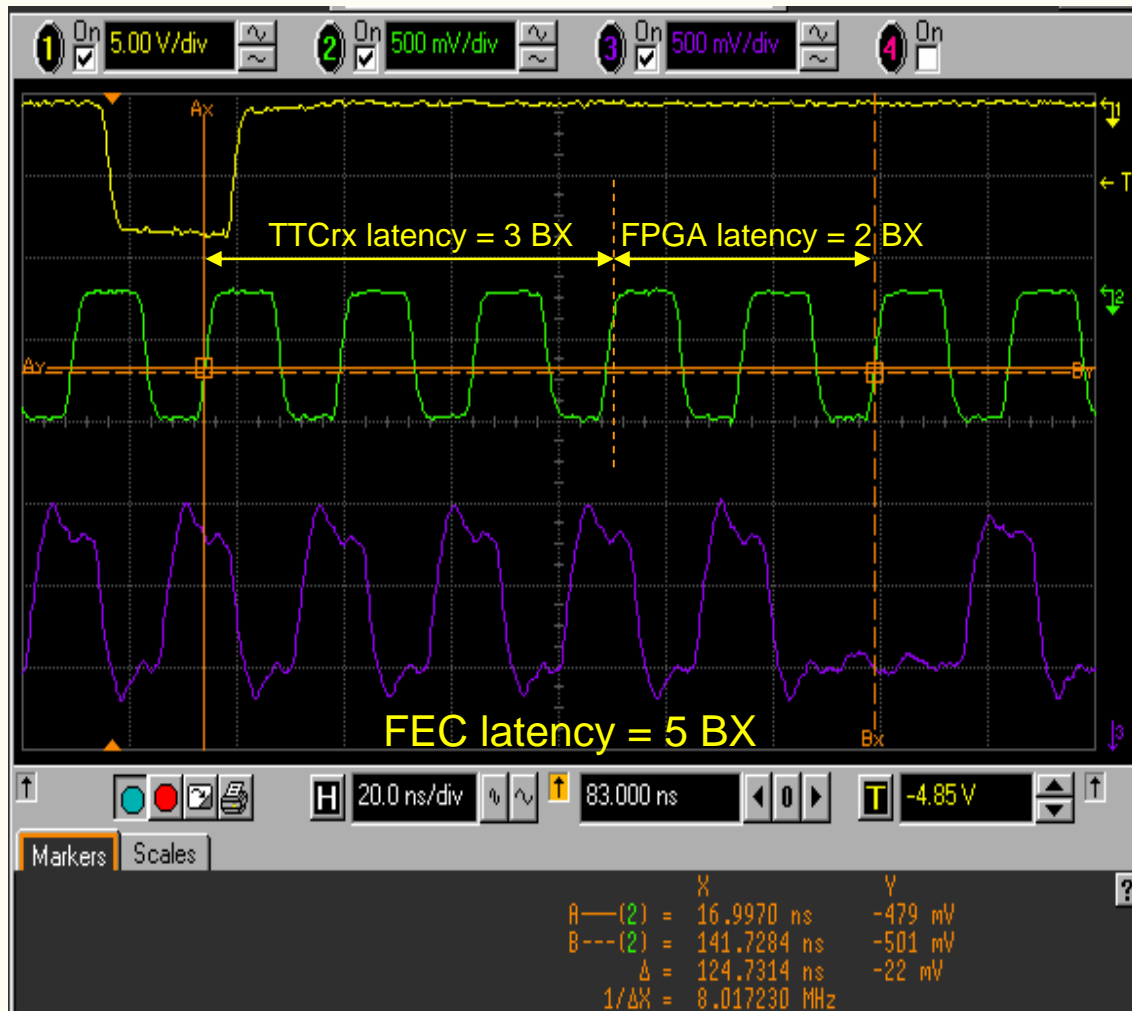


Trigger Latency = 5 BX  
from TTC input to mFEC output

TTCci L1A out

TTCci CLK out

VME FEC  
mFEC CLK\_OUT\_P





# Local Trigger Generation Logic



- Functionality needed in stand alone DAQ system setups, without a TTC system support.
  
- Generic Logic architecture
  - Instead of a hardwired trigger logic customized for a specific test setup, a flexible, user configurable trigger logic, is implemented.
  - The Physicists and Engineers can configure the Trigger Generation logic as required for each test system setup.
  
- Flexible and configurable logic
  - Generation of
    - Single trigger commands.
    - Bursts of trigger commands.
    - Single shot sequences of trigger commands.
    - Periodic sequences of trigger commands.
  - Programmable delays for the timing of the trigger commands.
  - Synchronization with external signals.





# Local Trigger Generator



## ■ Modular design

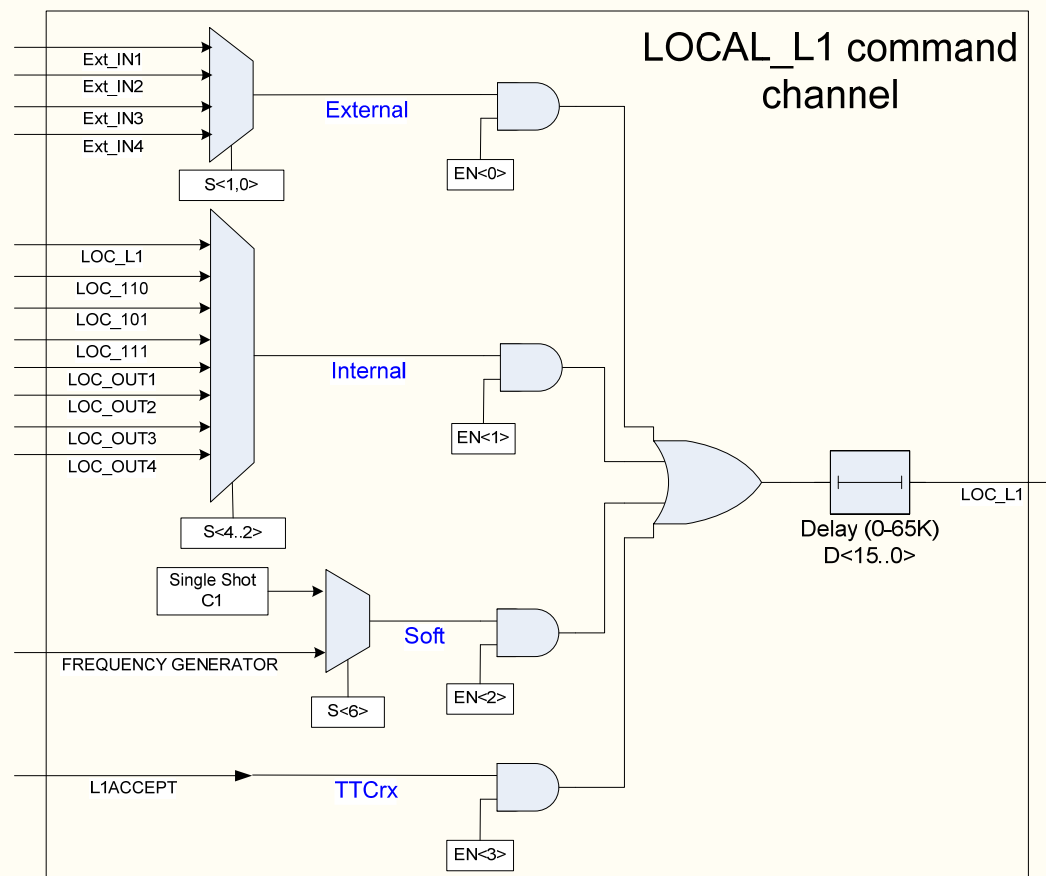
- ❑ 8 identical “command channels”.
  - 4 Control Ring command channels.
  - 4 Auxiliary command channels.

## ■ Trigger Command sources

- ❑ User selectable
  - External signals
  - Internal signals
  - Software (VME)

## ■ Trigger Command outputs

- ❑ Control Rings
- ❑ ECAL bus
- ❑ NIM Outputs

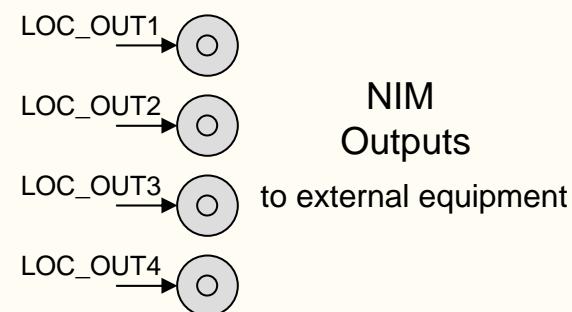
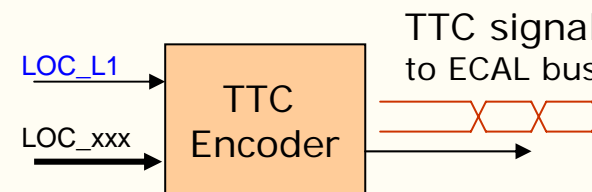
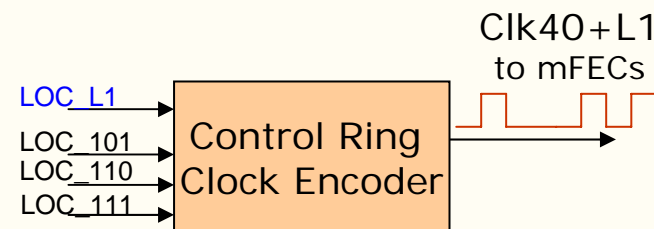
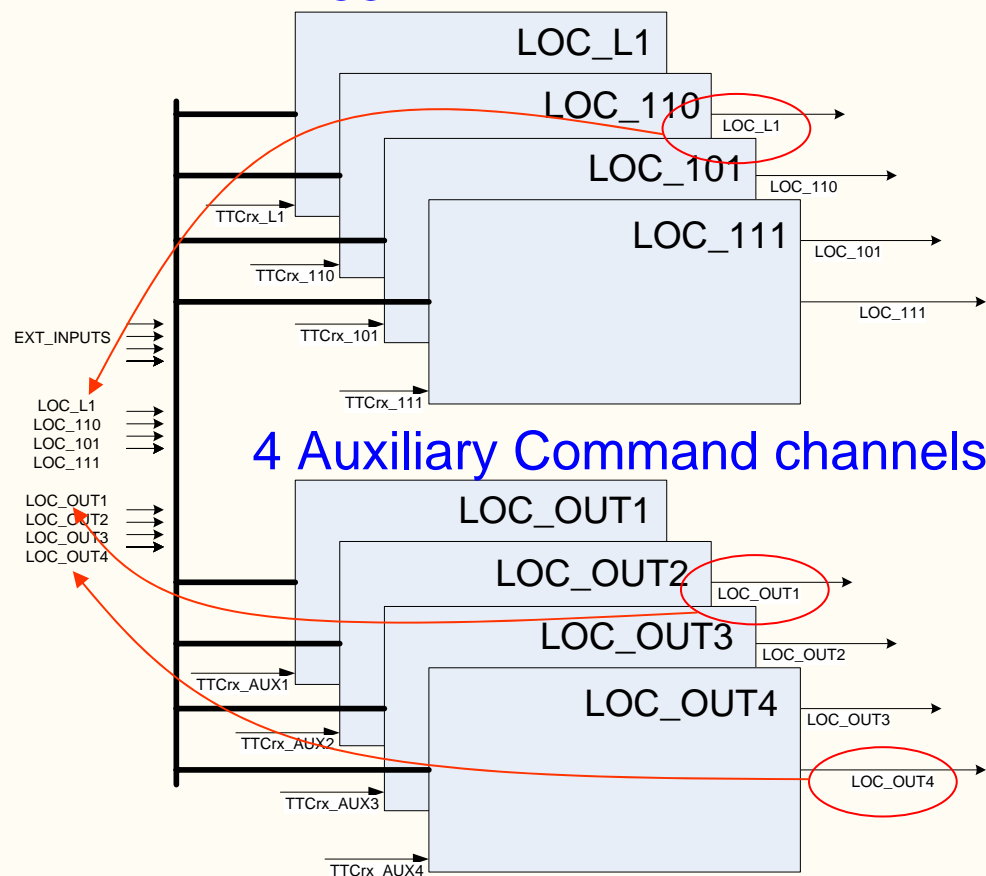




# Local Trigger Generator

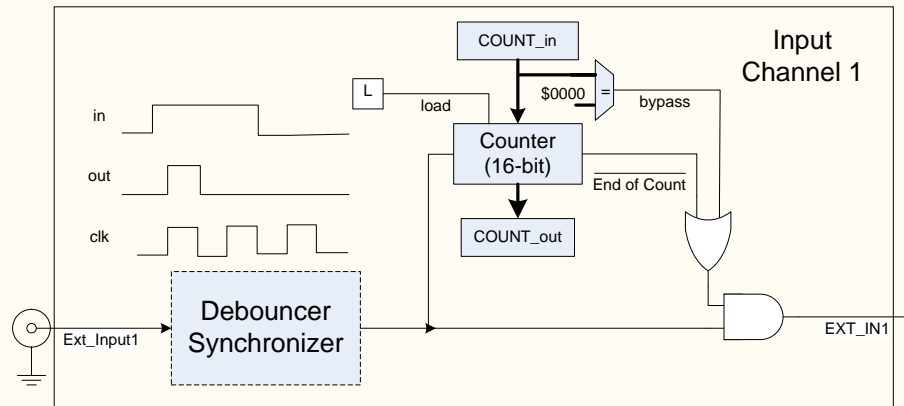


## 4 Trigger Command channels



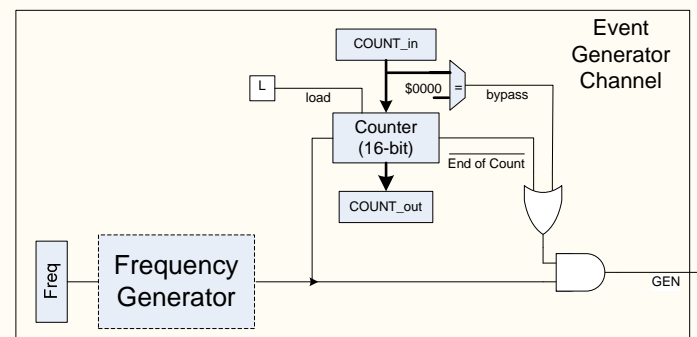
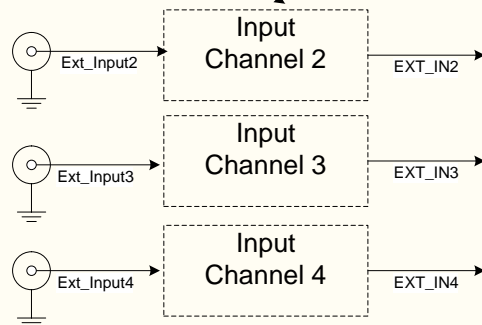


# Local Trigger Generator



- 4 External Input Channels
- Event rate prescaling.
- 1 Generator for Periodic Events
- Emulate LHC Orbit signal.

NIM  
Inputs  
from external  
equipment





# Results from Field operations



- Local Trigger Generation Logic use in ECAL system setups:
  - ECAL Test Beam run 2004.
  - Supermodule Integration Hall (Bldg. 867).
  - H4 Cosmic calibration stand.
  - H4 ECAL Test Beam stand.
  - H2 ECAL+HCAL Test Beam stand.
  - MTCC (Magnet Test Cosmic Challenge) run 2006.
    - Local mode used for debugging. Remote mode used with TTCi.
  
- Typical Operations
  - Pedestal Run
    - Software programmed periodic L1 triggers.
  - Electronics Calibration Run
    - Sequence of FE charge injection commands followed by delayed L1 trigger.
  - Laser Calibration Run
    - Command the firing of Laser pulser. Receive trigger from Laser apparatus.
  - Test Beam Run
    - Receive external trigger from counters and NIM logic.

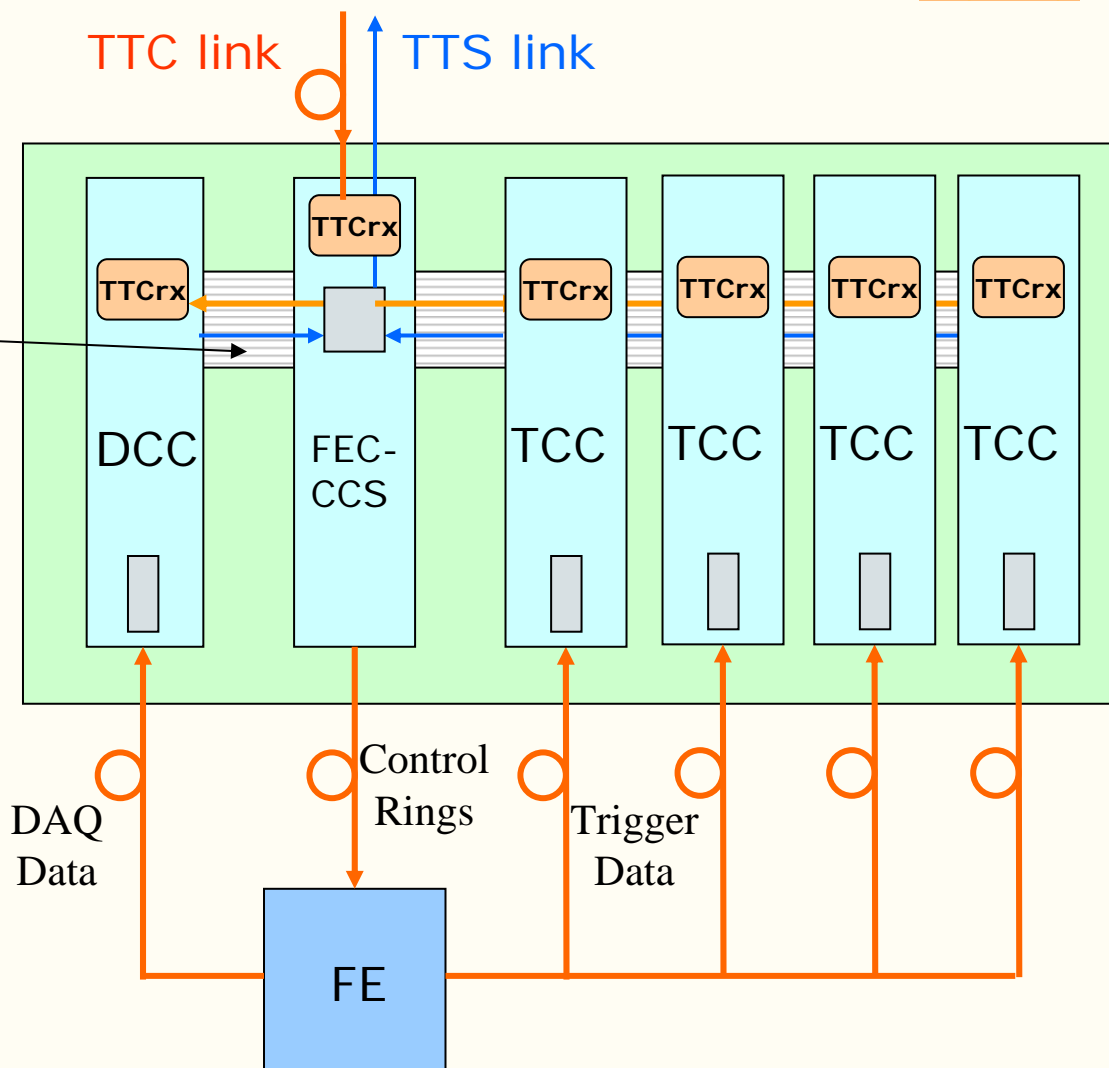


# The CMS ECAL case



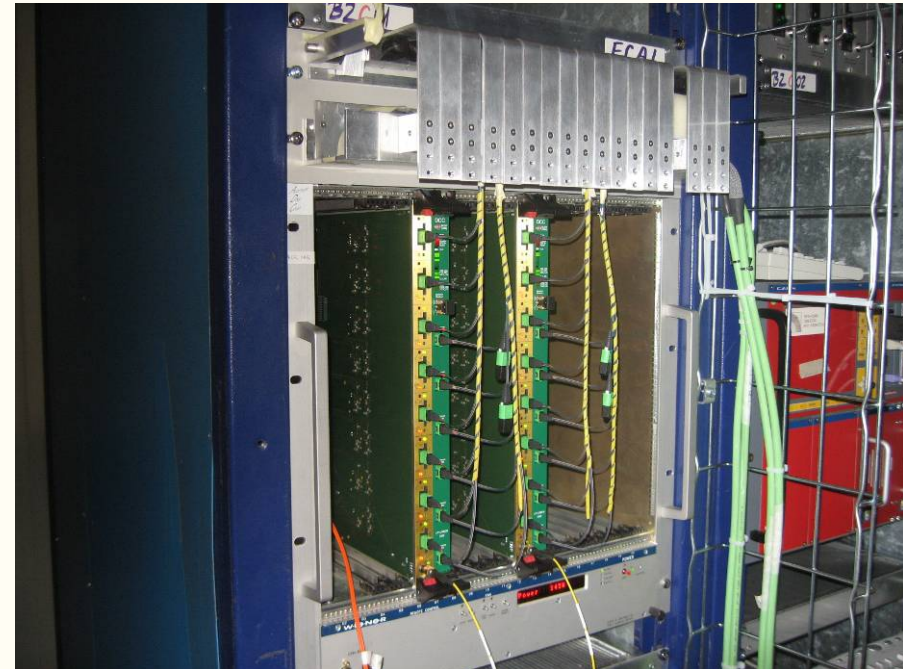
DAQ and Control cards coexist in the same crate.

- ECAL TTC/TTS bus:
  - Distribute TTC signal
    - PECL
  - Merge TTS signals
    - LVDS
  - Bus Length:
    - Endcap: 3 VME slots
    - Barrel: 6 VME slots
- ECAL system
  - EB (Barrel) 36 FEC-CCS cards
  - EE (Endcap) 18 FEC-CCS cards





# The CMS ECAL case



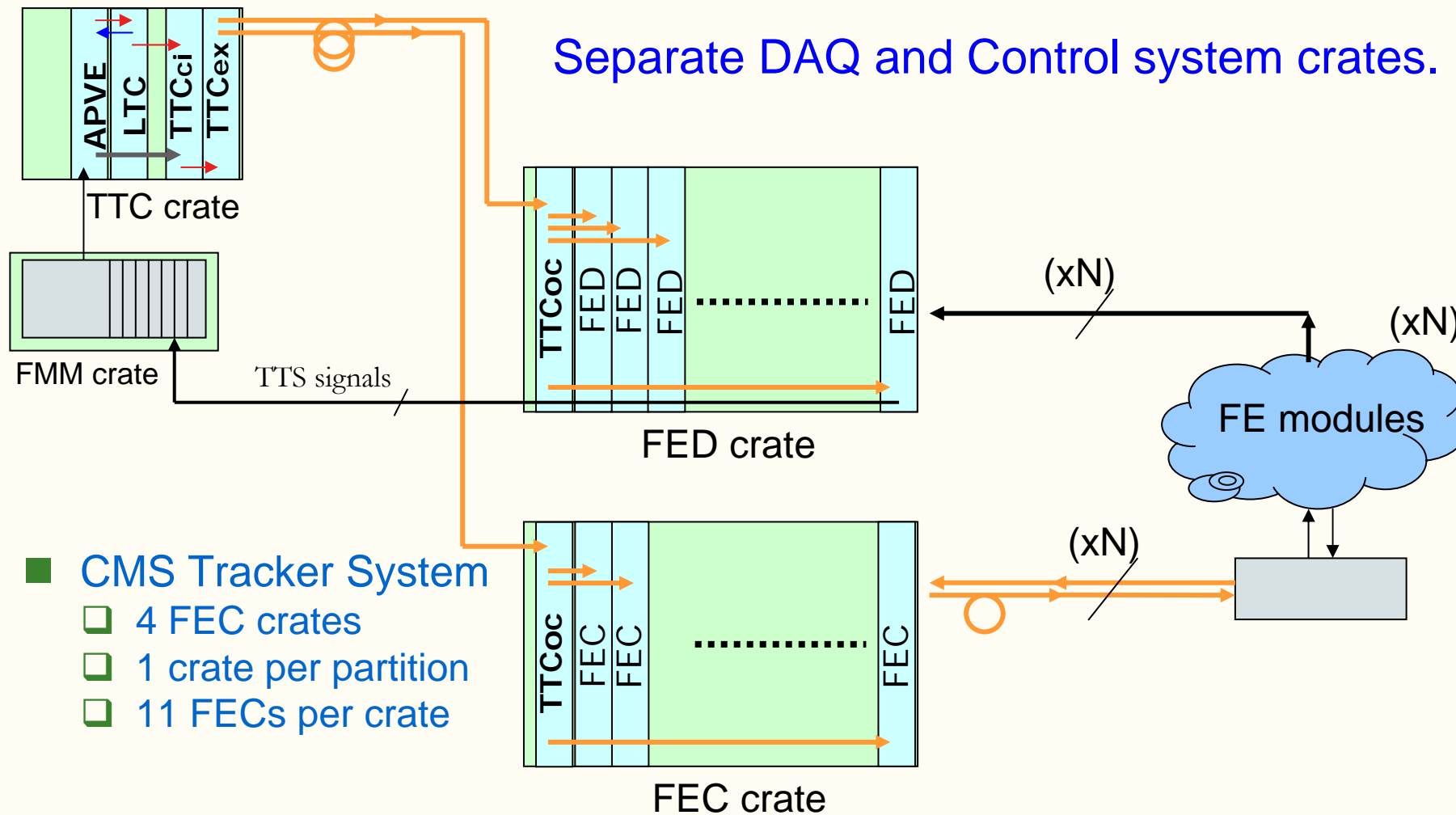
- 5 different setups in operation:
  - ❑ Supermodule Integration Hall (Bldg 867)
  - ❑ H4 Cosmic calibration stand
  - ❑ H4 ECAL Test Beam stand
  - ❑ H2 ECAL+HCAL Test Beam stand
  - ❑ MTCC (Magnet Test Cosmic Challenge)



# The CMS Tracker case



Separate DAQ and Control system crates.



## ■ CMS Tracker System

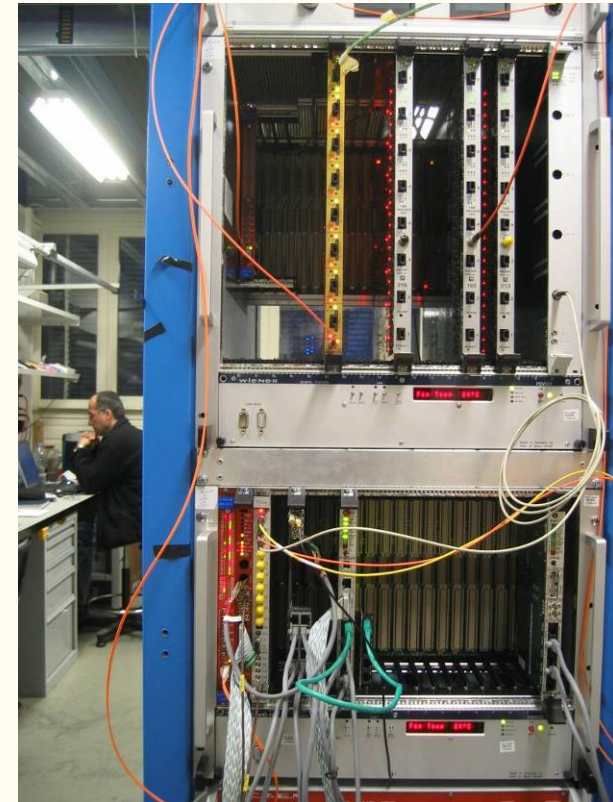
- 4 FEC crates
- 1 crate per partition
- 11 FECs per crate



# The CMS Tracker case



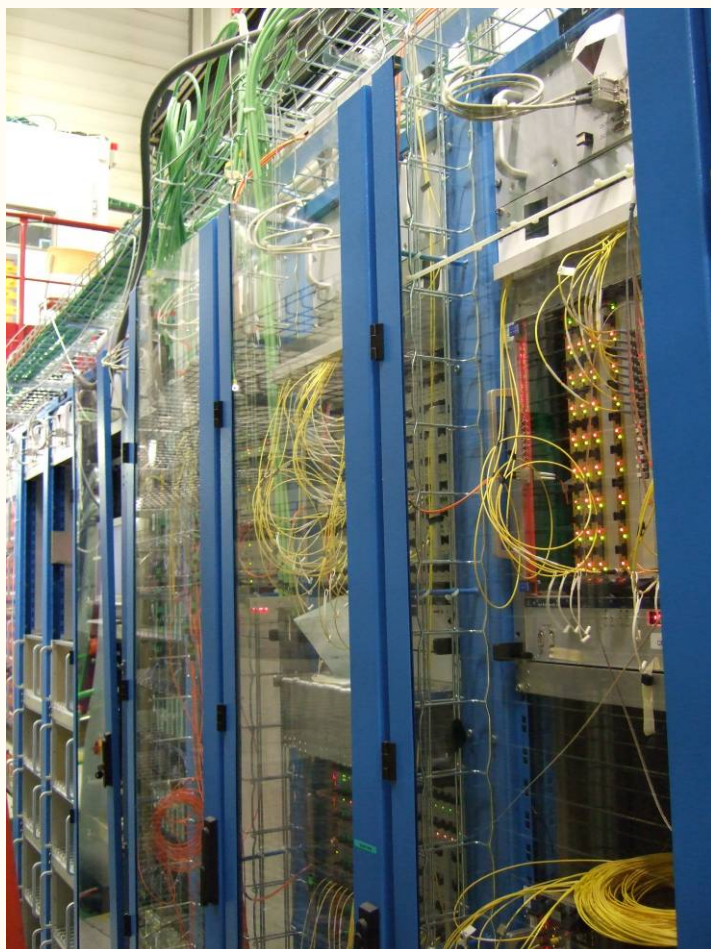
- Tracker electronics system setups:
  - Electronics System integration center, bldg. 904
  - Tracker Integration Facility (TIF), bldg. 186
    - TOB (Tracker Outer Barrel)
    - TIB (Tracker Inner Barrel)
    - TEC+ (Tracker End Cap +)
  - Aachen
    - TEC- (Tracker End Cap -)
  - Firenze/Pisa
    - TID (Tracker Inner Disk)
  
- MTCC test results
  - Validation of Front-End configuration procedures.
  - Validation of the Control Ring Redundancy.
  - Successful integration with the global TTC system.
  - Validation of the Tracker Trigger Throttling control loops.
    - APVE loop (APV emulator module)
    - FMM loop (TTS signals)



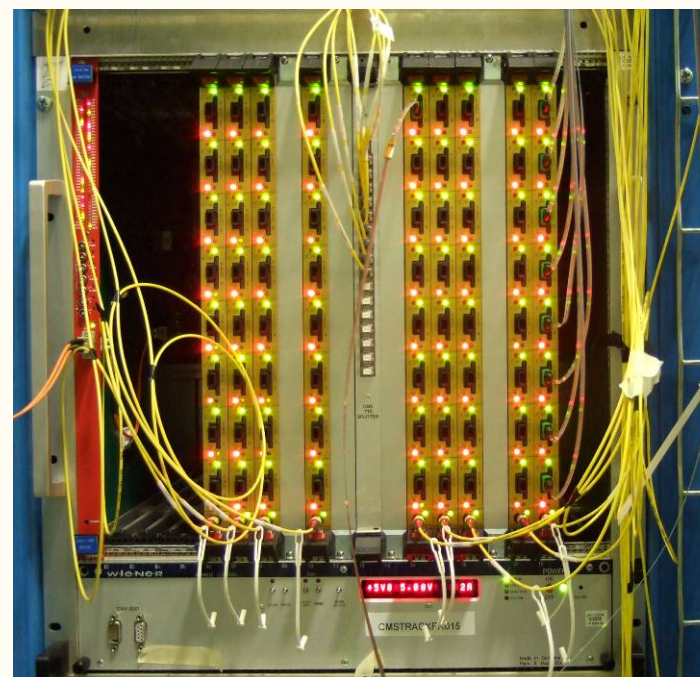




# The CMS Tracker case



## Tracker Integration Facility CERN building 186





# Other CMS subsystems



- Preshower
  - 20 FEC-CCS cards, 54 mFECs
  - Use of ECAL bus and special functions.
  
- PIXELs
  - 16 FEC-CCS cards, 80 mFECs
  - Special mFEC firmware for PIXEL specific Control Rings.
  - Special functions implemented on Trigger FPGA firmware.
  
- RPCs
  - 4 FEC-CCS cards, 25 mFECs
  - System used only for FE electronics control.
    - Timing distribution is done with on-detector TTCrx chips.
  
- TOTEM
  - 4 FEC-CCS cards, 16mFECs
  - Use of ECAL bus and special functions



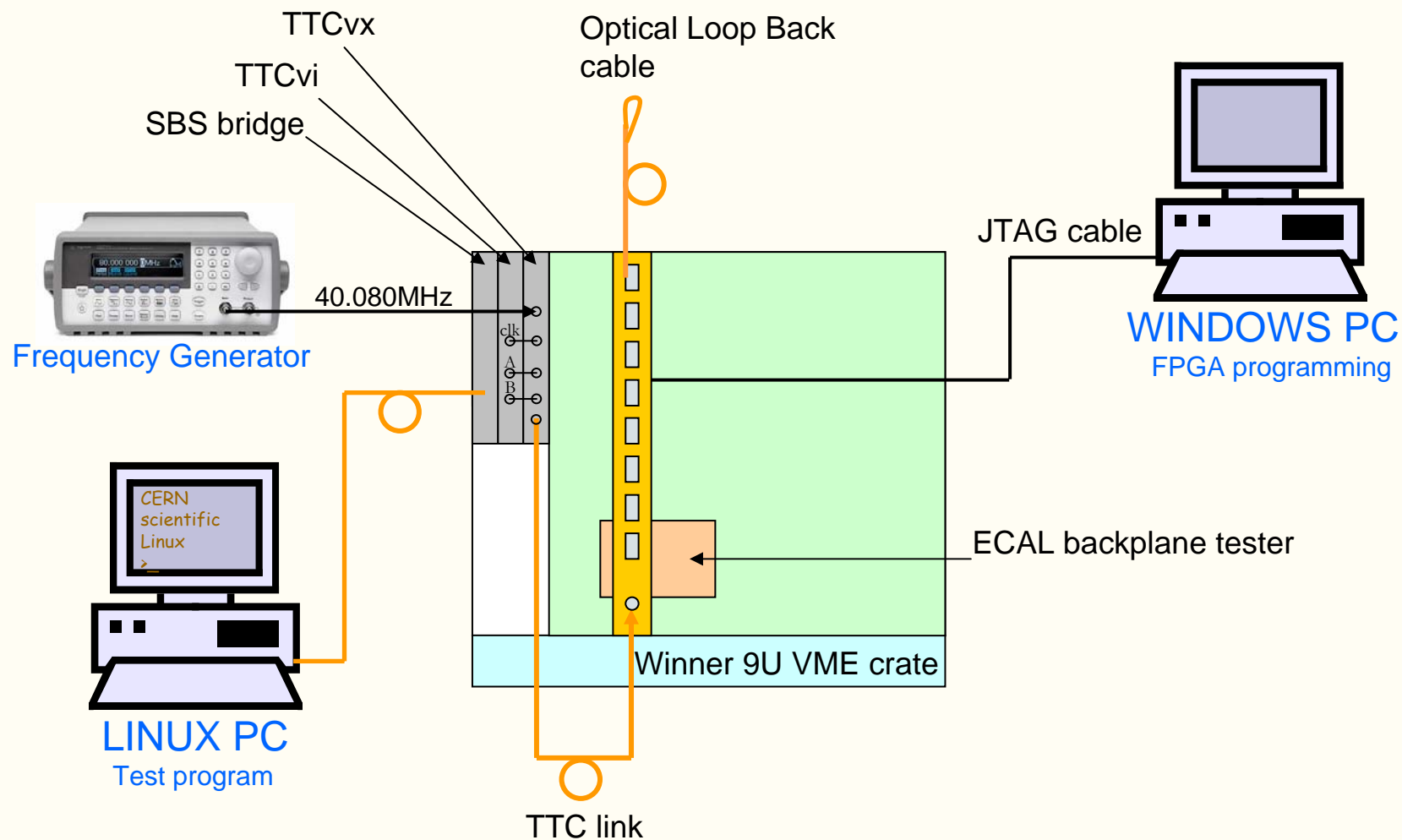
# FEC-CCS Production Testing



- In-house Production Testing.
  - CERN ECAL Lab. Bldg. 11.
  
- Custom made production test bench.
  - Test bench hardware based around a VME crate.
  - Test bench software prepared by Evgueni Vlassov.
  - Operated by a technician.
  - Same test bench used for both mFEC modules and VME FEC-CCS cards production testing.

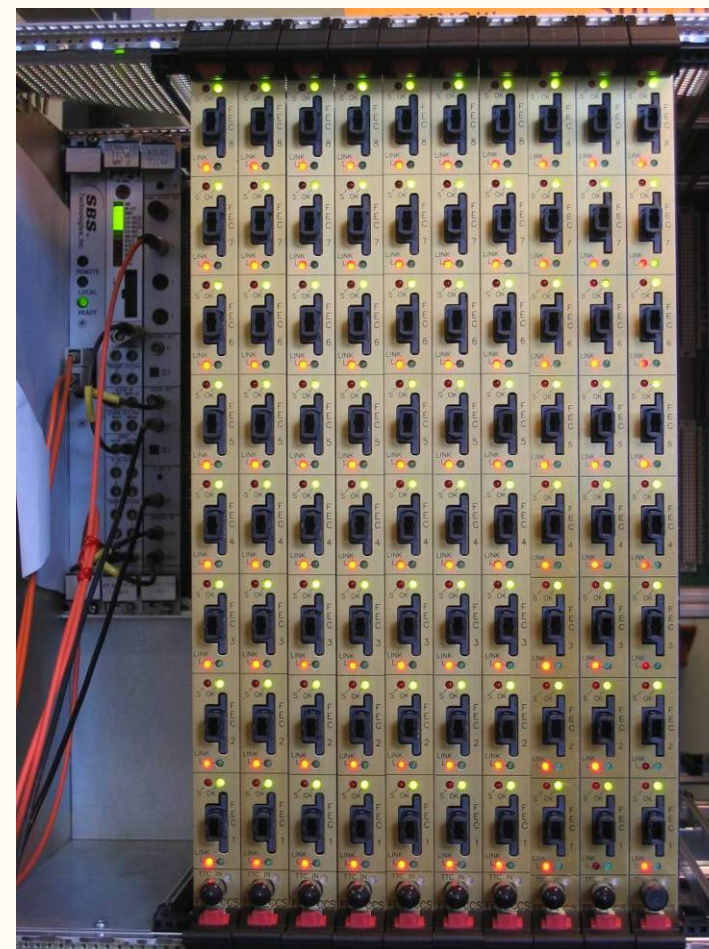
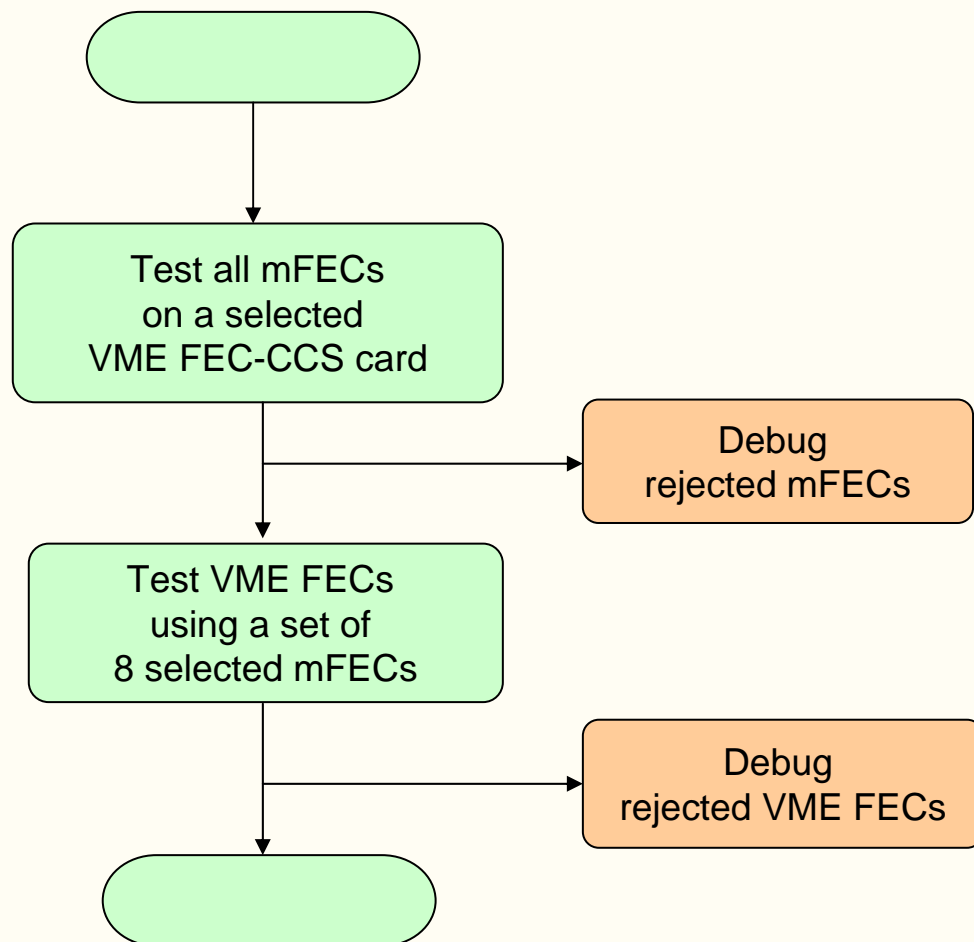


# Production Test Bench





# Production Testing Procedure





# FEC Production Status



- **mFEC Final Production: Completed**
  - **900 modules** tested.
    - 35 rejected modules
    - Post-production run of 50 modules to compensate
  
- **VME FEC-CCS Production: Testing in Progress**
  - **Pre-production volume: 40 boards**
    - Distributed to ECAL, Tracker, Pixels, Preshower & RPCs sub-systems to equip their DAQ test setups.
    - These boards will also be used to equip the final systems in CMS.
  
  - **Final production volume: 130 boards**
    - Assembled PCBs delivered at CERN
      - Production testing is in progress.
      - Estimated delivery period ~10/2006.



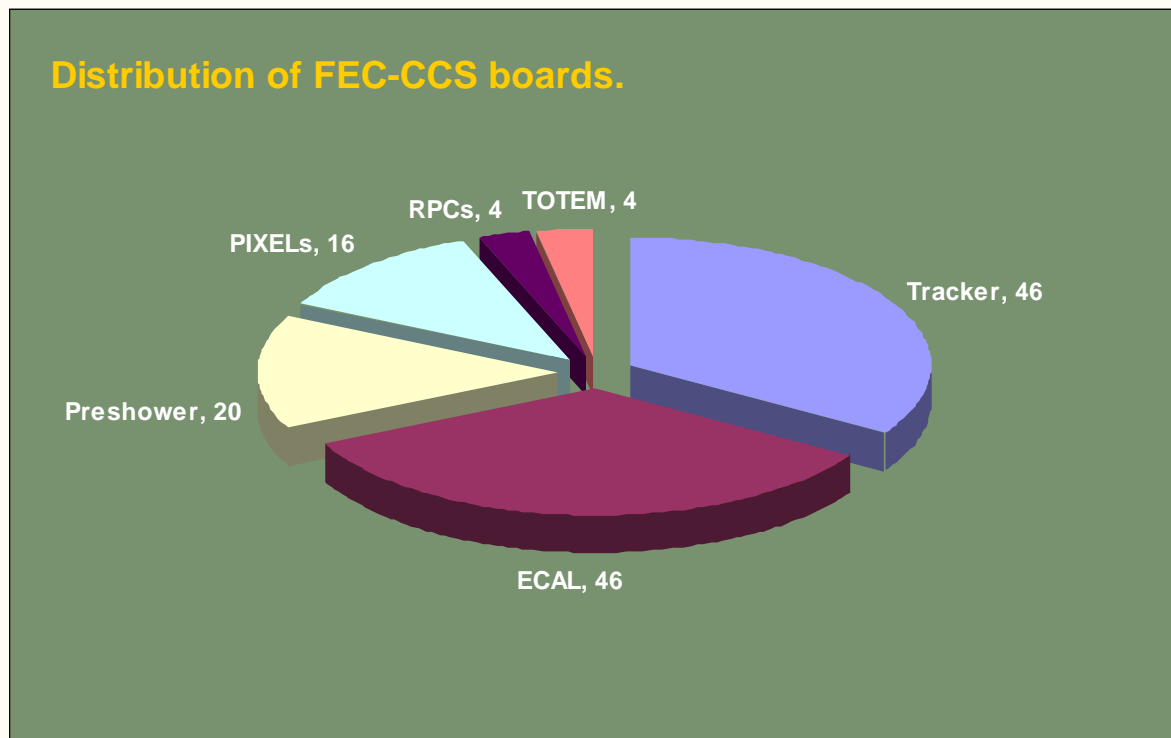
mFEC



FEC-CCS



# A common module for CMS



- 60 cards already distributed to the CMS sub-system groups.
  - Installed in various test systems at CERN and external institutes.
- PIXEL group received full production cards



# FEC Common Software



- FEC Common Software
  - ❑ Provide access to the common hardware
  - ❑ Facilitate Maintenance and User Support
  
- Features
  - ❑ Multi-Layered software.
  - ❑ Support several types of FEC hardware (PCI, VME, USB)
  
- FEC Common Software development team:
  - Frederic Drouhin (Tracker)
  - Laurent Gross (Tracker)
  - Evgueni Vlasov (ECAL)
  - Wojciech Bialas (Preshower)

Detector Run Control (Supervisor)

Subsystem Specific Software

- FEC Supervisor
- Configuration
  - DCU readout

Common Generic Library

Management of several Rings

Management of one Ring

Management of Hardware  
VME, PCI, USB

FEC hardware  
VME-FEC, PCI-FEC,  
USB-FEC





# FEC-CCS User Support



## ■ Hardware

- mFEC, PCI-FEC (optical, electrical), VME FEC-CCS cards.
- Support: CERN MIC group.
- Contact persons: Kostas Kloukinas, Christer Ljuslin and Christian Palliard.

## ■ Firmware

- Unique Firmware version for all the sub-systems to ease maintenance.
- New firmware releases fixes various system “glitches” and adds functionality.
- Anticipate to have firmware revisions during the subsystem integration and commissioning periods.
- Visit the FEC-CCS project Web Site for relevant information
  - <http://proj-fec-ccs.web.cern.ch/proj-FEC-CCS>
  - or GOOGLE it -> (FEC-CCS)

## ■ Software

- FEC Common Software support:
- Contact person: Frederic Drouhin
- Provide common software user support for:
  - Tracker, ECAL, Preshower, Pixels, RPCs & TOTEM.
- Web Page:
  - <http://x5oracle.cern.ch:8080/JSPWiki/Wiki.jsp?page=FECSoftware>



# Summary



- A common FE controller card for CMS sub-systems
  - Fulfils the requirements of the CMS sub-systems.
- Modular hardware design and flexible firmware to accommodate the different requirements.
- Successfully tested in numerous sub-system test setups.
- Production testing in final stage.
  - Boards are being delivered to CMS subsystems.
- Provide support during detector commissioning period.