Optical Module Front-End for a Neutrino Underwater Telescope: PMT interface

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On behalf of the NEMO collaboration

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Abstract

A proposal for a new system to capture signals in the Optical Module (OM) of an Underwater Neutrino Telescope is described. It concentrates on the problem of power consumption in relation to precision. In particular, a solution for the interface between the photomultiplier (PMT) and the front-end electronics is presented.

I. INTRODUCTION

An Underwater Neutrino Telescope uses large area PMTs to detect the Cherenkov light from the muons generated by neutrinos in the seawater. The PMTs are put in a 17" glass sphere at 350 Atm pressure. The signals detected by PMTs must by suitable coded and sent on-shore. A mini-tower equipped with 16 OMs will be deployed in 2006 in front of Catania arbour as a first prototype. It uses a front-end electronics described in [1]. Three main problems are not yet successful resolved: power consumption, PMTs aging and signal dynamics. To overcome these problems a different front-end electronics is proposed.

The research and development work aimed at the developing the low-power front-end for the Optical Modules (OM) of the NEMO submarine neutrino detector [2,3,4] has led to the design of different ASIC prototypes for the development of the Trigger, photomultiplier (PMT) signal classification and fast sampling according to signal classification. Moreover, commercial ADCs and a FPGA, provide digital encoding, data packing and then data transfer towards the shore station for acquisition.

A board containing the PMT interface electronics, the ASIC, the ADC and the FPGA constitutes the OM front-end. By means of the FPGA, this board receives the slow control and transmits the measurements of environmental parameters such as temperature, humidity etc. together with the data.

The final version of the chip has been tested and the single blocks, constituing its architecture, that is, the analog memory, the trigger and single photon classifier and the clock frequency multiplier, have been characterised. The board to test the whole front-end together with the PMT is being prepared.

II. THE FRONT-END

The design of the front-end board and the chip, in particular, are based on parameters and specifications which in some cases are not yet definitive and restrictive, for the performance of the whole detector.

Recently data coming from simulations of high energy neutrino events produced in a submarine detector became available for analysis. These data provide the signals of all the PMTs in the detector in the presence of such events and take into account the ^{40}K background, the optical properties of the sea water, the orientation and position of the PMTs etc. Therefore, using these data, it was possible to define new specifications for the front-end electronics that optimise the detector performances from the front-end point of view. As a result a new architecture has been defined for the chip that performs the sampling.

This new device, called Smart Autotriggering Sampler (SAS), will be composed of functional blocks very similar to those already designed and succesfully tested. This will allow the performance of the blocks to be introduced into the simulations of the whole front-end making the results more significant and realistic[4]. The block diagram of the front-end under design is shown in figure 1. One fundamental part is the PMT interface with the board. It allows the de-coupling, amplification, filtering and delay of the signals, with low power dissipation and with the maximum design reliability and compactness.

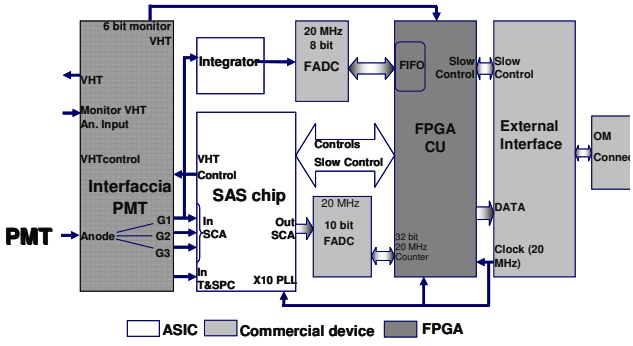

Figure 1 Front-end electronics block diagram

The present work concentrates on this part of the front-end, the PMT interface.

III. SIGNAL SIMULATIONS

From the results of the simulations of high energy neutrino events in a detector, like NEMO, various important points emerge:

- Three main pieces of information must be extracted by the front-end:

- The signal arrival time, with resolution lower than 1 ns;
- The charge of the signal from the PMT with very high resolution;
- The shape of the signal.

- The front-end must have the following characteristics:
  - Wide input dynamics, since the signals to be sampled have a very wide dynamic range according to the signal time duration, that is 1000 photoelectrons (pe) in 500 ns and 10000 pe in 10μs;
  - Negligible dead time. The presence of the single pe background due to spontaneous decay of the ^{40}K present in the seawater, with an average rate of 50 KHz imposes a suitable memory channel depth and a precise relationship between the sampling and conversion frequencies.

IV. THE PMT

The considerations and simulations are related to the 10" PMT selected for the NEMO experiment. The selected gain is $5 \cdot 10^7$.

The PMT base is active and provides single pe signals on an anodic load of 50Ω of about 50 mV amplitude with a rise time of about 2.6 ns. The PMT signal amplitude linearity is up to about 100 pe. Due to the signal frequency spectrum and the resolution required for the measurement of the arrival time we chose to sample the signal at 200 MHz with analog memories. This value is a good compromise between dissipated power and the quantity of samples taken for every signal.

The conversion of each sample is effected by a commercial 10 bit 20 MHz ADC. A consideration must be made on the signal frequency band. It presents components above 100 MHz which can produce aliasing effects. Therefore the PMT signal must be filtered. Furthermore in order to increase the PMT signal amplitude it is possible to use a higher anodic load, for example 800Ω. This allows the gain of the PMT to be reduced, increasing the average life time of the PMT. To cover the wide signal dynamic range in the most linear possible way, a PMT interface is foreseen that provides an input impedance of about 800 Ω, signal filtering, reducing the components above 100 MHz to -60 dB and, in three channels with different gain, produces three signals with different amplitude but identical shape. The three gains have been derived from the simulations in order to use three dynamics of 1 volt that cover signals of up to 512 pe. For istance, the first channel is direct, the second is reduced by a factor 8 and the third by a factor 64. Each channel has a suitable buffer to drive the delay lines and the load of the analog memories. The delay is essential and is of the order of 30 ns: from the moment in which the signal cross a suitable threshold a time interval is required for its classification and the beginning of the appropriate sampling of the signals according to their classification. Integrated delay lines will be used, greatly reducing bulk and having a greater mechanical robustness compared to the classical delay lines made with coaxial cables.

Other specifications are the 3.3 V power supply and the low-power dissipation. As a result of the former each channel has to be protected from PMT signals that go over the 3.3 V. The second channel, having a gain of 1/8 can, for example, sustain signals of up to 24 V. For this reason a switch has been introduced into every amplification branch with a fast JFET that excludes the amplifiers from the signal setting it to high impedance as soon as the voltage at its input goes over an adjustable threshold. This threshold is related to the threshold voltage of the JFET and to its externally applied gate voltage. The selected JFET introduces very low parasite capacitances making it possible to limit the input signal bandwidh to about 40 MHz at -3 dB, allowing the use of a low power operational amplifier with 3.3 V single supply whose power consumption is of about 5 mW. In figure 2 the circuit schematic of the interface board is shown.

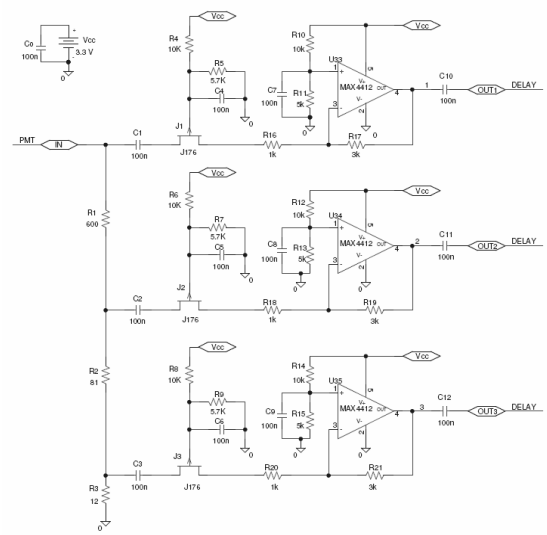

Figure 2 Schematic view of the PMT interface.

In figure 3 a picture of the PMT interface board is shown.

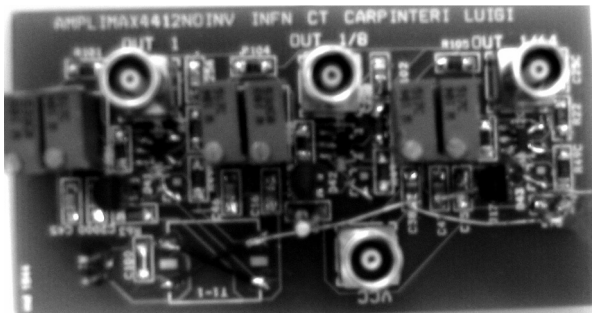

Figure 3 A picture of the PMT interface board.

It has been designed and tested with the NEMO selected PMT in a dark box using a laser to produce light. The typical signals of the three channels in presence of a signal of single pe are shown in figure 4.

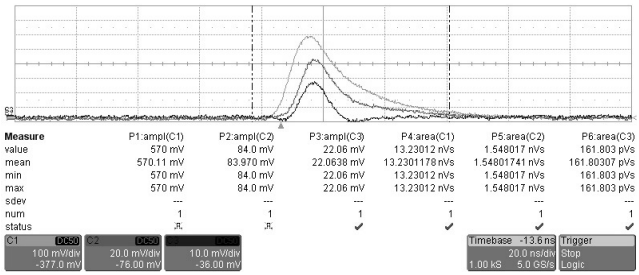

Figure 4 Single pe signal output of the PMT interface board.

In figure 5 the three channels in presence of a signal of PMT of 27 pe are shown. There it is shown how the first channel is saturated and the second presents an exact replica of the PMT signal attenuated of a factor 8 while in figure 6 the output of the board corresponding to 81 pe are shown. Finally in figure 7 all the three channel are in saturation.

The single photelectron signal output is of about 570 mV *and we want to have a voltage dynamic range of 1 V corresponding to 8 pe. So the gain of the PMT must be* lowered by a factor of about 5 which means $1 \cdot 10^7$.

The rise time of the signals is of about 9 ns as a result of the filtering of the signal. This will avoid aliasing effect in the 200 MHz sampling performed by the analog memories.

The values of gain of the three output channels are easily settable by adjusting the resistor ladder at the input. The power consumption of the PMT interface board is of 8 mA at 3.3 V. The board could also work very well with power supply as low as 2.7 V.

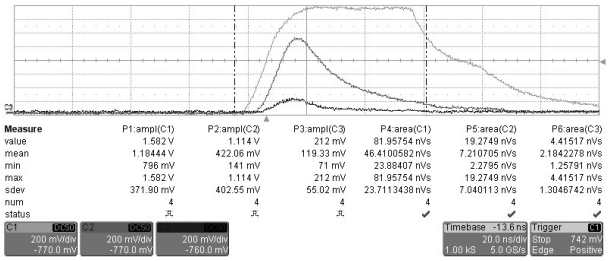

Figure 5 27 pe signal output of the PMT interface board.

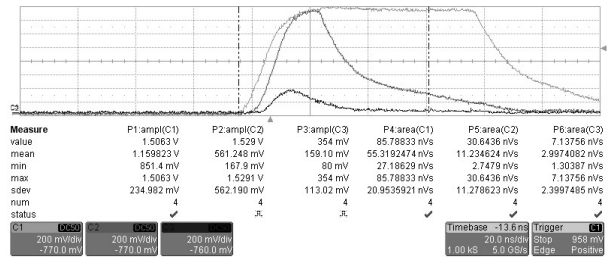

Figure 6 81 pe signal output of the PMT interface board.

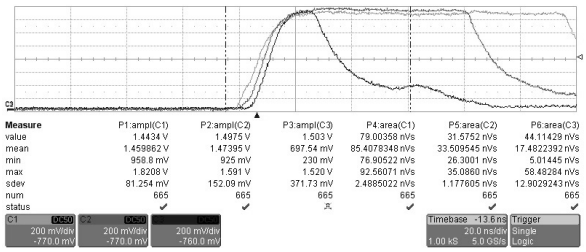

Figure 7 Saturation of all the PMT interface board output.

V. CONCLUSION

A proposal for a system to capture signals in the Optical Module of a Underwater Neutrino Telescope has been described. It pays great attention to the problem of power consumption with relation to precision. All considerations regarding the signals and their acquisition are made starting from the most general hypothesis possible, so that they will be valid for any Underwater Cherenkov Neutrino Telescope.

The development of the PMT interface board to meet the specifications of power dissipation, filtering properties, anodic load and required gain estabilishes the basis for the definitive design of the SAS chip. As soon as the chip is available, the whole front-end will be tested together with the PMT.

The PMT interface board will, in the meantime, be tested together with the preceding version of the front-end.

VI. REFERENCES

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