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Low-power front-end for a Neutrino Underwater Telescope

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The work described here has been developed in the context of the NEMO Collaboration with the aim of studying and designing a front-end electronics for the Optical Modules, which contain the telescope optical sensors, as a full-custom Very Large Scale Integration ASIC. The solution has a multitude of advantages.
The most important are low power consumption and the preanalysis and suitable reduction of data to be transferred to the shore station for acquisition. A detailed description of the chosen architecture and the design principles of the blocks, that carry out the specialized function required by this architecture, will be given.

Summary

A proposal for a system to capture signals in the Optical Module of an Underwater Neutrino Telescope is described.
An underwater neutrino telescope detects the muons produced by the interaction of neutrinos with the nuclei of matter along the path through the Earth.
These, emerging from the bottom of the sea and passing through sea water, produce light due to the Cherenkov effect.
The detection of the tracks allows the direction and energy of the primary neutrinos to be reconstructed.
The detector sensors are large area (>8")photomultipliers (PMT) in pressure resistant borosilicate glass spheres called Optical Modules (OM).
These also contain the high voltage power supply device, the front-end electronics and the required data transfer and communication unit.
There is a large number of OMs, about 6000, and the power they require is a key element when considering the feasibility of such a detector.
In the experimantal conditions the power transfer is limited, the electronics power consumption must be limited to not more than a few kW in the whole detector, that is less than 200-300 mW in the OM.
Power is transferred to the whole telescope at a great distance from the shore by means of an electro-optic cable and is limited by cable capacity.
Anything which is commercially available and satisfies the technical and power consumption requirements will be adopted in the OM.
Not included in this forecast are: the Switched Capacitor Array Analogue Memory to capture the signal (LIRA), the module which triggers and classifies the signals, the T&SPC, the synchronous frequency multiplier (PLL), the

Control system, the DC/DC conversion system that supplies power starting from the single one that enters from the connector.
The front-end electronics, therefore, have to have low power consumption.
The aim of the Catania Microelectronics group is to design a full custom VLSI ASIC containing as many circuital blocks as possible in order to reduce the total cost of the electronics, utilizing commercial devices for the other blocks.
In the following the blocks which are present in the chip will be described in more detail.
In particular, a device to capture the electric signals of the PMT must perform suitably.
These signals have a very wide dynamic range and a lot of care has to be devoted to the design of the device with the aim of its being able to respond to the need to acquire all the PMT signals adequately.
An accurate analysis of the signal shapes and careful design of the front-end architecture must guarantee the efficiency and precision of the electronics in capturing the signals in very low power conditions.
The design of the Smart Autotriggering Sampler (SAS) chip is the final result.
It is introduced in this presentation together with the simulation results.
A proposal for a system to capture signals in the Optical Module of a Underwater Neutrino Telescope has been described.
It pays great attention to the problem of power consumption with relation to precision.
All considerations regarding the signals and their acquisition are made starting from the most general hypothesis possible, so that they will be valid for any Underwater Cherenkov Neutrino Telescope.

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