Signal Integrity Analysis of High-Speed Interconnects

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Abstract

LHC detectors and future experiments will produce very large amount of data that will be transferred at multi-Gigabit speeds. At such data rates, signal-integrity effects become important and traditional rules of thumb are no longer enough for the design and layout of the traces.

Simulations for signal-integrity effects at board level provide a way to study and validate several scenarios before arriving at a set of optimized design rules prior to building the actual printed circuit board (PCB).

This article describes some of the available tools at CERN. Two case studies will be used to highlight the capabilities of these programs.

I. INTRODUCTION

Increasing clock-speeds and decreasing signal rise- and fall-times means that printed circuit board (PCB) traces on typical high-speed designs can no longer be considered as perfect point-to-point connections. Typical signal-integrity effects can lead to crosstalk, reflection and power-distribution noise problems that can cause false signal switching. These problems are exacerbated with the introduction of vias or other discontinuities.

It becomes necessary to provide more accurate models of interconnects and associated discontinuities on a typical PCB. Electromagnetic field solvers can be used to provide very accurate representations of interconnections but they are time- and compute-intensive to obtain so can only be used to characterise relatively small regions of the design. Using such a method for a full board simulation is impractical. To overcome this problem, the electromagnetic tool derived model is typically extracted and used in a conventional circuit simulator to analyse signal-integrity effects more fully.

Two examples will be presented. The first illustrates the design of an optimum low-mass cable which minimizes crosstalk between a pair of 2.5Gbps signals and the adjacent traces. The second case involves the study of the transmission of 1.6Gbps signals through via discontinuities within a 18 layer PCB stack-up.

The two case examples were analysed using commercially available programs to investigate if they could provide an efficient and practical way to take into account design aspects affecting signal propagation.

II. LOW MASS CABLE DESIGN

The Gigatracker is to be used in the proposed NA48/3 experiment as part of the high performance hodoscope to track a high density beam of one thousand million particles per second [1]. The Gigatracker Low Mass Cable **(**LMC) is used to bring data outside the high radiation environment for digital processing.

A. Low Mass Cable

Gigatracker's LMC is designed as a 3-layer PCB on an aluminium/kapton substrate [2]. The initial proposal for the design of the LMC is shown in Figure 1.

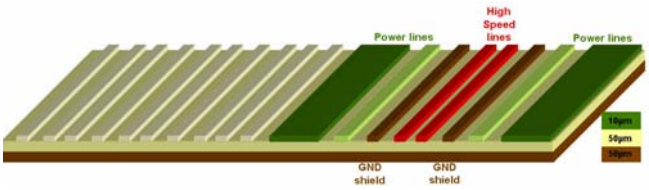


Figure 1: LMC initial design proposal

High-speed data (running at 2.5Gbps), control information (at 40MHz rate) and power are transferred through adjacent microstrip traces on the top layer of the LMC's PCB. In between signals, the initial design considers shielding (GND shield) to minimize the electromagnetic fields transfer to neighbouring traces.

B. Objectives

The Gigatracker design calls for an optimum LMC which minimizes signal integrity issues such as reflections and crosstalk.

Starting from the initial design proposal and taking into account given constraints, we focussed on how to find an optimum design for the LMC such that to reduce the coupling between different traces. Another objective was to extract a corresponding model for the LMC and use it in the HSPICE simulation of a full transmission channel incorporating a custom designed LVDS transceiver.

C. Constraints

One of the most important constraints of the LMC design, with direct impact on the amount of coupling and induced crosstalk, is the imposed maximum limit of 10mm for the cable's width. Due to this, the crosstalk cannot be reduced by placing the traces further away from each other. Other constraints of the design were accounting for a fixed 3-layers PCB stack-up build with aluminium as conductive material for low material budget, and with kapton as dielectric due to its mechanical flexibility.

D. Strategies

Theory states that the coupling between adjacent traces is influenced by the distance and the shielding. The analysis focussed therefore on crosstalk minimization by studying the influence of the shielding and the effect of bringing the power lines closer to the signal traces.

E. Tools and Methodologies

The HFSS electromagnetic field solver from Ansoft [3] was used to analyse and provide verified rules to be applied in the design of the LMC.

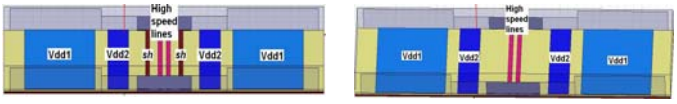
In order to be able to compute Maxwell's equations in the frequency domain using Finite Element Method, HFSS requires a 3-D geometry problem description, the specifications of the electromagnetic characteristics of materials composing the geometry, the setup of the excitation ports and the boundaries along with the required frequency bandwidth and the desired computation accuracy.

The program uses an adaptive mesh refinement algorithm to discretize the geometry into small mesh elements - such as tetrahedrons - in the 3D space. Maxwell's equations are computed within each individual mesh element for different frequency points. The final solutions from HFSS are represented by electromagnetic fields, Scattering-parameters and impedance values, all results being obtained after interpolating the individual values computed within the previously user-defined frequency range.

F. HFSS Results

The HFSS results for the LMC design presented in this section are obtained over a frequency range from 100MHz to 25GHz.

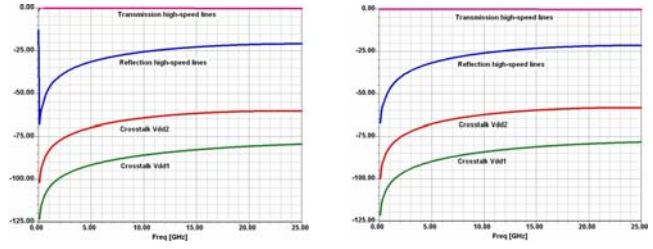
HFSS was used to analyse the LMC geometries with and without the shielding traces to examine their influence on the induced crosstalk from the high-speed signals into the power lines (Figure 2 a. and b.).



a.) shielding b.) No shielding

Figure 2: LMC geometry

The Scattering-parameter results, in terms of transmission through the high-speed lines, reflection at the incident port and crosstalk into the power line Vdd2, respectively Vdd1 are presented in Figure 3 a. and b.



a.) shielding b.) No shielding

Figure 3: S-parameter results from HFSS

The crosstalk induced into the closer power line Vdd2 stays below a level of -60dB at 25GHz; this corresponds to a level of induced noise of less than 0.1%. By removing the shielding, the crosstalk, induced into the same line, increases with 2dB (0.125%), value which is still considered very low. From these results we could conclude that the influence of the shielding on the overall crosstalk level is minimal. A first design rule would therefore suggest building the LMC without the shielding. This, in turn, will result in an important economy of aluminium material.

We further studied the impact of bringing the power lines closer to the high-speed signals. The geometry analysed and the corresponding S-parameters for this case are shown in Figure 4 and Figure 5.

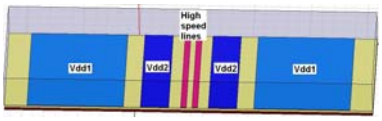


Figure 4: New LMC geometry

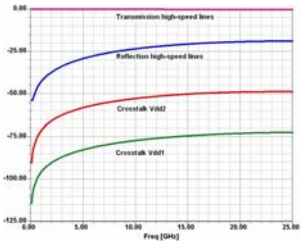


Figure 5: S-parameter results

In this case, the crosstalk induced from the high-speed lines into the power increases evidently more. However, a value of -47dB at 25GHz could be considered acceptably low. A second design rule suggests therefore bringing the power traces closer to the serial lines. This would allow the final LMC to be even narrower than the designer imposed constraint.

G. Time-domain Results

The previous results from HFSS can also be made available to other simulators via the implemented Spice-extraction scheme or through Touchstone export.

The resulting equivalent full-wave model provided by HFSS was exported to HSPICE and simulated as part of a larger electrical circuit. The extended transmission channel from the read-out chip to an ideal receiver, across the LMC, is shown in Figure 6. The read-out chip on the detector is a custom ASIC design realized by the MIC group at CERN.

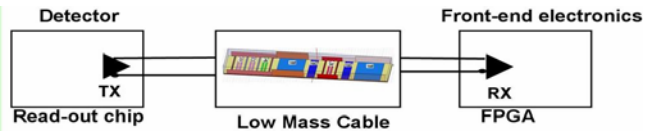
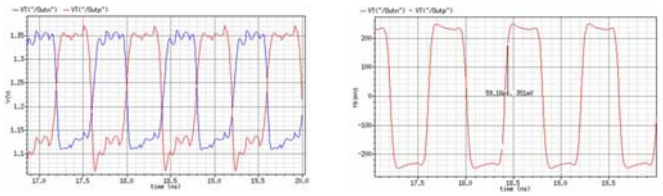


Figure 6: Simulated transmission channel

The time-domain simulations were performed in Cadence Specctre and the single-ended and differential results seen at the receiver are shown in Figure 7.



a.) Single-ended b.) Differential

Figure 7: Time-domain simulation results

The simulation shows very good signal characteristics: the rise time is not degraded and the desired amplitude level is reached after switching with no obvious ringing present in the received signal.

H. Conclusions

Starting from an initial design proposal, we highlighted the usefulness of a 3D electromagnetic field solver such as HFSS. By employing frequency-domain modelling in the analysis of different configurations, we developed pre-layout analysis rules to be followed for an optimum design of the LMC. An accurate SPICE model, extracted from the field solver analysis, was used to simulate and estimate in the time-domain the signal transmission quality between the read-out and the processing electronics using the LMC.

III. PCB VIA DESIGN

At increasing clock-speeds and decreasing signal switching times, it becomes necessary to provide accurate modeling of vias and connectors, as part of an usual PCB design.

A. Differential pair of vias

As a concrete example, we look into the design of an inter-layer connection represented by a differential pair of vias built within a 18 layer PCB stack-up. This via structure, shown in Figure 8, is used to pass LVDS signals at 1.6Gbps from one layer to another of the muon trigger processing board used in the LHCb experiment [4].

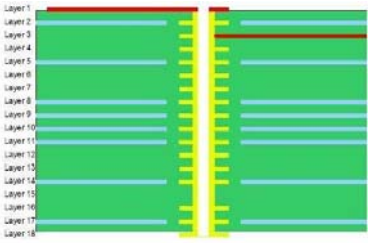


Figure 8: Differential pair of vias within the PCB stack-up

B. Objectives

While PCB interconnects, such as microstrip and stripline, can be modelled accurately using 2D solvers, the complexity of via interconnects warranted deeper study and therefore requires the use of 3D electromagnetic programs. Our goal throughout this exercise was to model the vias throughout the electromagnetic analysis and then to incorporate the obtained model within a full-transmission channel simulation at the circuit-level.

C. Tools and Methodologies

The differential via geometry was analyzed using 3D electromagnetic field simulation in Microwave Studio from CST [5]. Microwave Studio (MWS) is an electromagnetic field solver based on Finite Integration Technique, method which solves in the time-domain the integral form of Maxwell's equations. For this, MWS requires the input of the geometric model, the materials' definition, the boundaries' specification and the setup of the signal ports.

The main results from MWS are transient (time-domain) fields and signals, allowing a direct study of possible signal integrity issues without an immediate need for a SPICE simulation. MWS also provides the electromagnetic field distribution and the S-parameters of every port at any given frequency.

D. MWS Results

We analyzed with MWS the following 3D geometry (Figure 9) which includes a differential pair of signal vias and their adjacent via connections to the analogue, respectively the digital ground planes within the PCB's stackup.

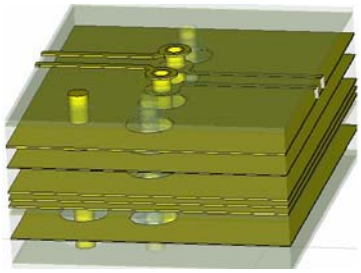


Figure 9: Differential vias geometry in MWS

MWS analyses the structure by applying a Gaussian signal automatically defined according to the user-specified frequency range. The structure's response to a pulse excitation is obtained through post-processing based on the original Gaussian simulation response. The resulting pulse signals are presented in Figure 10.

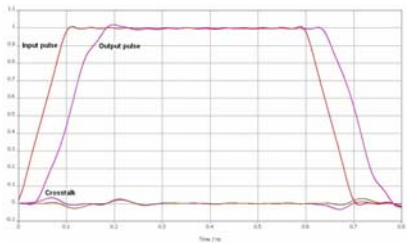


Figure 10: Time-domain pulse signals from MWS

The pulse transmitted through the via maintains good signal integrity characteristics: no obvious ringing is present, the steepness of the slope of the rise- and the fall-times is maintained and the induced near- and far-end crosstalk between the two vias is minimal (3 %).

From MWS we can also indirectly obtain the S-parameters for the studied via geometry (Figure 11).

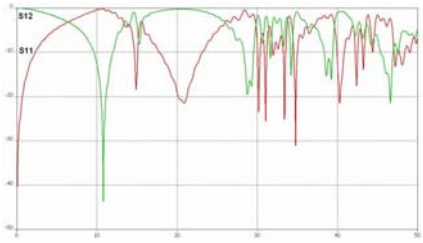


Figure 11: Time-domain pulse signals from MWS

The transmission (S12) and the reflection (S11) parameters show that via inclusion has little effect up to a frequency of 7GHz.

E. Time-domain results

The results obtained from a MWS computation gives a first indication of the signal integrity characteristics of the studied via geometry. However, on a real PCB, a signal is transmitted not only across vias but along a whole channel including different lengths of transmission lines and other discontinuities. All these elements must be included to give a more realistic estimation of the final signal arriving at the receiver.

In order to simulate the entire transmission channel, the via model was exported to HSPICE. A simplified representation of the final simulated circuit is shown in Figure 12.

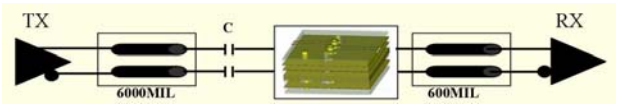
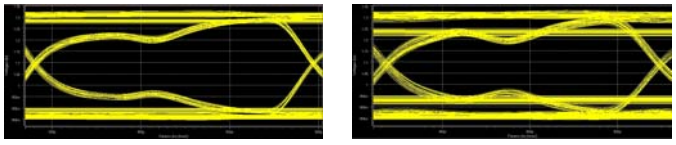


Figure 12: Simplified transmission channel on the PCB

HSPICE models were obtained for the Altera StratixGX FPGA transmitter and receiver. The transmission lines were modeled as W-elements using the Cadence Allegro PCB SI 2D solver [6]. The complete channel was simulated with and without the via models extracted by MWS. The resulting eye-diagrams seen at the receiver input are plotted in Figure 13.

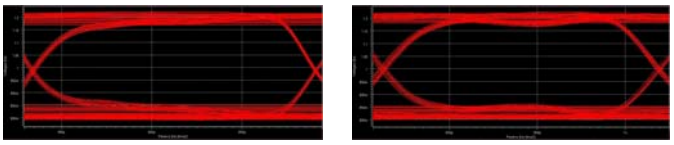


a.) No vias b.) Vias from MWS

Figure 13: Eye-diagrams before the receiver's package

The eye amplitude diminishes for the case in Figure 13.b due to energy loss in the reflections encountered at the via discontinuity. Both plotted eye-diagrams show a 'pear shape. This is probably caused by a reflection at the receiver die returning back along a short transmission line length (representing the chip package) to the receiver external pins where it sums with the original incoming signal.

The eye-diagrams at the receiver die were also examined (Figure 14).



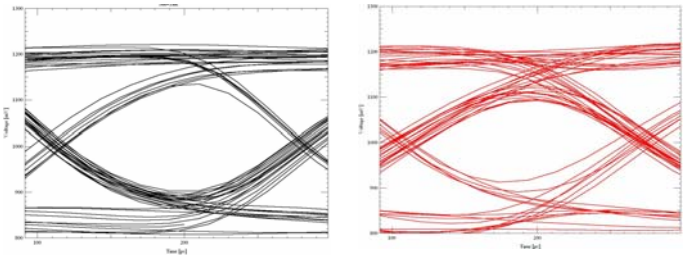
a.) No vias b.) Vias from MWS

Figure 14: Eye-diagrams after the receiver's package

The previous 'pear' shape completely disappears as no negative reflection affects the signal at this point. In addition, we note that the receiver's capability of recovering the incoming signal makes little difference for the cases with and without the vias. Close inspection reveals a slight vertical closure in the middle of the eye for the channel including vias (Figure 14. b).

It appears that the via influence on the overall quality of the transmitted signal is almost negligible on the LCHb processing board. Indeed, a 1.6Gbps signal has spectrum components at a maximum frequency of 4GHz (5^{th} order frequency component) and the S-parameters of this via show excellent characteristics up to 7GHz (see Figure 11).

This via will start however degrading faster signals. To illustrate such a case, we increased the data rate from 1.6 to 6Gbps and simulated the same channel with and without the vias. The results at the receiver's die are presented in Figure 15.



a.) No vias b.) Vias from MWS

Figure 15: Eye-diagrams after the receiver's package

The via's contribution manifests itself as a reduction in the eye amplitude and increase of the added jitter.

F. Conclusions

The differential vias geometry was analyzed using CST Microwave Studio. The time-domain results from MWS have given a first indication of the quality of the transmission through this structure. The resulting model of the geometry was exported to HSPICE where a complete transmission channel was simulated with satisfactory results. We concluded that the signal running at 1.6Gbps on the LHCb processing board can be properly recovered despite the vias discontinuity.

Throughout this example we presented a practical simulation methodology which can be applied for the analysis of any PCB discontinuities. Using this method we verified, through simulation in post-layout, that the overall quality of the received signal corresponds to the specifications and we showed that the current via design has minimal influence on the 1.6Gbps signal running on the LHCb processing board.

We have also shown how the signal would deteriorate if the switching rate was increased.

IV. FINAL CONCLUSIONS

Throughout the two examples presented in this paper, we showed how using commercially available programs provides an efficient and practical way to study signal integrity effects and to help minimise the number of design iterations for completing projects within time and budget constraints. These tools are readily available and supported at CERN.

V. REFERENCES

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