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Signal integrity analysis for the electronic design of printed circuit boards

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LHC detectors and future experiments will produce very large amount of data that will be transferred at multi-Gigabit speeds. At such PCB data rates, signal-integrity effects become important and traditional rules of thumb are no longer enough for the design and layout of the traces.

Simulations for signal-integrity effects at board level provide a way to study and validate several scenarios before arriving at a set of optimized design rules prior to building the actual PCB.

This article describes some of the available tools at CERN. Two case studies will be used to highlight the capabilities of these programs.

Summary

Increasing clock-speeds and decreasing signal rise- and fall-times means that PCB traces on typical high-speed designs can no longer be considered as perfect point-to-point connections. Typical signal-integrity effects can lead to crosstalk, reflection and power-distribution noise problems that can cause false signal switching. These problems are exacerbated with the introduction of vias or other discontinuities.

It becomes necessary to provide more accurate models of interconnects and associated discontinuities on a typical PCB. Electromagnetic field solvers can be used to provide very accurate representations of interconnections but they are time- and compute-intensive to obtain so can only be used to characterise relatively small regions of the design. Using such a method for a full board simulation is impractical. To overcome this problem, the electro-magnetic tool derived model is typically extracted and used in a conventional circuit simulator to analyse signal-integrity effects more fully.

Two examples will be discussed.

The Alice Silicon Pixel Detector design calls for an optimum low-mass cable which minimizes crosstalk between a pair of 1.6Gbps signals and the adjacent traces. The HFSS electro-magnetic field solver from Ansoft was used to analyse this cable and provide such a design. The extracted corresponding model was subsequently used to simulate in HSpice a full transmission channel incorporating a custom designed LVDS transceiver.

The second case involves the study of the transmission of 1.6Gbps signals through via discontinuities within a 18 layer PCB stack-up. A prototype board had already been designed for the read-out chain of the LHCb experiment using the Cadence SI-tools. These programs can give sufficiently accurate results for reasonably complex designs but in this case, it was thought that the complexity of the via interconnects warranted deeper study. Electromagnetic field solvers were again used for further analysis.

In conclusion, these two case examples show that reliable high-speed PCB digital design needs to take into account all design aspects that will affect signal propagation. These can be examined using commercially available programs to provide an efficient and practical way to study signal integrity effects.

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