The ALICE Silicon Pixel Detector Control System and Online Calibration Tools

I.A. Cali[a,b], M. Caselle[a], S. Ceresa[b], A. Kluge[b], M. Krivda[b,c], P. Riedler[b]
H. Tydesjo[b], C. Torcato De Matos[b]

on behalf of the Alice SPD project

[a] Dipartimento di Fisica e Sez. INFN di Bari, I-70126, Bari, Italy
[b] CERN - European Organization for Nuclear Research, CH-1211 Geneva 23, Switzerland
[c]Institute of Experimental Physics, SK-04353, Kosice, Slovakia

ivan.amos.cali@cern.ch

Abstract

The ALICE Silicon Pixel Detector (SPD) contains nearly 10^7 hybrid pixel cells. The operation of the SPD requires on-line control and monitoring of some 2000 parameters and $\sim 50000 DACs$. Information for each channel is stored in a configuration database. Timing and data management ($\sim 6GB$ of raw data each calibration) are critical issues. An overview of the SPD electronics read out chain and of the detector control system is given with a detailed description of the front-end controls and the calibration strategy. The status of commissioning and a preliminary evaluation of detector performance are presented.

I. Introduction

The operation of the ALICE Silicon Pixel Detector (SPD) requires the on-line control and monitoring of a large number of parameters. This task is performed by the SPD Detector Control System (DCS). The DCS also has a key role in the calibration of the detector. These combined functions increase the complexity of the system, whose main features are presented and discussed in the following sections.

II. Main features of the electronics system

The SPD (see Fig. 1) constitutes the two innermost layers of the ALICE Inner Tracking System (ITS) at radii of 3.9 cm and 7.6 cm respectively.
The detector consists of 120 half-staves (HS) mounted on 10 carbon fibre support sectors. An HS is an assembly of two ladders glued and wire-bonded to a multi-layer interconnect (the pixel bus) that distributes power and signals. Each ladder consists of 5 pixel chip ASICs [10], 150 μm thick, bump bonded to a 200 μm thick silicon sensor and contains nearly 41k active hybrid pixel cells with dimensions of 50 μm (rϕ) x 425 μm (z). A Multi Chip Module (MCM) [5] on each half-stave distributes the timing signals, provides the required analog references and performs data multiplexing and serialization. The communication between the MCM and the counting room is via optical links with three single-mode fibres. The front-end electronics clock speed is 10 MHz (heavy ion operation). The readout data stream uses a G-link compatible protocol with a 800Mb/s clock. Zero suppression and data encoding are performed in the Link Receiver mezzanine cards (LRx) in the VME based Router readout modules. One Router with three LRx cards [9] serves a half sector (6 half-staves) and has optical links to the experiment DAQ and trigger system.

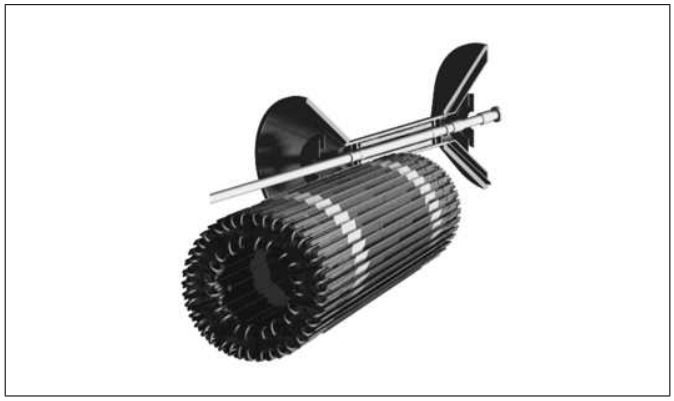

Figure 1: A draw of the full SPD

A unique feature of the SPD is that it can provide a prompt multiplicity trigger within the latency of the L0 trigger (850ns) [8]. The LV power supply requirements for the front-end electronics on each half-stave (HS) are 1.85V ($\sim 6A$) for the pixel bus and 2.6V ($\sim 0.5A$) for the MCM. The LV power supply (PS) system is based on 20 CAEN A3009 LV modules (12 LV channels each), housed in 4 CAEN Easy3000 crates located in the experimental area. Detector bias (50 $\div$ 100 V, $< 7\mu A$) is provided by 10 CAEN A1519 HV modules (12 HV channels each) housed in a CAEN SY1527 mainframe located in the counting room. The SY1527 communicate with the software layer via ethernet (TCP/IP). The SY1527 communication with the LV modules is via CAEN A1676 branch controller.
The FE electronics power dissipation is $\sim 1.3kW$. Cooling is based on an evaporative system with C_4F_{10}. The cooling plant provides one main cooling line for each SPD sector. Each line feeds 6 cooling capillaries, embedded in each sector, to which the staves are thermally coupled by means of thermal grease. The operating temperature of the detector is $\sim 25^oC$. The cool-

ing plant is controlled by a PLC. Communication with the control PC is via ethernet (TCP/IP) using OPC Server-client protocol. Efficient cooling is vital for this very low mass detector. If the cooling were suddenly switched off, the detector temperature would increase at a rate of 1 $^oC/s$. The detector temperature is therefore a critical parameter that must be monitored online and safety interlocks must be activated immediately. On each HS surface are mounted two series of 5 temperature sensors (Pt1000). One group of Pt1000 series (120) are read out via analog modules in a dedicated PLC that generates the corresponding temperature interlocks and sends online via ethernet the detector temperatures readout to the counting room.

III. Detector operation issues

The operation and performance of the SPD require a tight control of many parameters such as timing, the pixel bus power supply voltage Vdd, the reference voltages provided by an analog ASIC on the MCM (Analog Pilot [2]), and the settings of the various DACs in each front-end pixel ASICs. The objective of the SPD calibration is to adjust these parameters in order to obtain the highest efficiency and response uniformity of the pixels matrices. Dead and noisy pixel identification is performed as well during the calibration phase.
Calibration is mainly performed using test pulses (TP) that can be generated in each FE chip. The pulses can be set independently to each single pixel; the amplitude is programmable and is controlled by the Analog Pilot. The detector efficiency and the uniformity of response of the pixels matrices are studied by varying the pulse amplitude at various threshold settings (S-curves)[6].
The list of the noisy and dead channels is important for the offline particle tracks reconstruction.
As previously pointed out, the SPD has the capability to provide a prompt multiplicity trigger. This is the Fast-OR pulse that is generated in each pixel chip when a particle hit is detected. The Fast-OR contributes to the L0 trigger input to the ALICE Central Trigger Processor (CTP). Several calibration procedures are implemented using the TP and eventually the interactions:

a) Uniformity scan: a sequence of TPs is applied to each pixel with an amplitude $>$ 2 Mean Threshold of the chip. The uniformity of the response of the pixel matrix is determined from the efficiency distribution (ratio of hits to pulses).

b) DAC scan: a sequence of triggers is applied to the detector under test, using TPs or a radioactive source, while varying the references generated by the Analog Pilot and/or the DACs in the pixel chip. For each DAC value, the average efficiency of response and the average multiplicity are determined.

c) Mean threshold scan: the uniformity of the pixel matrix is studied by varying the TP amplitude. For each pixel, the efficiency of response is determined as a function of the DAC setting. The TP amplitude that gives an efficiency of 50 % represents the equivalent in voltage of the applied threshold.

d) Noisy and dead pixels identification.

e) Fast-Or characterization: a sequence of TPs is applied to one pixel at a time. The efficiency map of the pixel matrix is determined from the corresponding number of generated Fast-ORs.

Automated configuration calibration procedures are implemented in the Detector Control System that is also able to emulate the ALICE DAQ and trigger system.
The calibration raw data from the 1200 FE chips are analyzed online either by the DCS or by the DAQ system. The calibration sequence is iterated until the optimal parameter settings are determined. These settings, including FE chip DACs values, MCM chips configuration and power supplies voltages, are stored in an Oracle based configuration database. The configuration versions are tagged in function of the run (PHYSICS p-p, PHYSICS Pb-Pb, CALIBRATION, BEAM TUNING) for witch they will be applied.

IV. Control System

The system is based on a commercial Supervisory Control And Data Acquisition (SCADA) named PVSS. Five PVSS projects are running independently on different working nodes to control, respectively the cooling system, the Power Supply (PS) system, the interlock and monitor system and the FE electronics; the fifth project links together and monitors the 4 subsystem projects. In the future it is planned to integrate the control of the Pixel Trigger electronics in the SDP DCS as well. A block diagram that represent the HW/SW interconnection is shown in fig.2.

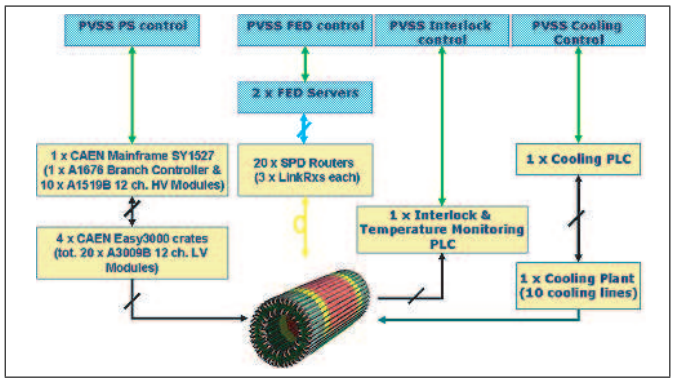

Figure 2: Block diagram that shows the SPD branches of the detector control system

Each main hardware branch is connected directly to an independent PVSS project that bridges the hardware with the logical control of the full system carried out through a Finite State Machine (FSM). The FSM is based on a State Management Interface (SMI++) capable of defining logical domains and links the different SPD sub-systems. The lowest FSM software layer is formed by Device Units (DU) providing the upper layers with an hardware state. The DUs are capable of sending instructions to the PVSS layer connected to them as child. The DU can be connected together either via Logical Units (LU) or via Control Units (CU) that generate states as functions of their children state. The LU and CU are sending commands to the underlying level on the FSM hierarchy. The CU and its children form a domain and can run autonomously on a different computer but the CU has higher RAM requirements (5 MB/DU) than a LU. The SPD FSM hierarchy is shown in fig.3.

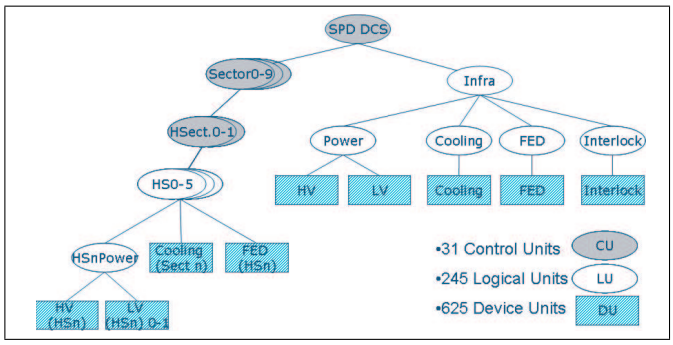

Figure 3: The SPD Finite State Machine hierarchy blocks diagram

The system comprises 31 CUs to place the detector partitioning at the half-sector level. This structure allows to debug a detector subset without interfering with the normal data taking. The SPD FSM contains 245 LUs and 625 DUs. The *SPD* node has 11 branches: one for the infrastructure and one for each sector. The children of the *Infra* LU are the DUs representing the status of the subsystem infrastructures. They are PS mainframe, crates, cooling plant etc. The READY state of the *Infra* is foreseen only when all the subsystem infrastructures are fully operative. If the *Infra* LU is not in ready status the SPD DCS top node sends the switch-off command to all the detector subsystems.
Each sector CU is partitioned in 2 half-sectors CU including 5 HS LUs. The HS LU retrieve information from the cooling system and switch off the power supplies in case of anomalies.
The HV and LV DUs are linked together via a LU (*HSnPower*) that provides the proper HS power-up and power-down sequence.
A set of macroinstructions is provided by the HS LU to the FE control DU that can execute monitoring, control and detector calibration. The SPD is ready for physics or for calibration when the on-detector and off-detector electronics is configured. Different sets of configuration parameters are making the switch between different SPD status such as i.e. calibration and physics.

Each PVSS software layer contains translator scripts capable of converting macroinstructions into the sequence of operations required for the hardware.
Background scripts monitor continuously the status of the hardware and take automatic actions to protect the system in case of abnormal states.
The PVSS layer controlling the PS system allows to upload the prescribed voltage settings in the SY1527 mainframe. The parameters are retrieved from a specific Oracle Configuration Db (CDB). All the voltages and currents are monitored online and archived during all the detector operation phases. An HS power-up and power-down sequence is foreseen to activate or deactivate sequentially MCM, detector bias (HV) and FE chips. The sequence is controlled via the FSM and PVSS background scripts are used for monitoring the status and taking corrective actions if necessary.

The FED DUs control two Front End Device (FED) Servers (C++ based), one for the detector side A and one for side C. The FED Server is a stand alone application consisting of three software layer. The top one hosts a Distributed Information Management System (DIM - TCP/IP) server that allows the communication with the PVSS layer. The intermediate FED application layer hosts all the logical functions required. It retrieves the commands received by the DIM server, checks the hardware status, pulls or stores, if required, the data from/to the database and communicates with the driver layer to apply the required operations to the hardware. The FED state machine is hosts in this layer. The bottom software layer is the driver for the VME access of the off-detector electronics.

The system structure allows fast remote operator intervention and is highly modular. The communication between the different software applications is via DIM. Most processes are fully automated in order to obtain the required reliability and safety of operation.
The power system (HV and LV) and the cooling systems are controlled directly by PVSS.
The FSM represents also the operator interface to the detector and allows the interconnection with the general ALICE DCS.

V. Calibration Procedures

The system is designed to allow fast and automated calibration procedures. The calibration of the full detector will be carried out during the LHC fill time ($\sim$ 70 mins); the updated configuration settings are calculated automatically.
Two calibration procedures can operate independently: DCS_ONLY and DAQ_ACTIVE. The DCS_ONLY procedure requires the emulation of the alice DAQ and trigger system by the DCS system. It is slower then the DAQ_ACTIVE during the data acquisition but allows the calibration and debug of a detector subset without interfering with the data taking of the other detector partitions.
The block diagram of the DCS_ONLY procedure is displayed in fig.4.

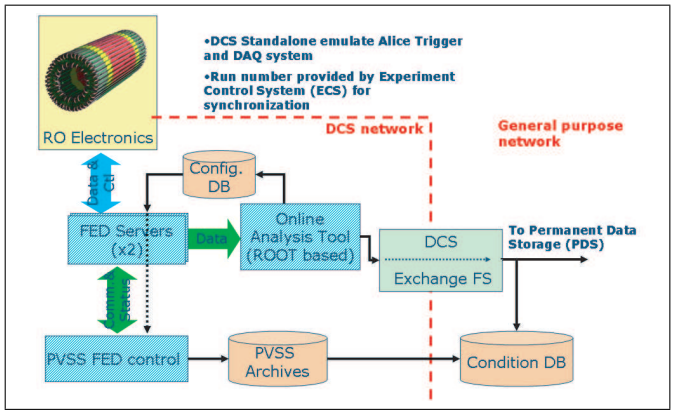

Figure 4: A block diagram of the DCS_ONLY calibration procedure

The routers data spy capability are enabled in this procedure and the main detector data stream is forwarded to an internal router dual port memory accessible via VME bus. The PVSS and the FED servers perform the detector configuration and status monitor. The routers then send triggers and data are

read back via VME by the FED servers acting as software data buffer. The detector data are sent to a ROOT based analysis tool. The tool defines the updated configuration and stores it in the CDB. The analysis results are stored in ROOT format files and forwarded to an Exchange File System (EFS) that allows the communication with the offline network and the Permanent Data Storage (PDS). The analysis tool is controlled and retrieves the configuration parameters needed for the data analysis by PVSS. The communication between the 3 software tools such as PVSS, FED servers and Analysis Tool is performed via DIM. When he calibration is completed the DCS moves automatically the FSM from the calibration state to a standby state. The ECS is the user interface to the detector in operation. The ECS controls the SPD subsystems such as DAQ, DCS and Trigger. In the DCS_ONLY calibration procedure, the ECS sends the calibration start command to the DCS and disables the other two subsystems. A new run can be started only when the DCS leaves its calibration state.

The DAQ_ACTIVE calibration procedure requires the DCS, DAQ and Trigger systems to be all active. A block diagram of this procedure is displayed in fig.5.

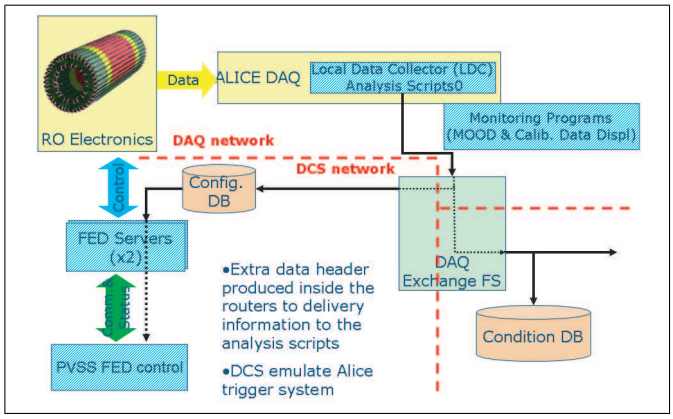

Figure 5: A block diagram of the DCS_ACTIVE calibration procedure

In this configuration the ECS issues the calibration start command to the different subsystem and waits for confirmation of detection configuration execution by the DCS. Depending on the required calibration mode either the Trigger system or the routers generate the readout sequences. The data are recorded in the DAQ Local Data Collectors (LDC). When the calibration procedure is completed, the ECS starts a set of LDC preprocessing scripts. These scripts analyze the raw data and generate ROOT files with the distributions of the hits detected on the pixel matrices (hit-maps). The files are forwarded automatically to a second level of processing that extracts the parameters needed for the reconfiguration of the detector. The processed and pre-processed data files are sent to the EFS that forwards them to the PDS, the CDB and the condition database used for track reconstruction. When this sequence of operations is completed the ECS closes the run and the system is placed in a standby condition.

The calibration procedure start and the SPD subsystems configuration request is performed by the ECS. The two calibration procedures have been implemented in the system test facility at CERN and are used for the SPD sector characterization. The DAQ_ACTIVE procedure allows the fast calibration of the full detector using the parallel data readout functionality.

VI. Safety Interlocks

Efficient cooling is vital for this very low mass detector. In the case of a cooling failure, the detector temperature would increase at a rate of 1 $^oC/s$. The detector temperature is therefore a critical parameter that must be monitored online and requires the immediate activation of a safety interlock if necessary. The maximum temperature allowed for the detector is 40 ^oC and the interlock threshold is set at 35^oC. Four levels of hardware interlocks and two levels of software interlocks are foreseen. In fig.6 is displayed the hardware interlock block diagram.

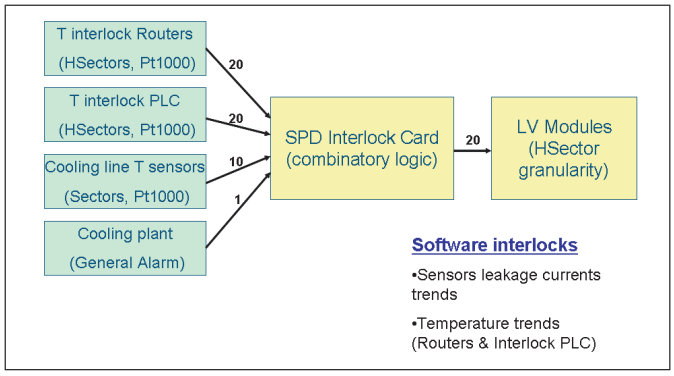

Figure 6: A block diagram of the SPD interlock interconnections

Each HS is equipped with 2 independent series of 5 temperature sensors (Pt1000) each. One of the series is readout by the Analog Pilot on the MCM and the data are encoded in the readout data stream. The Routers read the temperature values and assert the interlocks if needed. The other serie is hardwired out of the detector and read out in a dedicated PLC. The PLC scans the 120 chains in less than 1s. The hardwire interlock lines are processed in a card with SEU mitigation circuitry that provides direct safety interlock lines to the 20 LV power modules (one each half-sector). The temperature readouts are also sent online to the counting room via an ethernet link.
On the ten cooling lines have been placed temperature sensors read back via the temperature monitor PLC. The PLC and the Routers continuously monitor temperature trends and assert preventive interlocks if malfunctions are observed. The detector bias current roughly double each increase of temperature of 8^oC. The PVSS controlling the power supply system monitors constantly the sensor bias currents and in case of dangerous trends it switches off the corresponding HS.
A set of PVSS scripts run in the background to provide the proper overall power-down sequence in case of a part of the system is switched off by an hardware interlock.

VII. SPD INTEGRATION AND COMMISSIONING

The final test, integration and commissioning of the SPD is carried out in a dedicated area inside the Divisional Silicon Facility (DSF) at CERN. The area is equipped with the final cooling plant, power supply system, readout electronics and control system including temperature monitoring and safety interlocks. The DAQ system is a subset of the ALICE general one but with all the functionality. The trigger system is the final SPD partition.
The main objective is to test and commission the full detector with all the final systems and services before installation in the experimental area. Two FED servers are implemented and operational. Three working nodes are used to run the FSM, the DCS data analysis tools and the PLC for temperature monitoring and safety interlock.
The sectors are characterized in DSF and the configuration parameters retrieved using the tools described above are stored in the CDB in order to be used during ALICE startup.
At the time of writing 6 sectors are under test and the mechanical integration of the first half-barrel is starting.

VIII. SUMMARY

The SPD control system has been developed and it is used for the test, integration and commissioning of the sectors and the half-barrels, in conjunction with the final detector readout electronics and services in the dedicated area in the CERN DSF. The integration with the ALICE DCS and DAQ is nearing completion. The detector FSM prototype is operational and it has been integrated in the ECS.
The calibration procedures have been developed and implemented in the system test. Measured performance matches the challenging requirements as reported.

REFERENCES

[1] *Alice technical design report of the inner tracking system (its)*, CERN /LHCC / 99-12 ALICE TDR 4.

[2] *Specification of the digital control part of the analog pilot chip*, CERN (2002), http://akluge.home.cern.ch/akluge/work/alice/spd/.

[3] *Report of activities in the divisions*, vol. Volume II, European Organization for Nuclear Research (CERN), 2003.

[4] Cal I. A., *Readout of the silicon pixel detector in tha alice experiment*, 2003 ICFA Instrumentation School, Itacurua, Rio de Janeiro, Brazil, December 2003, Poster.

[5] Kluge A., *Specifications of the on detector pixel pilot system-ops*, CERN, June 2000, http://akluge.home.cern.ch/akluge/work/alice/spd/.

[6] Cali I.A. et al., *Test, qualification and electronics integraion of the alice silicon pixel detector modules*, World Scientific (2005), ICATTP05 proceedings.

[7] Chochula P. et al., *The alice silicon pixel detector*, Nucl. Instrum. Methods Phys. Res. **A** (2003), no. 715, 849c–52c.

[8] G. Aglieri Rinella et al., *The level 0 pixel trigger system for the alice experiment*, Proceedings of the 12th Workshop on Electronics for LHC and Future Experiments, LECC, September 2006, Valencia, Spain.

[9] M. Krivda et al., *Alice spd readout electronics*, Proceedings of the 12th Workshop on Electronics for LHC and Future Experiments, LECC, September 2006, Valencia, Spain.

[10] Wyllie K., *A pixel readout chip for tracking at alice and particle identification at lhcb*, Proceedings of the 5th Workshop on Electronics for LHC experiments, September 1999, Snowmass, CO, USA.

[11] Riedler P., *The alice silicon pixel detector*, Tech. report, CERN, 2003, Series of presentation.

[12] The Pixel Team, *Receiver card*, Tech. report, ALICE Note, CERN, January 2003, http://alice1.home.cern.ch.