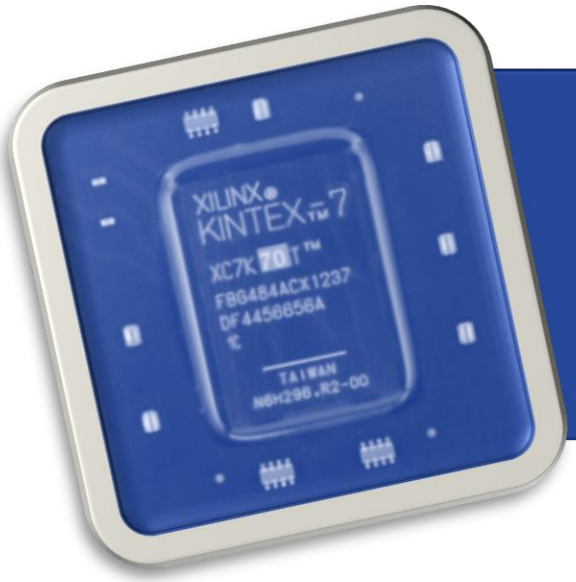

Experimental study on Soft Error Mitigation Core (SEM IP) efficiency

21.10.2016

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Workshop on Sensors and High Energy Physics (SHEP 2016)

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- FPGA configuration memory
  - Radiation-induced effects
- SEM IP Core
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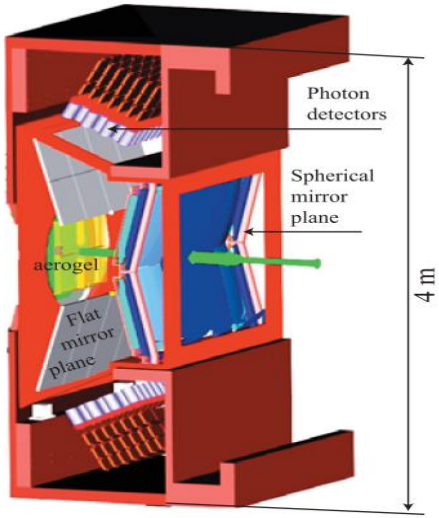
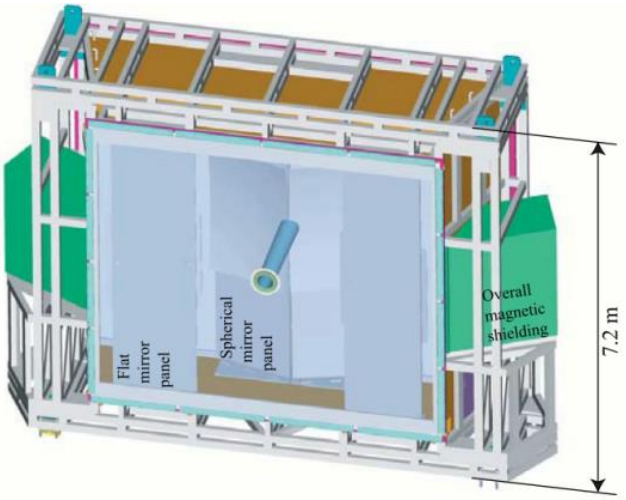
Introduction

- Study carried in the context of LHCb RICH sub-detectors Upgrade Program.
- Old photodetection system with Hybrid Photomultiplier-Detection tubes (HPD) replaced by new one based on Multi-anode Photomultiplier Tubes (MaPMT).
- New readout electronics is embedded in metallic structure making up the elementary cell, design to run at a trigger rate of 40 MHz**.**
- Harsh environment induced by beams head-on collisions and the resulting particles interacting with materials from LHCb detector.
- RICH radiation environment in case of 50 1/fb equivalent: 200 krad TID; 3 x 10^{12} for 1 MeV n_{eq} [cm^{-2}]; 1.2 x 10^{12} for hadrons >20 MeV [cm^{-2}].



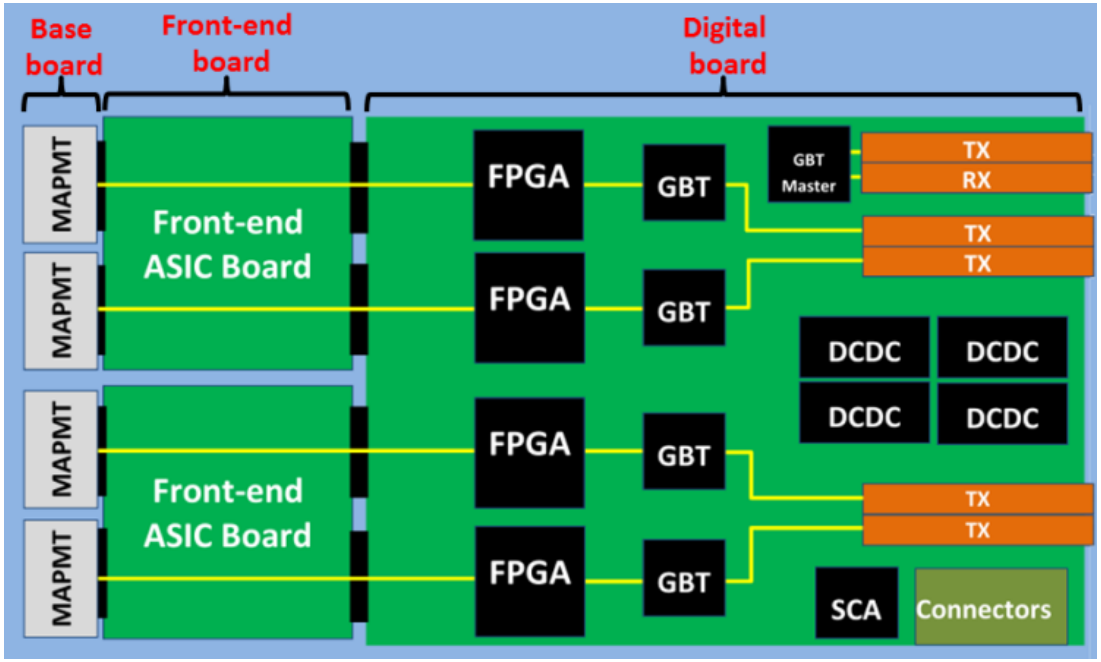
RICH1



RICH2

Introduction

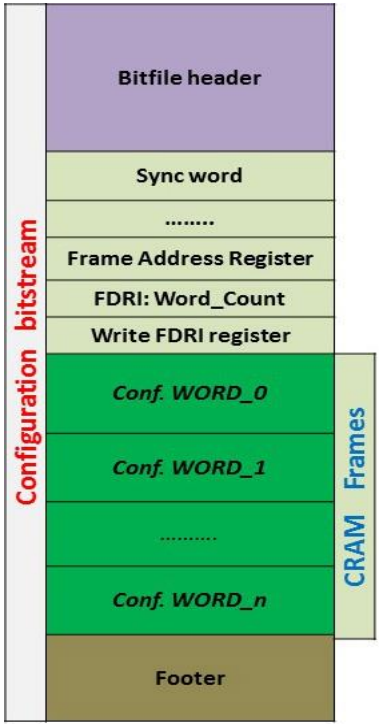
- Radiation-induce hardware & software failure in electronics device rise reliability issues.
- Changes in FPGA configuration memory modify the device functionality.
- Soft Errors Mitigation (SEM IP) Core from Xilinx.
- *Device Under Test: XC7K70T-FBG484C6 KINTEX-7*



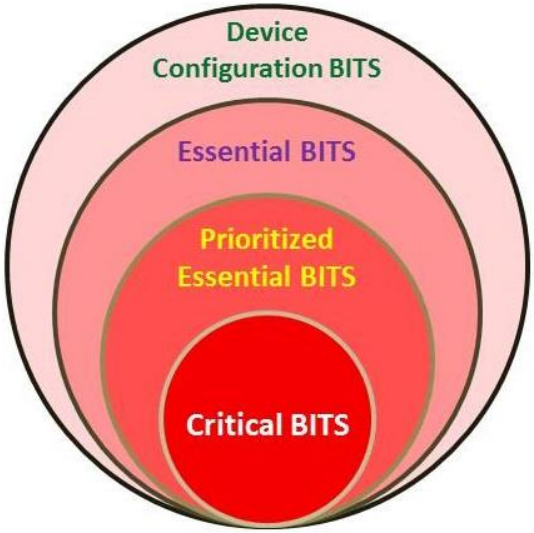
Elementary cell

FPGA configuration memory

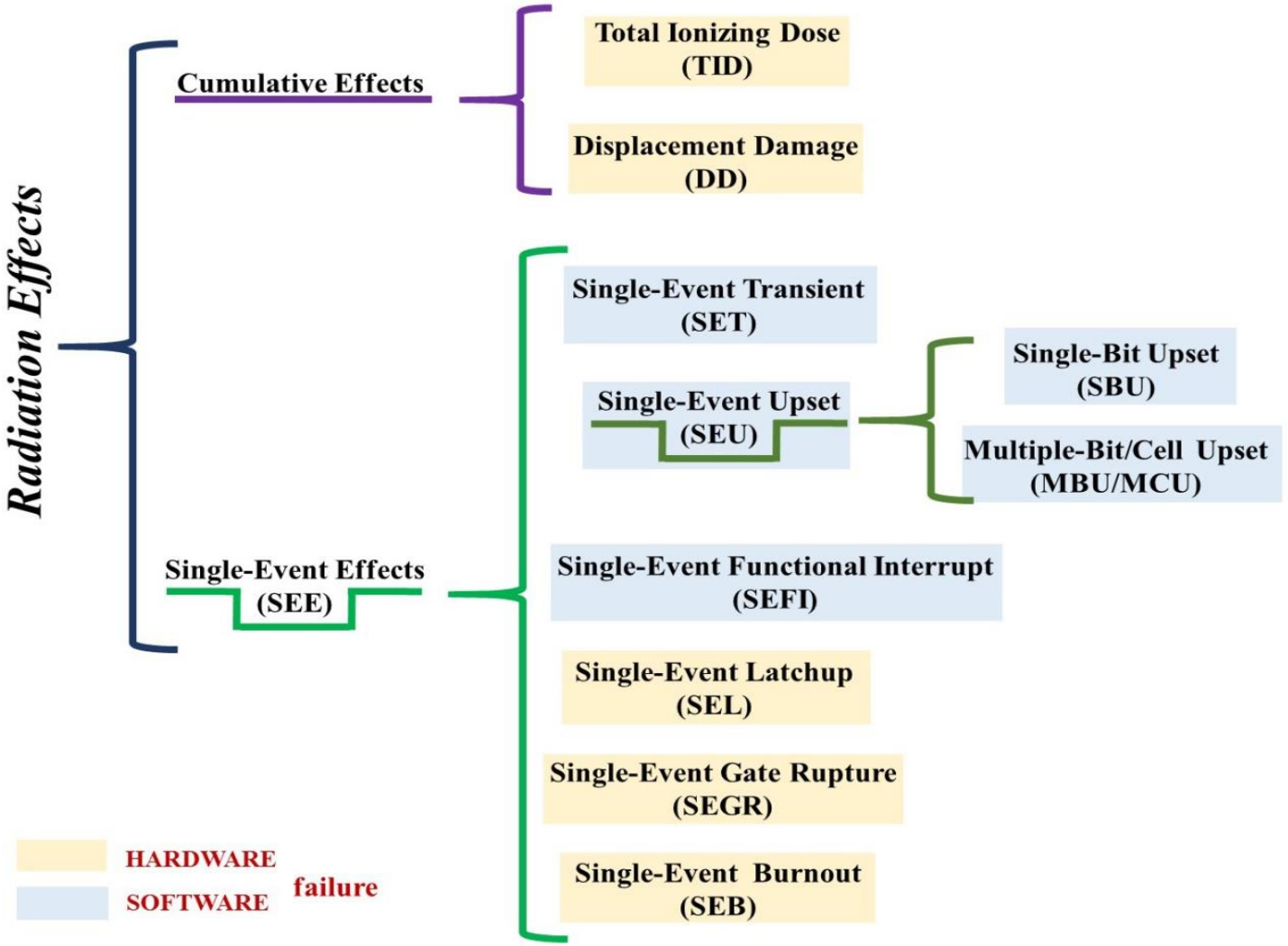
- Xilinx 7 series SRAM based FPGA built-in memory types: configuration memory (***CRAM***), block memory (BRAM); distributed memory; flip-flops.
- The design is loaded into device CRAM which is: arranged in frames, protected by error correction code (ECC) and cyclic redundancy check (CRC).
- Every frame consists on 101 configuration words of 32 bits each.
- A frame is the smallest addressable segments of FPGA CRAM



- FPGA design is compiled into ***bitstream*** with fixed length made up of configuration commands and configuration bits stored in CRAM.
- Design circuitry changes if one or more essential bits are flipped.
- XILINX essential bits technology embeds an algorithm for identifying the configuration bits essential to FPGA design.
- User can do a priority-filter of the design essential bits.



FPGA configuration memory (radiation-induced effects)



SEM IP Core

- SEM IP Core it is a free and pre-verified XILINX solution for automatic detection, correction and classification of the bits upsets in FPGA CRAM.
- Configurable to run in three modes Repair, Enhanced-Repair and Replaced.
- When SEM IP is set to idle, we "inject" errors by SEU simulated events into CRAM memory.
- FPGA has built-in memory bits as internal device control registers as well as state elements which are reserved and not addressable by SEM IP.
- Single-Event Functional Interrupt (SEFI) can not be mitigated by SEM IP Core.

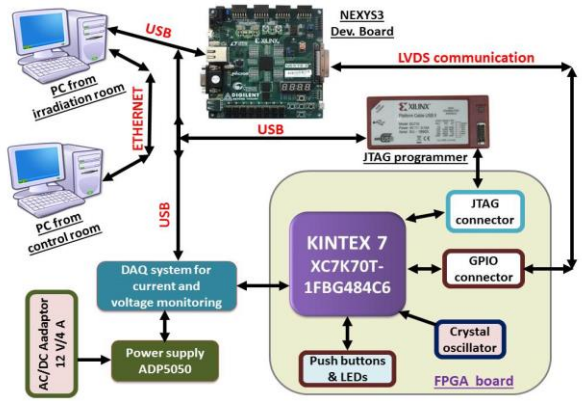
SEM IP Core in repair mode performance specification for the XC7K70T FPGA:

- start-up latency 110 ms, error detection latency 5.9 ms, error correction latency around 1 ms for 1 bit correctable in a memory frame.
- FPGA resources: 41000 x LUTs, 82000 x FFs, 270 x BRAM18 / 135 x BRAM36
- SEM IP resource utilization: 849 x LUTs, 682 x FFs, 3 x BRAM18 and 3 x BRAM36.

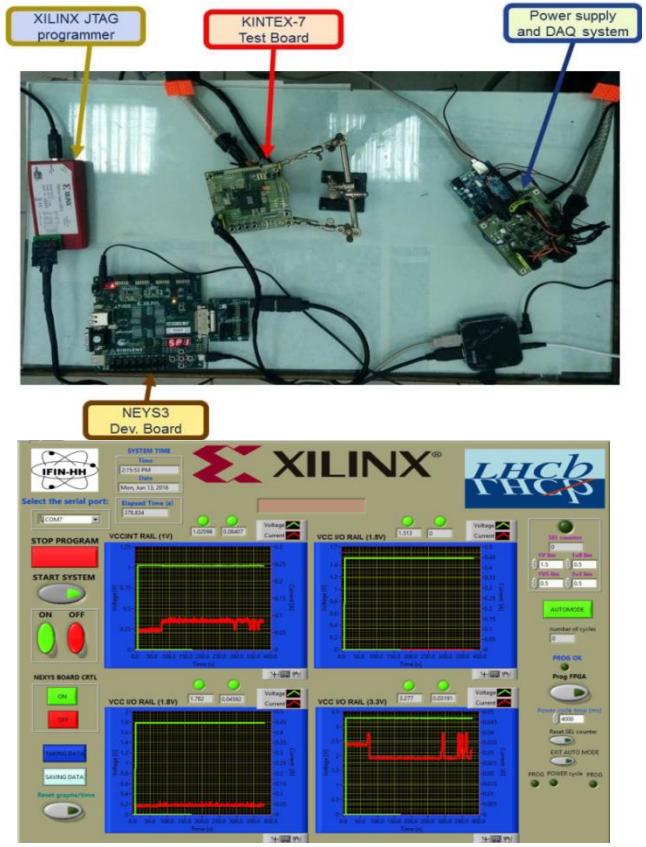
XILINX SEM IP core:

- www.xilinx.com/products/intellectual-property/sem.html#documentation
- www.xilinx.com/products/intellectual-property/sem.html#overview

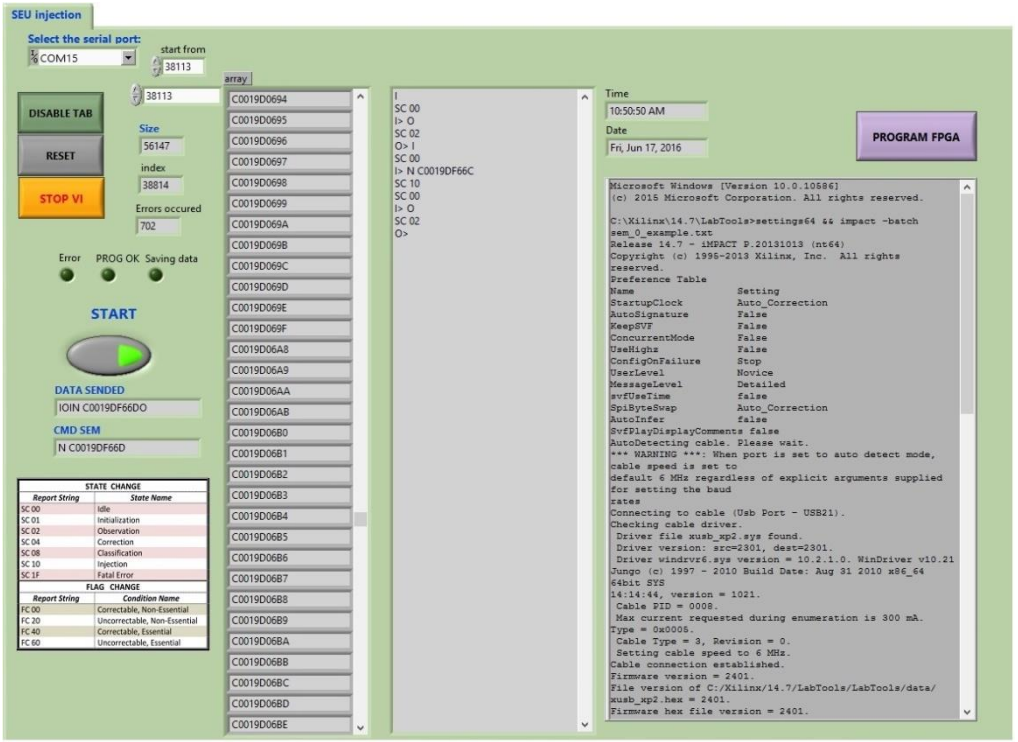
SEM IP Core (test bench)



Test bench for KINTEX-7 FPGA

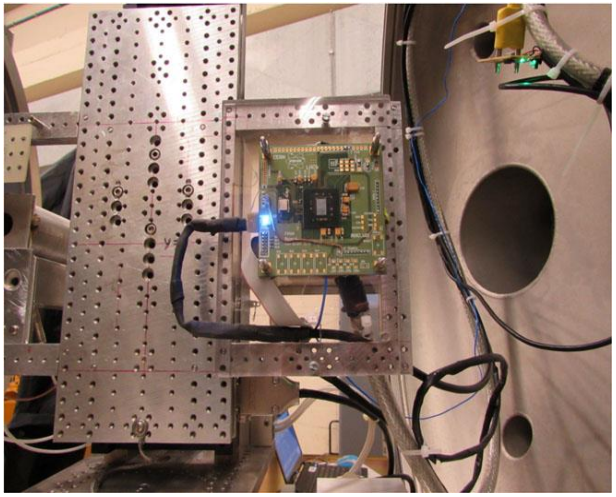


- Complete test bench developed for DUT radiation hardness qualification.
- Extensive study on SEM IP Core mitigation efficiency.
- Python script developed to decode and determine the address of each essential bit of the FPGA design.

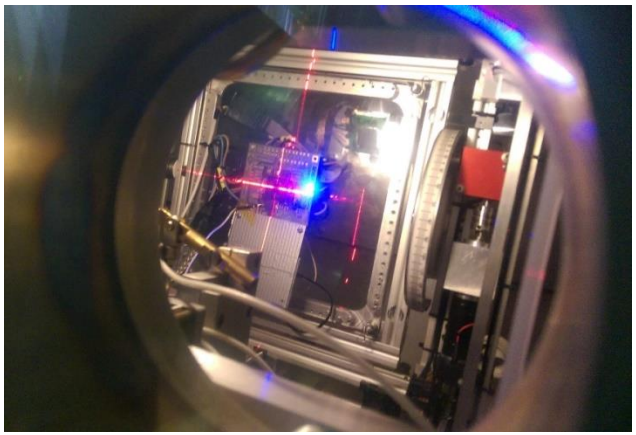


GUI developed for SEM IP control and CRAM errors injection

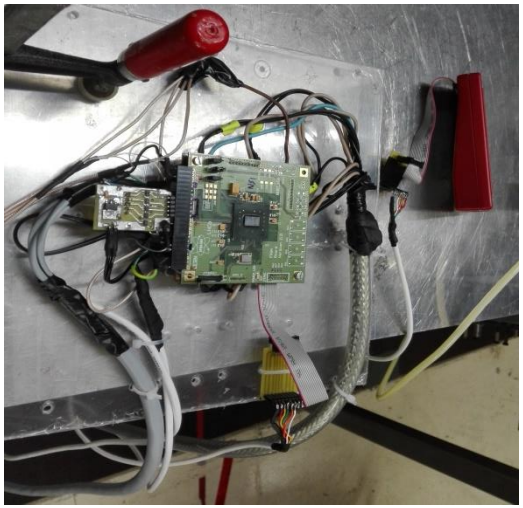
SEM IP Core (irradiation tests)

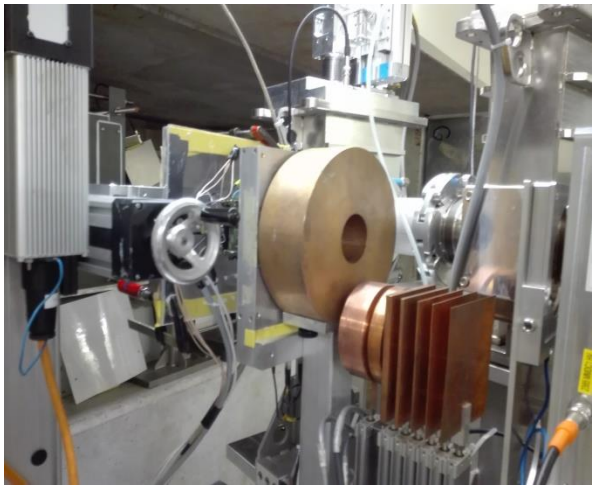


SIRAD facility from Legnaro National Laboratories, in Italy; (July 2015)



Heavy Ion Facility at Cyclotron Resource Center at Louvain-la-Neuve, Universite Catholique de Louvain Belgium (UCL), (June 2016)





PIF facility from Paul Scherrer Institute (PSI), in Switzerland; (August 2016)

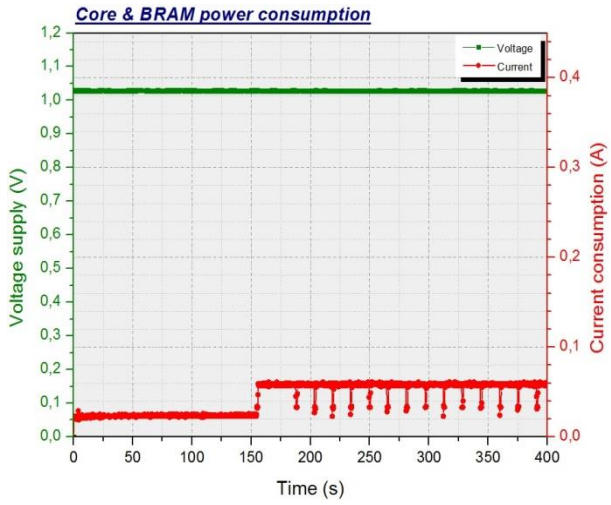
Results

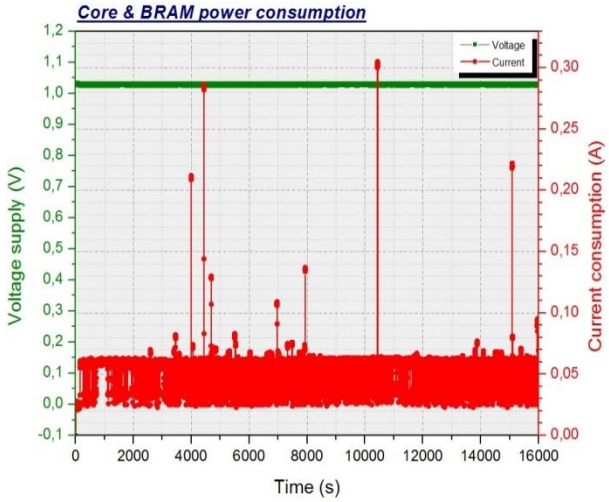
- Offline tests with only SEM IP core instantiated in repair mode.
- Errors injected one at a time, test bench has run 2 weeks continuously.
- Test bench for irradiation: FPGA power supplied over 5m cable and programmed through JTAG using 3m of cable.

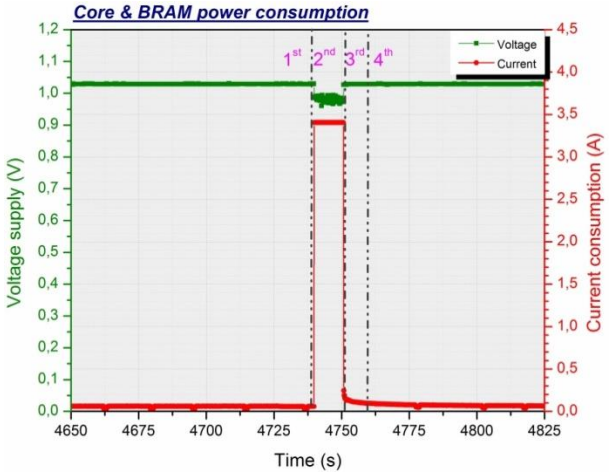
SEM IP Core vs CRAM occupancy

Bitstream length	24090592
Total config. bits	18884576
Essential bits (1)	56146

- TEST REPORT: 11 bits caused JTAG crash, 26 bits led to FPGA power consumption increasing, only 50% of SEM IP essential bits were correctable.
- If bit correction failed then blind scrubbing procedure was launched.

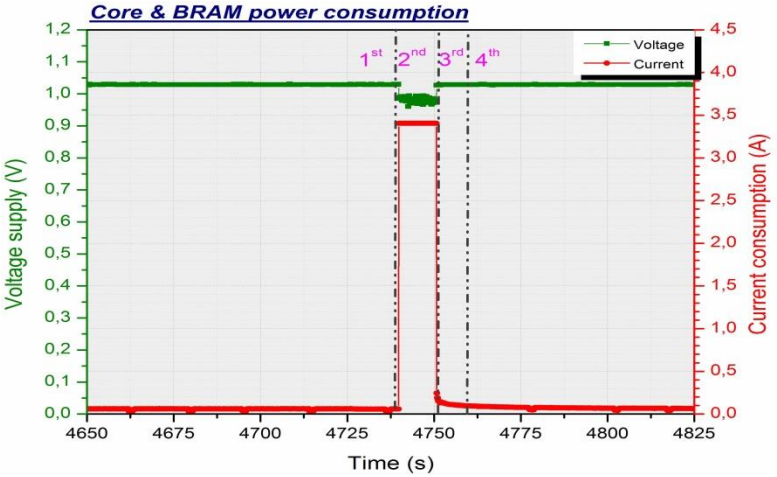




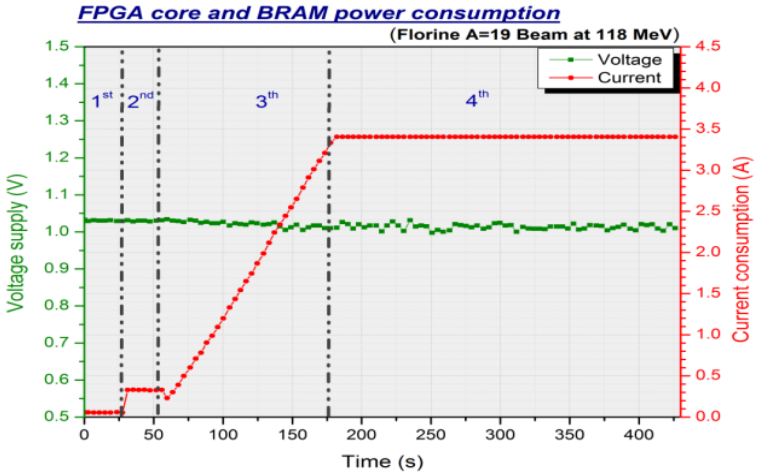


Offline tests with SEM IP Core

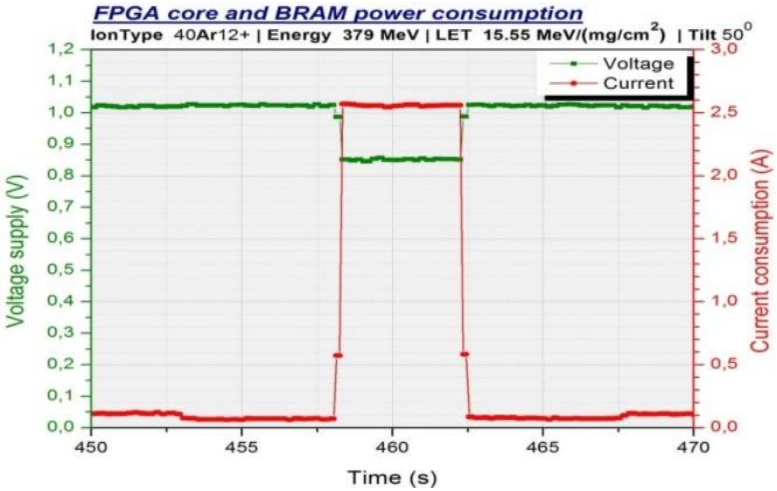
Results



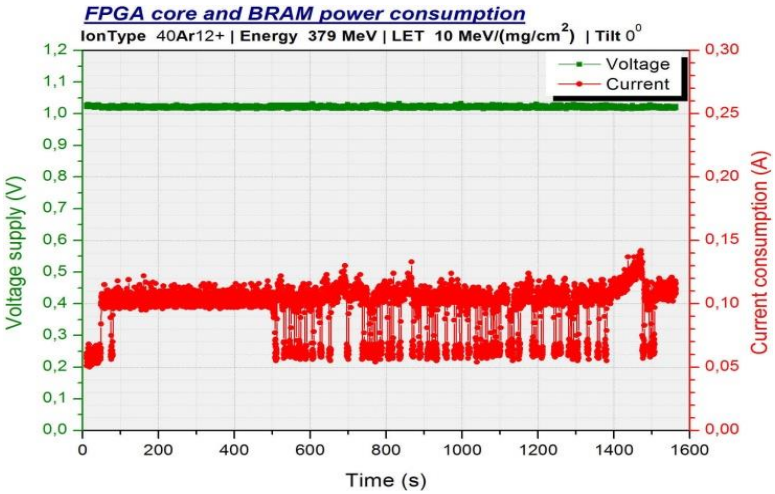
Offline tests with SEM IP Core



FPGA irradiation without SEM IP (Legnaro)



FPGA irradiation with SEM IP instantiated (Louvain)



FPGA radiation hardness tests with SEM IP instantiated (Louvain)

Conclusions

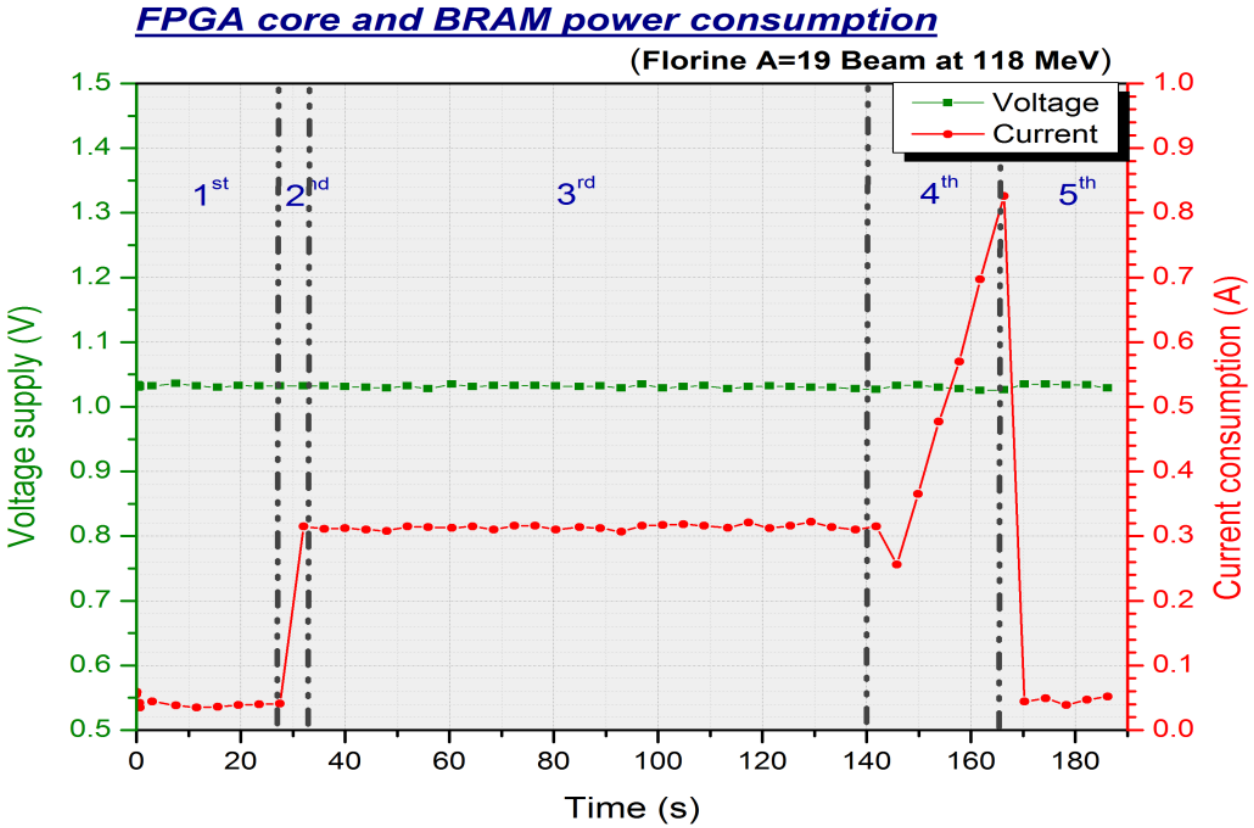
- SEM IP Core was proven a useful solution to investigate the reliability and behavior of an FPGA design when CRAM bits are changed.
- Mismatch in FPGA logic resources, because of a error in CRAM, can rise up the device power consumption.
- Once instantiated into FPGA design, the SEM IP core feedback helps to distinguish among various effects induced by radiation.
- Irradiation tests performed on our DUT rely on SEM IP mitigation and scrubbing capability.
- In the rad-hard tests different particle species has been used such as proton and ion cocktail.
- Result highlighted that SEM IP mitigation efficiency is overcome when the beam flux is higher than 10^3 ions/ cm^2/s and the efficiency become even lower if ions have high stopping power (LET).
- For accelerated irradiation tests, where the beam has high flux, it is recommended to use an external scrubbing solution.

Backup slides

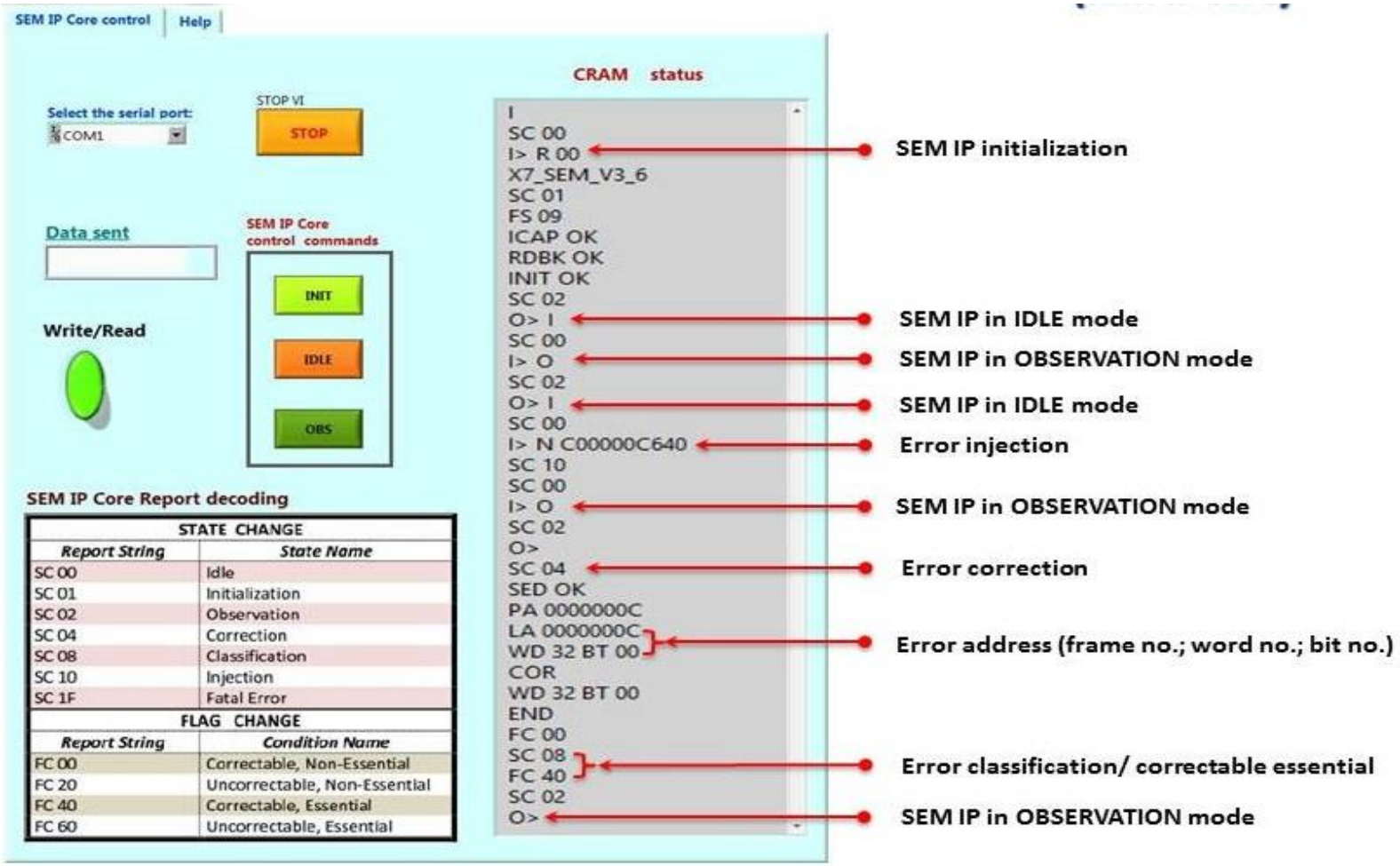
Irradiation facilities

- ***Heavy ions***:
  - $^{16}\mathbf{O}$ **at 126 MeV (LET=2.85** $\mathbf{MeV} * cm^2/\mathrm{mg}$**) and** $^{19}\mathbf{F}$ **at 118 MeV (LET=3.67** $\mathbf{MeV} * cm^2/\mathrm{mg}$**) at SIRAD facility served by a 14 MV TANDEM accelerator from Legnaro National Laboratories, in Italy; (July 2015)**
  - **Heavy Ion Facility at Cyclotron Resource Center at Louvain-la-Neuve, Universite Catholique de Louvain Belgium (UCL), the following ions were used (June 2016):**
    - $^{13}\mathbf{C}$ **at 131 MeV (LET=1.3** $\mathbf{MeV} * cm^2/\mathrm{mg}$**);**
    - $^{22}\mathbf{Ne}$ **at 238 MeV (LET=3.3** $\mathbf{MeV} * cm^2/\mathrm{mg}$**);**
    - $^{40}\mathbf{Ar}$ **at 379 MeV (LET=10** $\mathbf{MeV} * cm^2/\mathrm{mg}$**);**
    - $^{58}\mathbf{Ni}$ **at 582 MeV (LET=20.4** $\mathbf{MeV} * cm^2/\mathrm{mg}$**);**
    - $^{83}\mathbf{Kr}$ **at 769 MeV (LET=32.4** $\mathbf{MeV} * cm^2/\mathrm{mg}$**);**
- ***Protons***:
  - **Paul Scherrer Institute (at PIF) using 200 MeV protons (LET of 0.0036** $\mathbf{MeV} * cm^2/\mathrm{mg}$**); (August 2016)**

SEFI


FPGA core and BRAM power consumption
(Florine A=19 Beam at 118 MeV)
Voltage
Current
1st
2nd
3rd
4th
5th
Voltage supply (V)
Current consumption (A)
Time (s)
1.5
1.4
1.3
1.2
1.1
1.0
0.9
0.8
0.7
0.6
0.5
1.0
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0.0
0
20
40
60
80
100
120
140
160
180

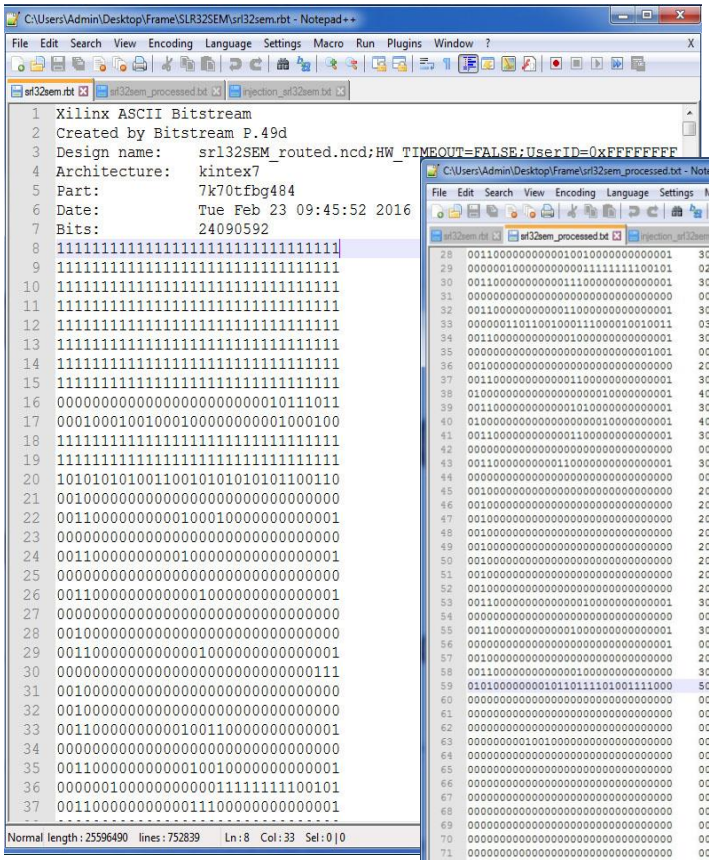
GUI



SEM IP Core Report decoding

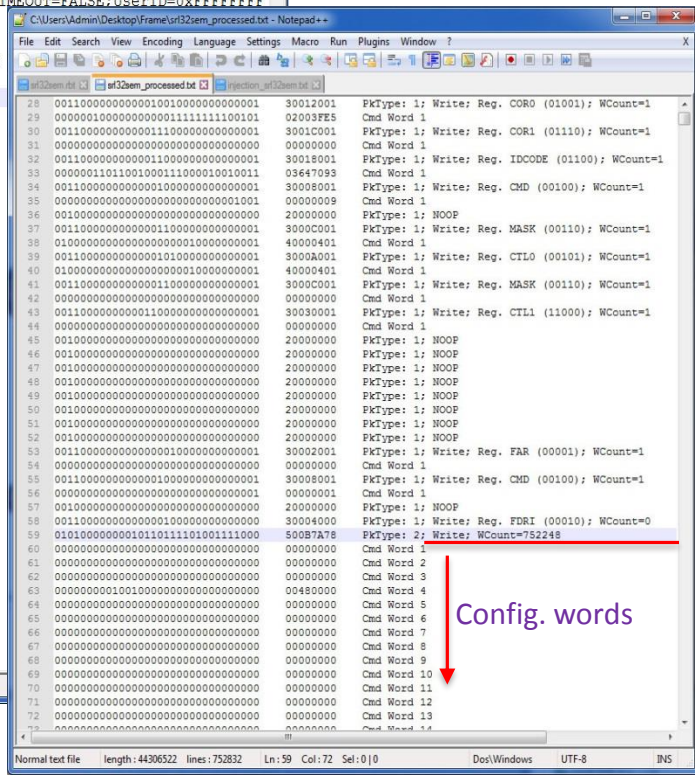
STATE CHANGE	
Report String	*State Name*
SC 00	Idle
SC 01	Initialization
SC 02	Observation
SC 04	Correction
SC 08	Classification
SC 10	Injection
SC 1F	Fatal Error
FLAG CHANGE	
Report String	*Condition Name*
FC 00	Correctable, Non-Essential
FC 20	Uncorrectable, Non-Essential
FC 40	Correctable, Essential
FC 60	Uncorrectable, Essential

file_1



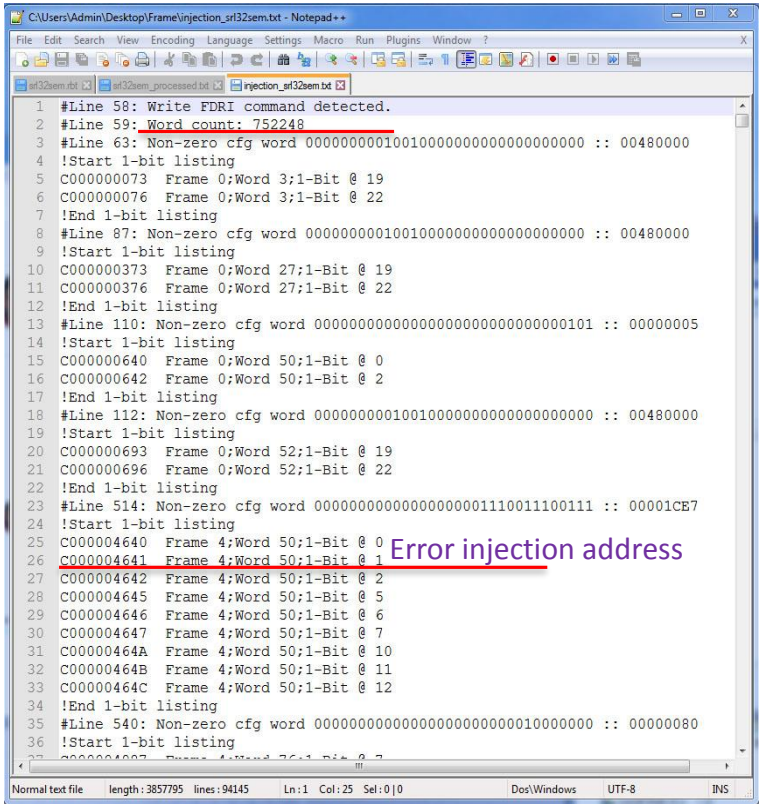
FPGA configuration file with the bitstream in ASCII

file_2



FPGA configuration file decoded and prepared for frames extraction

file_3



Essential bits address calculation

A script was developed in Python to automatically decode and determine the address of each essential bit.