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Experimental study on Soft Error Mitigation Core (SEM IP) efficiency

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Introduction

- Study carried in the context of LHCb RICH sub-detectors Upgrade Program.
- Old photodetection system with Hybrid Photomultiplier-Detection tubes (HPD) replaced by new one based on Multi-anode Photomultiplier Tubes (MaPMT).
- New readout electronics is embedded in metallic structure making up the elementary cell, design to run at a trigger rate of 40 MHz.
- Harsh environment induced by beams head-on collisions and the resulting particles interacting with materials from LHCb detector.
- RICH radiation environment in case of 50 1/fb equivalent: 200 krad TID; 3 x 10^{12} for 1 MeV n_{eq} [cm⁻²]; 1.2 x 10^{12} for hadrons >20 MeV [cm⁻²].





RICH2



Introduction

- Radiation-induce hardware & software failure in electronics device rise reliability issues.
- Changes in FPGA configuration memory modify the device functionality.
- Soft Errors Mitigation (SEM IP) Core from Xilinx.
- Device Under Test: XC7K70T-FBG484C6 KINTEX-7



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FPGA configuration memory

- Xilinx 7 series SRAM based FPGA built-in memory types: configuration memory (*CRAM*), block memory (BRAM); distributed memory; flip-flops.
- The design is loaded into device CRAM which is: arranged in frames, protected by error correction code (ECC) and cyclic redundancy check (CRC).
- Every frame consists on 101 configuration words of 32 bits each.
- A frame is the smallest addressable segments of FPGA CRAM
- FPGA design is compiled into *bitstream* with fixed length made up of configuration commands and configuration bits stored in CRAM.
- Design circuitry changes if one or more essential bits are flipped.
- XILINX essential bits technology embeds an algorithm for identifying the configuration bits essential to FPGA design.
- User can do a priority-filter of the design essential bits.









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SEM IP Core

- SEM IP Core it is a free and pre-verified XILINX solution for automatic detection, correction and classification of the bits upsets in FPGA CRAM.
- Configurable to run in three modes Repair, Enhanced-Repair and Replaced.
- When SEM IP is set to idle, we "inject" errors by SEU simulated events into CRAM memory.
- FPGA has built-in memory bits as internal device control registers as well as state elements which are reserved and not addressable by SEM IP.
- Single-Event Functional Interrupt (SEFI) can not be mitigated by SEM IP Core.

SEM IP Core in repair mode performance specification for the XC7K70T FPGA:

- start-up latency 110 ms, error detection latency 5.9 ms, error correction latency around 1 ms for 1 bit correctable in a memory frame.
- FPGA resources: 41000 x LUTs, 82000 x FFs, 270 x BRAM18 / 135 x BRAM36
- SEM IP resource utilization: 849 x LUTs, 682 x FFs, 3 x BRAM18 and 3 x BRAM36.

XILINX SEM IP core:

- www.xilinx.com/products/intellectual-property/sem.html#documentation
- www.xilinx.com/products/intellectual-property/sem.html#overview







SEM IP Core (test bench)

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- Complete test bench developed for DUT radiation hardness qualification.
- Extensive study on SEM IP Core mitigation efficiency.
- Python script developed to decode and determine the address of each essential bit of the FPGA design.

SEU injection			
Select the serial port: COM15	array		
DISABLE TAB	C0019D0694 ^	I SC 00 I> O SC 02	Time 10:50:50 AM Date PROGRAM FPGA
RESET index 38814 STOP VI	C0019D0697 C0019D0698 C0019D0699	SC 00 I> N C0019DF66C SC 10 SC 00	Microsoft Windows [Version 10.0.10586] (c) 2015 Microsoft Corporation. All rights reserved.
Error PROG OK Saving data	C0019D069A C0019D069B C0019D069C	SC 02 O>	C:\Xilinx\14.7\LabTools>settings64 65 impact -batch sem_0_example.txt Aslass 14.7 - xHRAT P.20131013 (nt64) Copyright (s) 1995-2013 Xilinx, Inc. All rights reserved
START	C0019D069D C0019D069E C0019D069F		preference fable Name StartupClock Auto_Correction AutoSignature False ZeegSVF False ConcurrentMode False
DATA SENDED	C0019D06A8 C0019D06A9 C0019D06AA		UseHighz False ConfigOnFalure Stop UserLevel Novice MessageLevel Detailed artInctime false
IOIN C0019DF66DO CMD SEM N C0019DF66D	C0019D06AB C0019D06B0 C0019D06B1		SpiByteSwap Auto_Correction AutoInfer false SvfPlayDiplayComment false AutoDetecting cable. Plasse wait.
STATE CHANGE Report String State Name SC 00 Idle	C0019D06B2 C0019D06B3 C0019D06B4		cable speed is set to default 6 HHz regardless of explicit arguments supplied for setting the baud rates Connecting to cable (USb Port - USB21).
SC 01 Initialization SC 02 Observation SC 04 Correction SC 05 Classification SC 10 Injection SC 12 F Fatal Error	C0019D0685 C0019D0686 C0019D0687		Checking cable driver. Driver file aush_prof.sys found. Driver version: src=2301, dest=2301. Driver windsvz6.sys version = 10.2.1.0. WinDriver v10.21 Jungo (c. 1987 - 2010 Build Date: Aug 31 2010 x86_64
FLAG CHANGE Report String Condition Name FC 00 Correctable, Non-Essential FC 20 Uncorrectable, Non-Essential FC 40 Correctable, Essential FC 60 Uncorrectable, Essential	C0019D0688 C0019D0689 C0019D0689		<pre>64bit SYS 14:14:44, version = 1021. Cable PID = 0000. Max current requested during enumeration is 300 mA. Type = 0x0005. Cable Type = 0 Servision = 0</pre>
1 e ve j e sud i CCON, Laponon	C0019D06BB C0019D06BC C0019D06BD		Setting Coble speed to f ME: Cable connection established. Firmware version = 2401. File version of C:/Klinky14.7/LabTools/LabTools/dats/ xubb_xp2.hes = 2401. Firmware her file version = 2401.
	C0019D06BE		·

GUI developed for SEM IP control and CRAM errors injection



SEM IP Core (irradiation tests)



SIRAD facility from Legnaro National Laboratories, in Italy; (July 2015)





Heavy Ion Facility at Cyclotron Resource Center at Louvain-la-Neuve, Universite Catholique de Louvain Belgium (UCL), (June 2016)



PIF facility from Paul Scherrer Institute (PSI), in Switzerland; (August 2016)





Results

- Offline tests with only SEM IP core instantiated in repair mode.
- Errors injected one at a time, test bench has run 2 weeks continuously.
- Test bench for irradiation: FPGA power supplied over 5m cable and programmed through JTAG using 3m of cable.
- TEST REPORT: 11 bits caused JTAG crash, 26 bits led to FPGA power consumption increasing, only 50% of SEM IP essential bits were correctable.
- If bit correction failed then blind scrubbing procedure was launched.



SEM IP Core vs CRAM occupancy

Bitstream length	24090592
Total config. bits	18884576
Essential bits (1)	56146







FPGA irradiation without SEM IP (Legnaro)





FPGA radiation hardness tests with SEM IP instantiated (Louvain)

Results

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Conclusions

- SEM IP Core was proven a useful solution to investigate the reliability and behavior of an FPGA design when CRAM bits are changed.
- Mismatch in FPGA logic resources, because of a error in CRAM, can rise up the device power consumption.
- Once instantiated into FPGA design, the SEM IP core feedback helps to distinguish among various effects induced by radiation.
- Irradiation tests performed on our DUT rely on SEM IP mitigation and scrubbing capability.
- In the rad-hard tests different particle species has been used such as proton and ion cocktail.
- Result highlighted that SEM IP mitigation efficiency is overcome when the beam flux is higher than 10³ ions/ cm²/s and the efficiency become even lower if ions have high stopping power (LET).
- For accelerated irradiation tests, where the beam has high flux, it is recommended to use an external scrubbing solution.







Irradiation facilities

- Heavy ions:
 - ¹⁶O at 126 MeV (LET=2.85 MeV * cm²/mg) and ¹⁹F at 118 MeV (LET=3.67 MeV * cm²/mg) at SIRAD facility served by a 14 MV TANDEM accelerator from Legnaro National Laboratories, in Italy; (July 2015)
 - □ Heavy Ion Facility at Cyclotron Resource Center at Louvain-la-Neuve, Universite Catholique de Louvain Belgium (UCL), the following ions were used (June 2016):
 - $\circ~^{13}\text{C}$ at 131 MeV (LET=1.3 MeV $*~cm^2/\text{mg}$);
 - ²²Ne at 238 MeV (LET=3.3 MeV $* cm^2/mg$);
 - 40 Ar at 379 MeV (LET=10 MeV * cm^2 /mg);
 - $^{\circ}$ ⁵⁸Ni at 582 MeV (LET=20.4 MeV * cm^2 /mg);
 - \circ ⁸³Kr at 769 MeV (LET=32.4 MeV * cm^2 /mg);
- Protons:
 - □ Paul Scherrer Institute (at PIF) using 200 MeV protons (LET of 0.0036 MeV $* cm^2/mg$); (August 2016)









GUI



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	file_1		
Colleges Admin Decision Frame) SI P22554 (cd22cam sht Netword or			filo 2
Cosers (domini) Desktop (Hame (Sch Sz Sz Mish Sz Semirbit - Hotepad++			lile_5
File Edit Search View Encoding Language Settings Macro Kun Plugi			C:\Users\Admin\Desktop\Frame\injection srl32sem.txt - Notepad++
			File Edit Search View Encoding Language Settings Macro Run Plugins Window ?
🔄 srl32sem.ht 🔀 📔 srl32sem_processed bt 🔀 🔚 injection_srl32sem.bt 🔀			
1 Xilinx ASCII Bitstream	<u>^</u>	filo 2	E tel 32sem thi 13 E tel 32sem processed thi 13 E injection st 32sem bt 13
2 Created by Bitstream P.49d	INFORM DATOR VICE ATD AND DDDDDDD	IIIe_2	1 #Line 58: Write EDRI command detected
3 Design name: Sri32SEM_routed.ncd;HW_T	IMEOUT=FALSE; USETID=UXFFFFFFFF		2 #Line 59: Word count: 752248
5 Part: 7k70tfbc/04	C: Users (Admin) Desktop (Frame (Sriszsen_processed.ox) - Notepad++		3 #Line 63: Non-zero cfg word 000000001001000000000000000000 :: 00480000
6 Date: The Feb 23 09:45:52 2016	File Edit Search View Encoding Language Settings Macro Ri		4 !Start 1-bit listing
7 Bits: 24090592			5 C00000073 Frame 0;Word 3;1-Bit @ 19
8 1111111111111111111111111111111111111	arliäzsem ibit 🔄 📄 arliäzsem_processed bt 🖾 📑 injection_arliäzsem bit 🖾		6 C00000076 Frame 0;Word 3;1-Bit @ 22
9 1111111111111111111111111111111111111	28 0011000000000000000000000000000000000	PRType: 1; Write; Reg. CORO (01001); WCount=1	7 !End 1-bit listing
10 111111111111111111111111111111111111	30 0011000000000111000000000000 3001C001	PkType: 1; Write; Reg. COR1 (01110); WCount=1	s #Line 8/: Non-zero cig Word 000000000000000000000000000000000000
11 111111111111111111111111111111111111	31 000000000000000000000000000000000000	Cmd Word 1 PkTvpe: 1: Write: Reg. IDCODE (01100): WCount=1	10 COMMON273 Frame 0.Word 27:1_Bit 0 19
12 111111111111111111111111111111111111	33 0000001101100100011100001001001 03647093	Cmd Word 1	11 C000000376 Frame 0:Word 27:1-Bit @ 22
13 111111111111111111111111111111111111	34 0011000000000000000000000000000000000	PkType: 1; Write; Reg. CMD (00100); WCount=1 Cmd Word 1	12 !End 1-bit listing
14 111111111111111111111111111111111111	36 0010000000000000000000000000000000000	PkType: 1; NOOP	13 #Line 110: Non-zero cfg word 000000000000000000000000000101 :: 00000005
15 111111111111111111111111111111111111	37 00110000000000011000000000000 30000001 38 0100000000000000000000000000000000000	PkType: 1; Write; Reg. MASK (00110); WCount=1 Cmd Word 1	14 !Start 1-bit listing
16 000000000000000000000000000000000000	39 00110000000000001010000000000 3000A001	PkType: 1; Write; Reg. CTL0 (00101); WCount=1	15 C000000640 Frame 0;Word 50;1-Bit @ 0
17 000100010010000000000000000000000	40 010000000000000000000000000000000000	Cmd Word 1	16 C000000642 Frame 0;Word 50;1-Bit @ 2
18 111111111111111111111111111111111111	42 000000000000000000000000000000000000	Cmd Word 1	17 End 1-bit listing
	43 00110000000001100000000000000 30030001	PkType: 1; Write; Reg. CTL1 (11000); WCount=1	10 FLHE 112: NON-ZETO CIG WORD 000000000000000000000000000000000000
	45 0010000000000000000000000000000000000	PkType: 1; NOOP	20 COLONOR693 Frame 0:Word 52:1-Bit @ 19
21 001000000000000000000000000000000000	46 0010000000000000000000000000000000000	PkType: 1; NOOP	21 C000000696 Frame 0;Word 52;1-Bit @ 22
22 001100000000000000000000000000000000	47 0010000000000000000000000000000000000	PkType: 1; NOOP PkType: 1; NOOP	22 !End 1-bit listing
24 0011000000000000000000000000000000000	49 0010000000000000000000000000000000000	PkType: 1; NOOP	23 #Line 514: Non-zero cfg word 000000000000000001110011100111 :: 00001CE7
25 000000000000000000000000000000000000	50 001000000000000000000000000000000000	PkType: 1; NOOP PkType: 1; NOOP	24 !Start 1-bit listing
26 0011000000000000000000000000000000000	52 0010000000000000000000000000000000000	PkType: 1; NOOP	25 C000004640 Frame 4; Word 50; 1-Bit @ 0 Frror injection address
27 000000000000000000000000000000000000	53 0011000000000000000000000000000000000	PkType: 1; Write; Reg. FAR (00001); WCount=1	26 <u>c000004641</u> Frame 4; Word 50;1-Bit @ 1
28 0010000000000000000000000000000000000	55 001100000000000000000000000000000000	PkType: 1; Write; Reg. CMD (00100); WCount=1	27 C000004642 Frame 4;Word 50;1-Bit @ 2
29 0011000000000000000000000000000000000	56 000000000000000000000000000000000000	Cmd Word 1	28 C000004645 Frame 4; Word 50; 1-Bit @ 5
30 000000000000000000000000000000000000	58 00110000000000010000000000000 30004000	PkType: 1; Write; Reg. FDRI (00010); WCount=0	30 C000004647 Frame 4:Word 50:1-Bit @ 7
31 001000000000000000000000000000000000	59 010100000001011011101001111000 500B7A78	PkType: 2; Write; WCount=752248	31 C00000464A Frame 4; Word 50; 1-Bit @ 10
32 0010000000000000000000000000000000000	61 000000000000000000000000000000000000	Cmd Word 1 Cmd Word 2	32 C00000464B Frame 4; Word 50; 1-Bit @ 11
33 001100000000000100110000000000000	62 000000000000000000000000000000000000	Cmd Word 3	33 C00000464C Frame 4;Word 50;1-Bit @ 12
34 000000000000000000000000000000000000	63 UUUU0000010010000000000000000000000000	Cmd Word 4 Cmd Word 5	34 !End 1-bit listing
35 0011000000000000000000000000000000000	65 000000000000000000000000000000000000	Cmd Word 6 CONTIG. WORDS	35 #Line 540: Non-zero cfg word 000000000000000000000000000000000000
36 0000001000000000011111111100101	66 00000000000000000000000000000000000	Cmd Word 7	36 !Start 1-bit listing
37 001100000000001110000000000000	68 000000000000000000000000000000000000	Cmd Word 9	<
Normal length: 25596490 lines: 752839 Ln:8 Col:33 Sel:010		Cmd Word 10	Normal text file length: 3857795 lines: 94145 Ln:1 Col: 25 Sel: 0 Dos\Windows UTF-8 INS
arro corros daro v	71 000000000000000000000000000000000000	Cmd Word 12	
FDCA configuration	72 000000000000000000000000000000000000	Cmd Word 13	

FPGA configuration file with the bitstream in ASCII

FPGA configuration file decoded and prepared for frames extraction

length: 44306522 lines: 752832 Ln: 59 Col: 72 Sel: 0 | 0

mal text file

Essential bits address calculation

A script was developed in Python to automatically decode and python^{*} determine the address of each essential bit.

Workshop on Sensors and High Energy Physics (SHEP 2016)

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