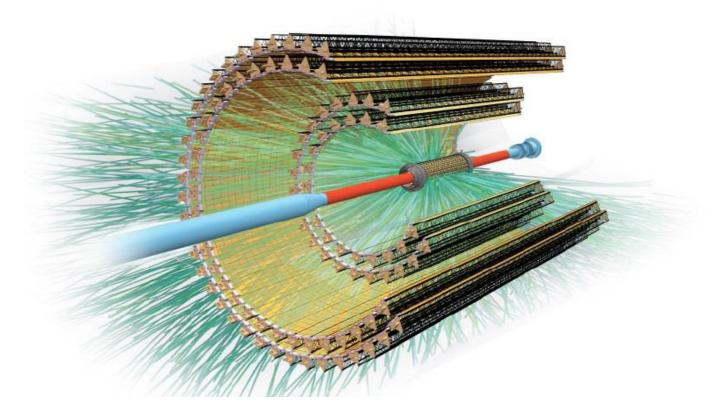


ALICE ITS Upgrade Status Report

In-Kwon YOO - Pusan National Univ. for ALICE collaboration









Outline

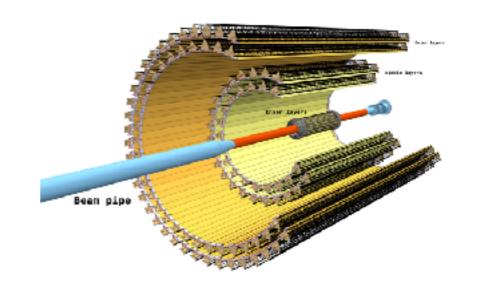


- 1. ALICE ITS Upgrade Motivation
- 2. Pixel Chip Performance, Status and Plan
- 3. Module and Stave Status and Plans
- 4. Barrel Mechanics Milestones
- 5. Readout Electronics
- 6. Overall ITS Construction and Integration Schedule

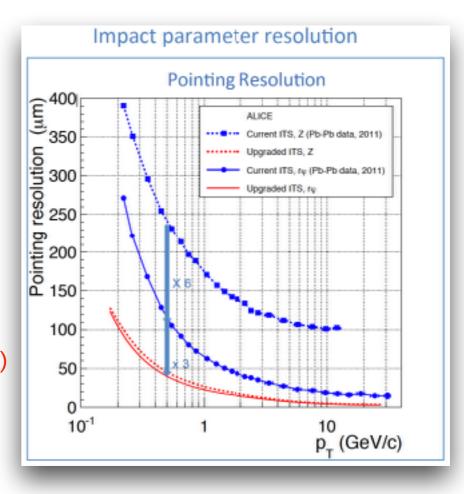
ALICE ITS Upgrade Motivations and Strategy



- Main detector requirements
 - Higher tracking efficiency and resolution at low p_T
 - ▶ Granularity ★ Material budget ↓
 - High-statistics, un-triggered data sample
 - ▶ RO rate ↑ Data size ↓ (Online)



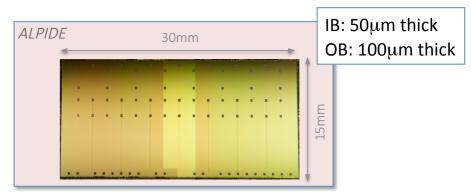
- → New Silicon Tracker (Inner Tracking System) for HL LHC (installation during 19/20)
- Improve impact parameter resolution by a factor of 3
 - Get closer to IP (1st layer): 39 430mm \rightarrow 23 400mm ($|\eta| \le 1.22$)
 - Material budget X/X0 per layer: ~1.14% ➤ ~0.3% (inner)
 - Reduce pixel size: 50μm x 425μm ➤ 28μm x 28μm
- Improve tracking efficiency and \mathbf{p}_{T} resolution at low \mathbf{p}_{T}
 - Increase granularity: 6 layers ➤ 7 layers w. reduced pixel size
- Fast readout: 1 kHz (1kHz) in PbPb (pp) ➤ 100 kHz (400kHz) in PbPb (pp)
- Power density < 40mW/cm²
- Fast insertion/removal for yearly maintenance

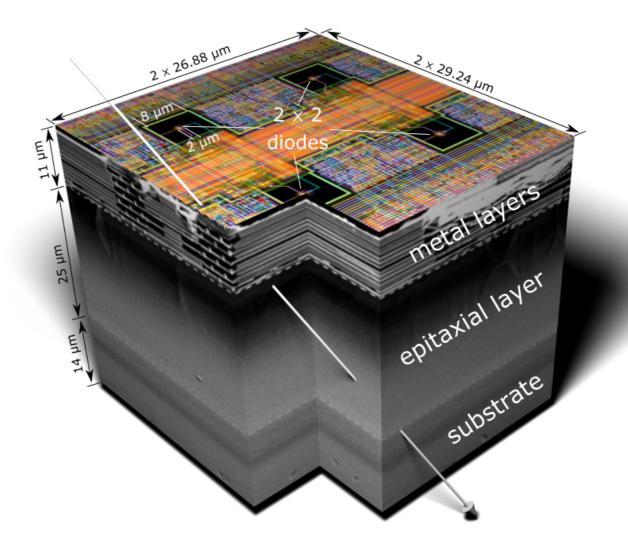


ALPIDE (ALice Plxel DEtector)



- CMOS Pixel Sensor using 0.18µm CMOS Imaging Process
 - Arr High-resistivity (>1kΩ · cm) p-type epitaxial layer (25μm) on p-type substrate
 - ▶ Small n-well diode ($2\mu m \phi$) ~ low capacitance (fF)
 - ightharpoonup -6V < V_{BB} < 0V to increase depletion zone around n-well diode
 - ▶ Deep p-well shields n-well of PMOS transistors
- Full CMOS circuitry within active area
- Pixel: 27 x 29 x 25 μm³
- 130,000 pixels/cm² ~ Total 10m², 12.5 G-pixels
- Spatial resolution ~ 5μm in 3D
- Max. particle rate: 100MHz/cm²
- fake-hit rate ~ 10⁻¹⁰ pixel/event
- Power ~ 300 nW/pixel



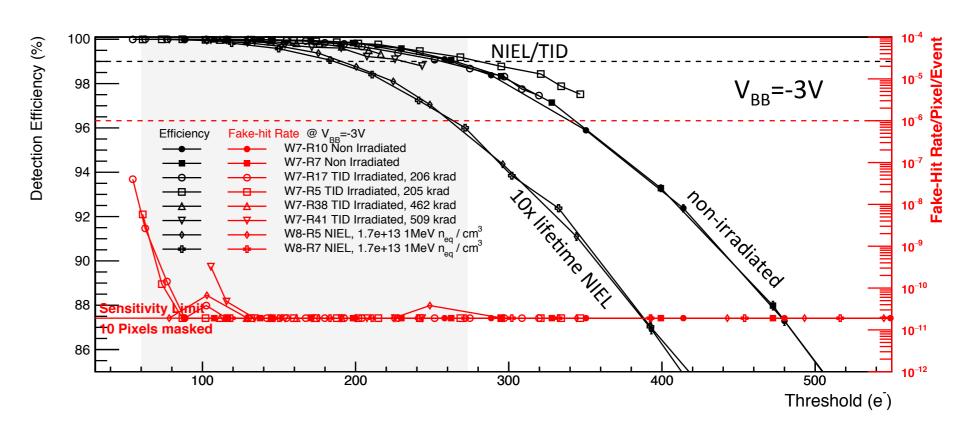


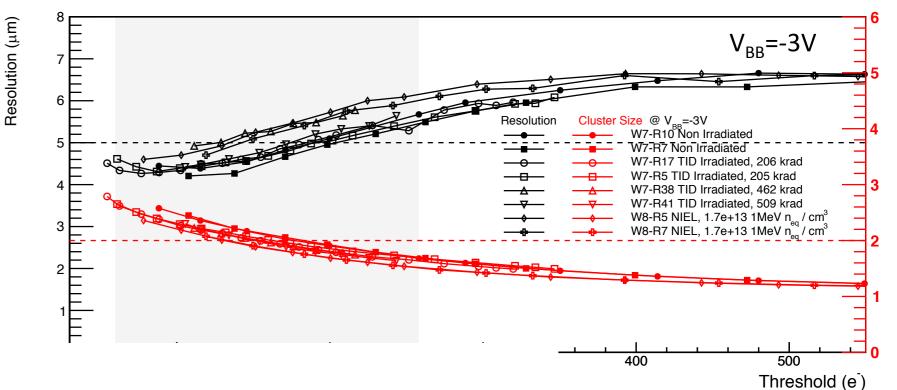
ALPIDE (ALice Plxel DEtector) Performance



Average Cluster

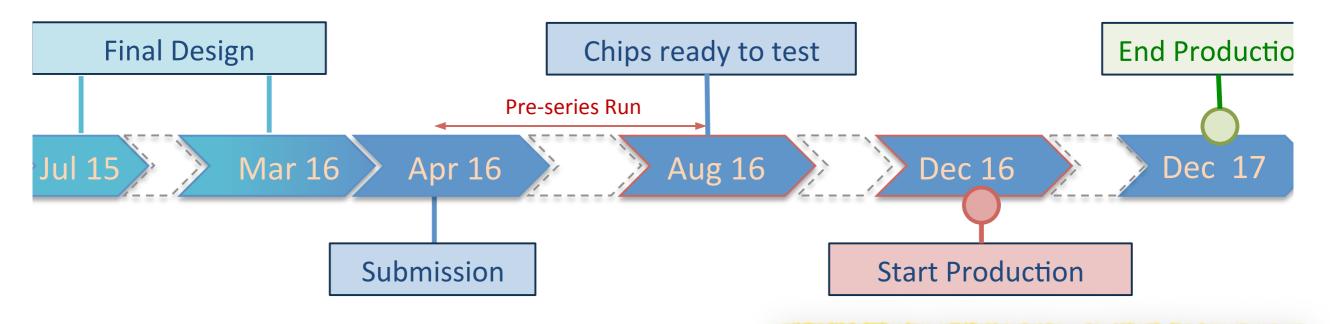
- Detection efficiency and Fake-hit rate
- Resolution and Cluster size
 - Non-irradiated and NIEL/TID chips ~ similar
 - Sufficient operational margin after 10 x lifetime NIEL dose
 - Resolution < 5μm at Threshold < 150 e
 - Resolution ~ 6μm at Threshold of 300 e
 - Chip-to-chip fluctuations negligible





ALPIDE (ALice Plxel DEtector) Plan





Pixel Chip Finalization and Production Timeline

Engineering	Design	Review	Oct 15 🗸
	DCJIBIT	I (C V I C V V	

- Complete design of final ALPIDE Mar 16 🗸
- ▶ Pre-series Run Aug 16
- ▶ Validation of final chip Nov 16 ✔
- ▶ Production Readiness Review Nov 16 ✔
- ▶ Start Series Production → Dec 16

March 2017

Delivery of first batch of wafers

TOWER => FUREX (KR)

- Delivery of first batch of chips
 - FUREX => Yonsei, Pusan/Inha (KR)
- 30% of Chip production completed by Tower (current)

ALPIDE - Mass Chip Test

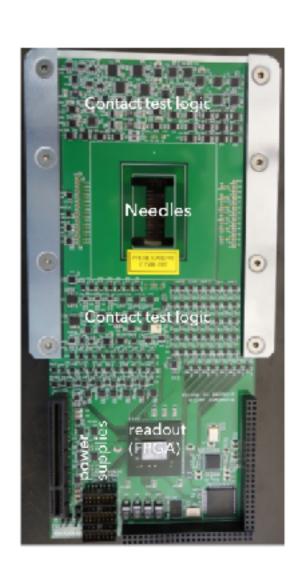




ALICIA (IBS) 3 machines 1 Pusan/Inha (KR), 2 CERN



Corea-YS01 (C-On)
1 dedicated chip ATE
Yonsei (KR)

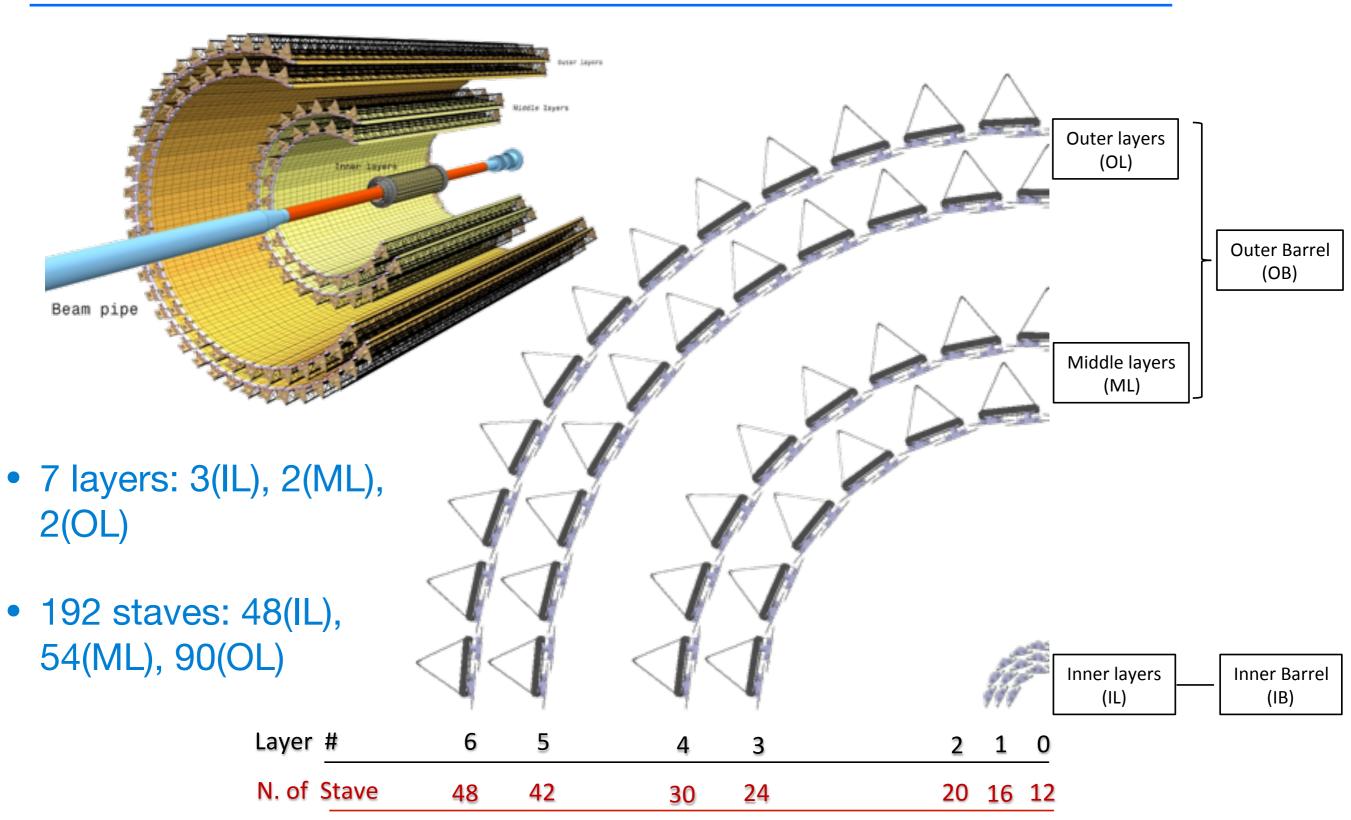


Probe Card CERN, Yonsei, NOTICE + EQ&G (KR)

Dress rehearsal at Yonsei & Pusan/Inha: DONE on 31 Mar. 2017

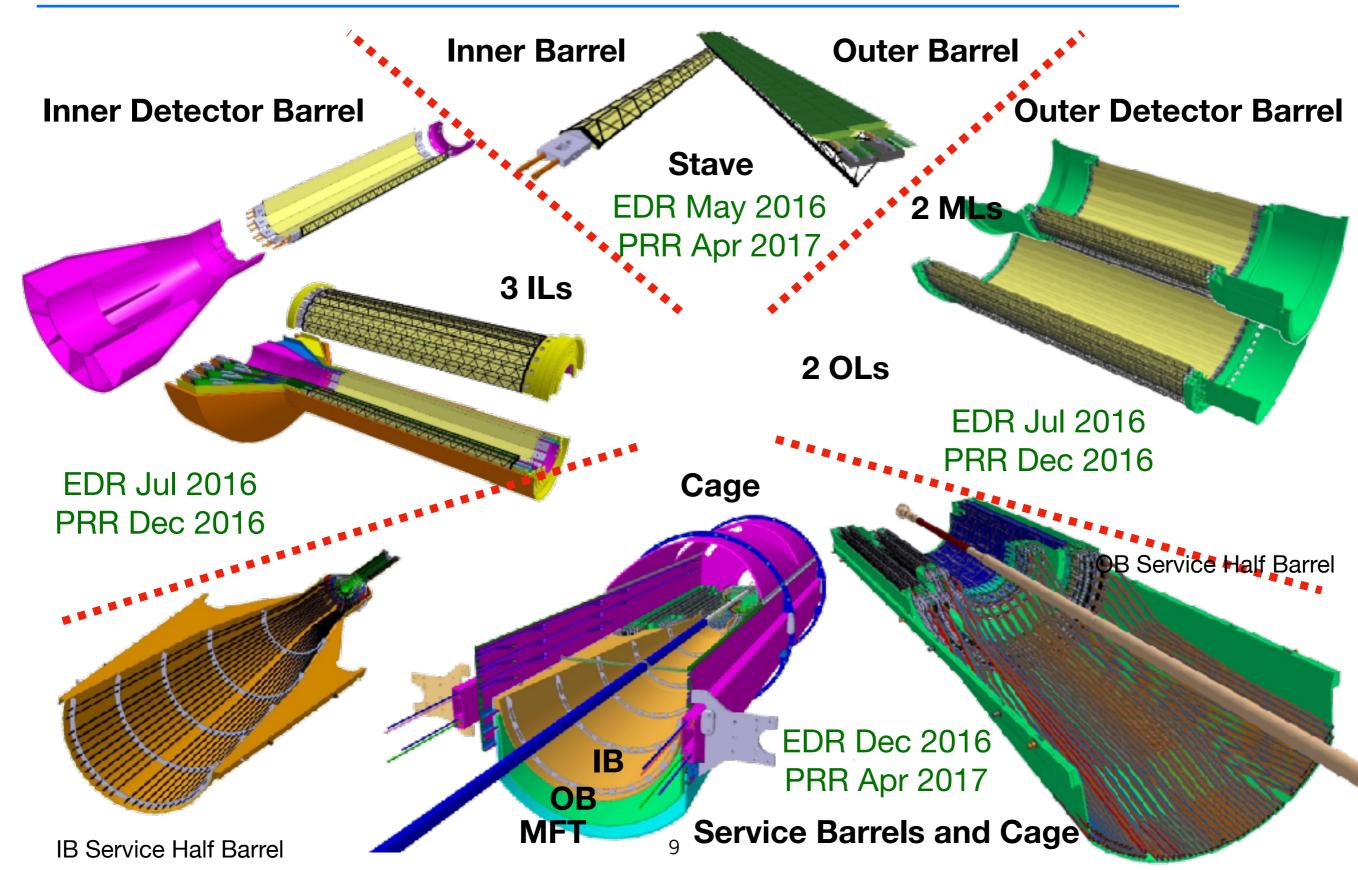
Detector Barrel Staves





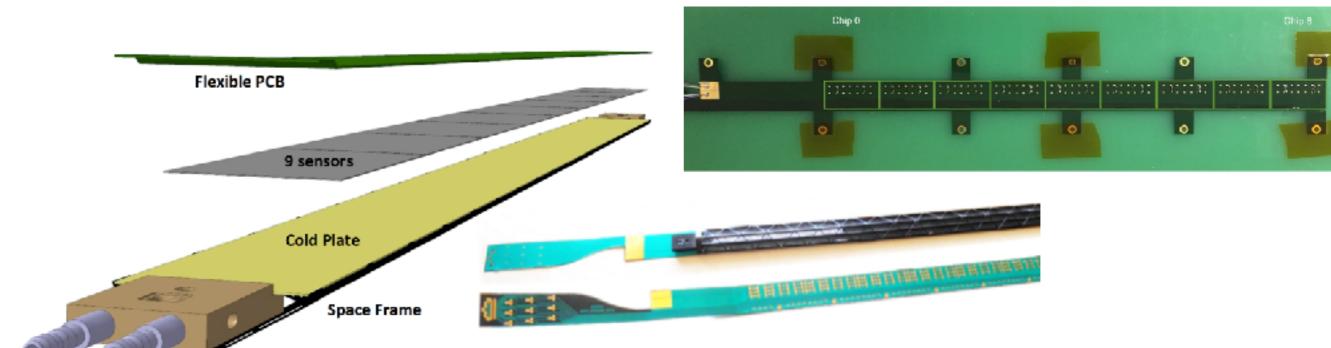
Detector Barrel and Service Barrel Mechanics



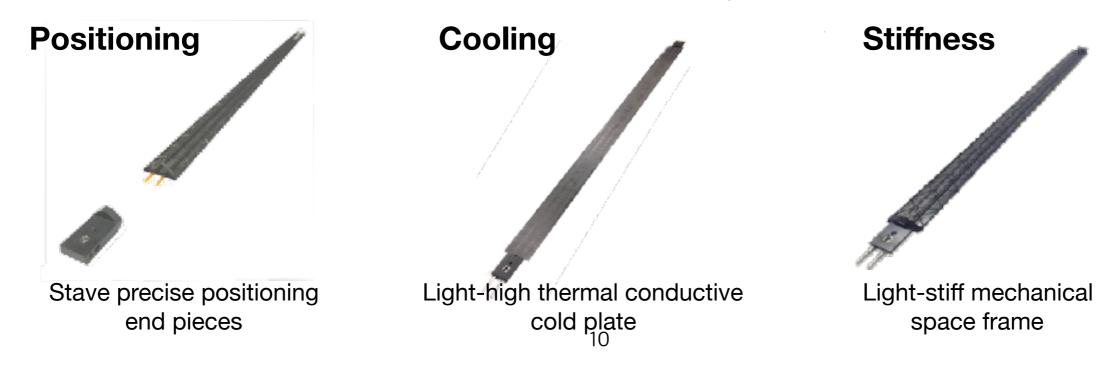


IB - Stave Production



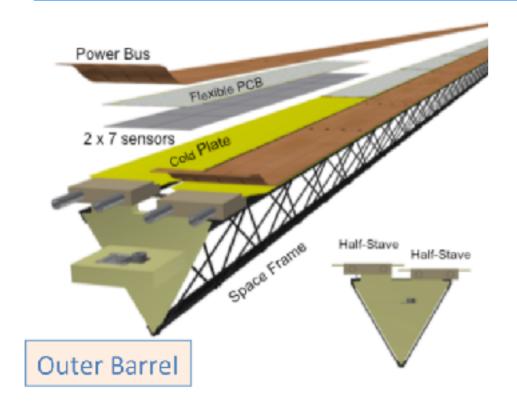


- Full characterization with different modes of operation, RO rates and environmental conditions (supp. V and T)
- Sensor performance same as for standalone chip



OB - Stave Production







- Full characterization with different modes of operation, RO rates and environmental conditions (supp. V and T)
- Sensor performance same as for standalone chip



Stave precise positioning end pieces

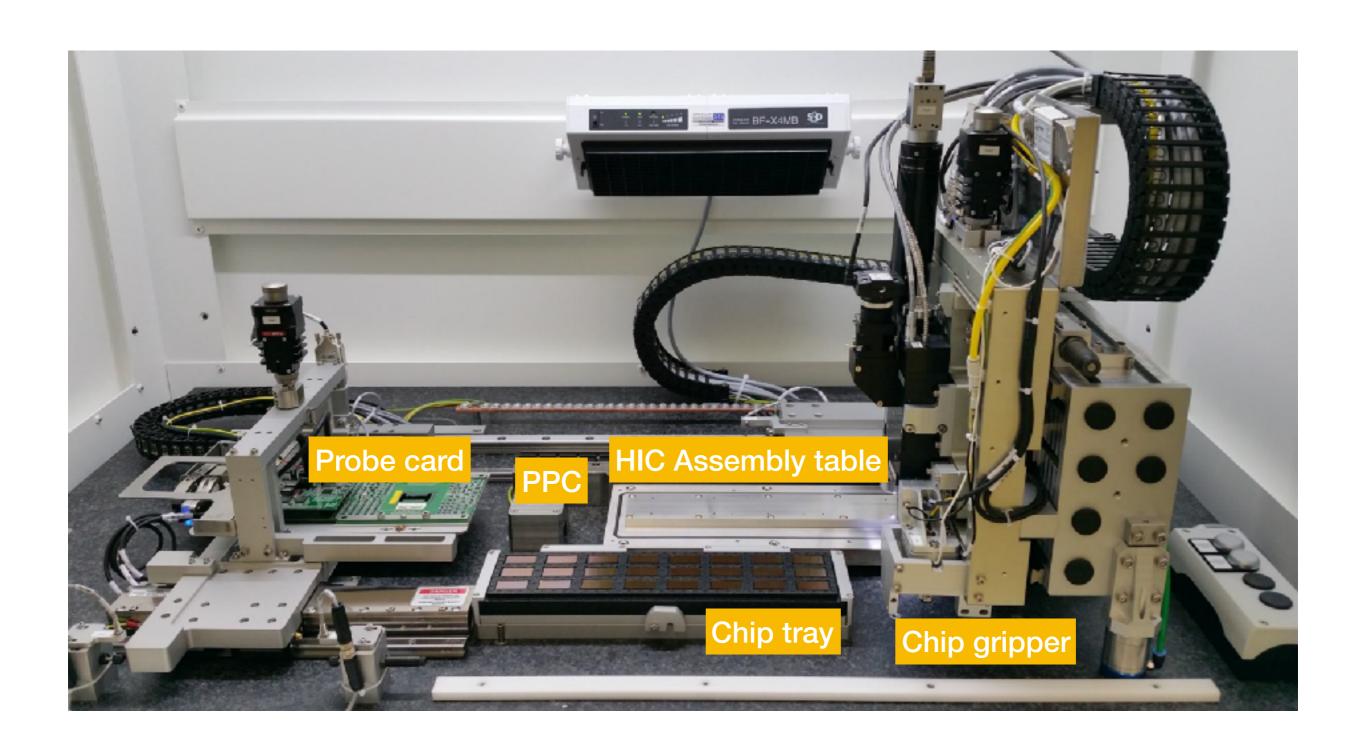


Light-high thermal conductive cold plate

Cooling

Module Assembly Machine





Site Acceptance Tests



Name	Institute	FAT date	FAT status	Delivery	SAT date	SAT status
ALICIA-3	Bari, Italy	03/10/16	ОК	Week 41	17-20/10/16	OK
ALICIA-2	Pusan/INHA, Korea	10/10/16	ОК	Week 43	07-11/11/16	OK
ALICIA-6	Wuhan, China	10/10/16	ОК	Week 44	17-23/11/16	OK
ALICIA-5	Strasbourg, France	27/10/16	ок	Week 46	21-24/11/16	OK
ALICIA-4	Liverpool, UK	27/10/16	ок	Week 49	12-14/12/16	OK
ALICIA-7	Saclay, France (MFT)	28/11/16	ок	Week 03 (2017)	16-20/01/17	OK









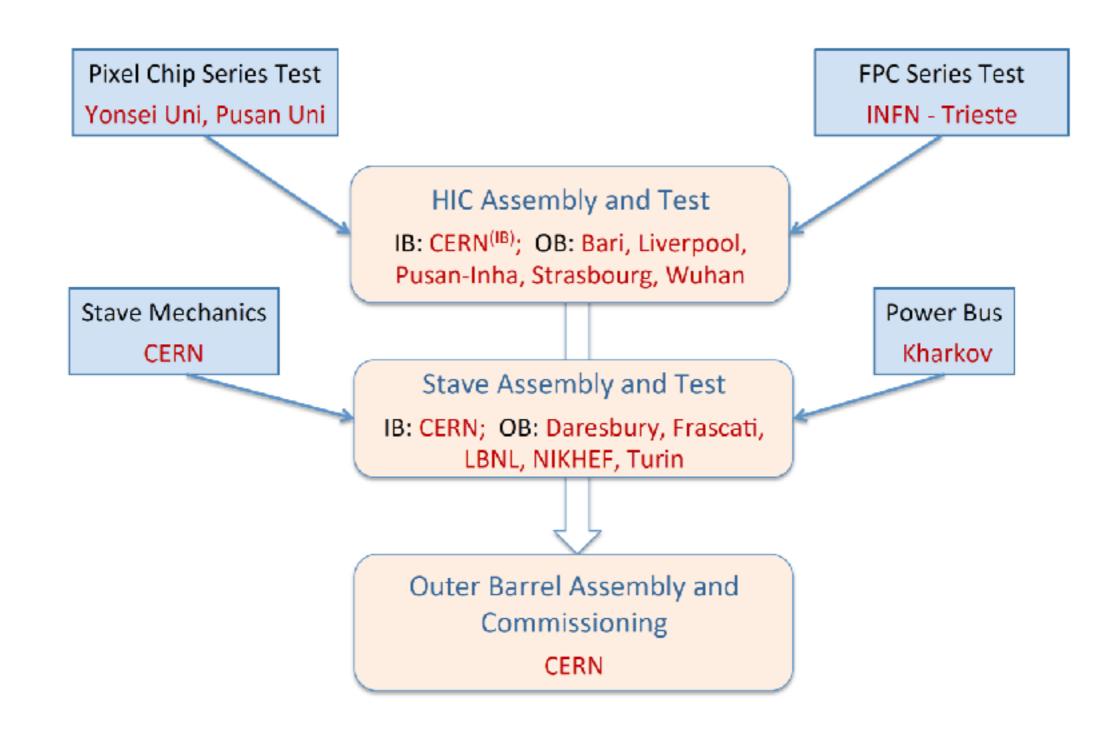






OB Stave Construction Flow





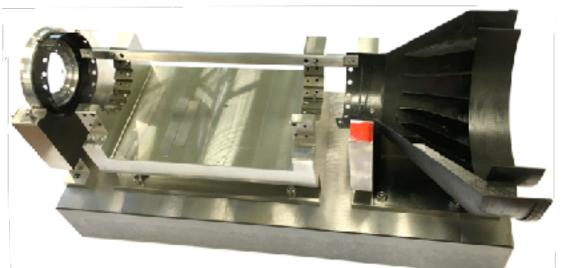
Detector Barrel and Service Barrel Mechanics

End Wheel A side



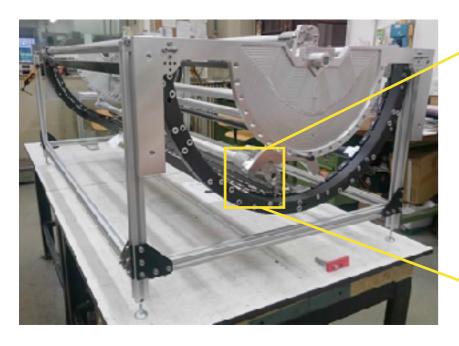
Prototype of IB End Wheels (EWs), Space Frames and Cold Plates

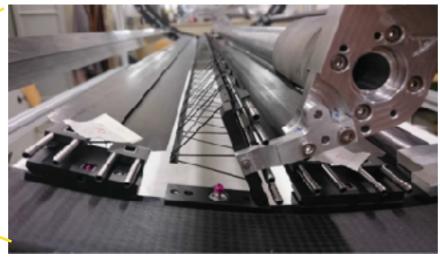
End Wheel C side

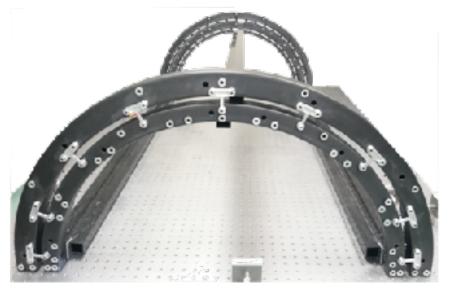




Prototype of OB End Wheels (EWs), Space Frames and Cold Plates



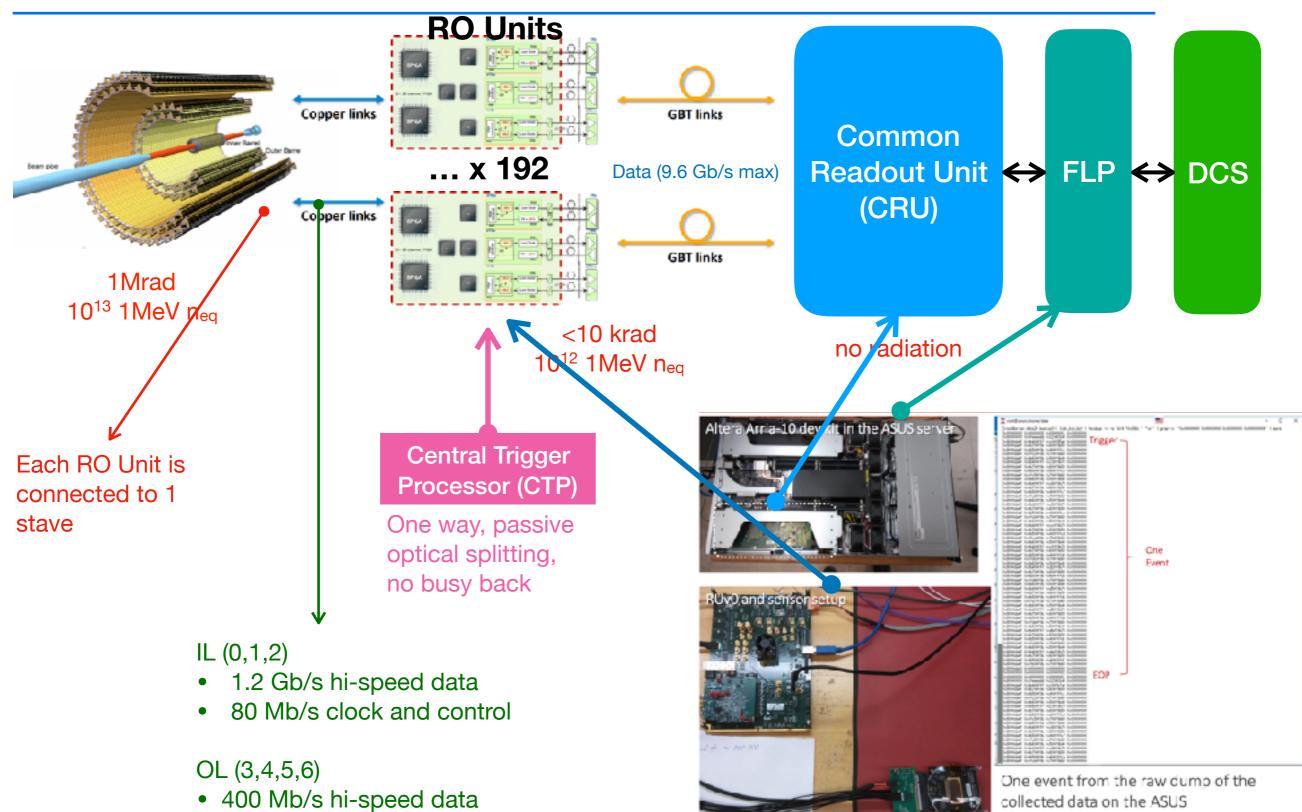




OB End Wheel

Readout Electronics - EDR (Jan 17)





Austin, Bergen, CERN, Nikhef, INFN-PD

• 80 Mb/s clock and control

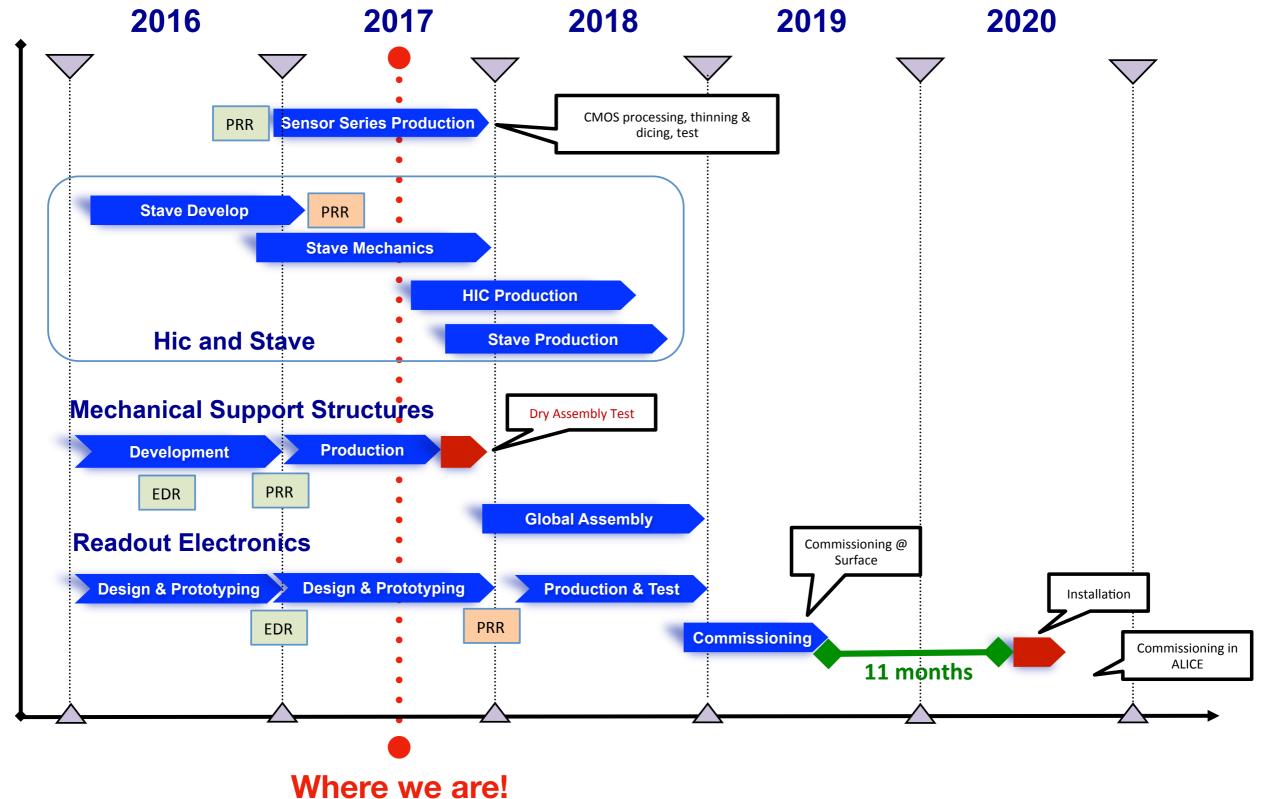
ALICE ITS Upgrade - Status and Plan



System`	Review	Schedule	Status
Pixel Sensor Chip	EDR	Oct 2015	✓
Pixel Sensor Chip	PRR	Sep 2016	√
HIC & Stave	EDR	May 2016	✓
HIC & Stave	PRR	Dec 2016	√
Detector Barrel Mechanics	EDR	Jul 2016	✓
Detector Barrel Mechanics	PRR	Nov 2016	✓
Service Barrel Mechanics	EDR	Nov 2016	✓
Service Barrel Mechanics	PRR	Feb 2017	✓
Cooling Plant	EDR	Jul 2016	✓
Cooling Plant	PRR	Dec 2016	1
Readout Electronics	EDR	Dec 2016	√
Readout Electronics	PRR	Dec 2017	

Overall ITS Planning







All components are ready to go for sequential batch procedures.

Veel dank