# YARR for RD53A

## RD53A Meeting - 20.10.2016

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# YARR in a Nutshell

## Hardware:

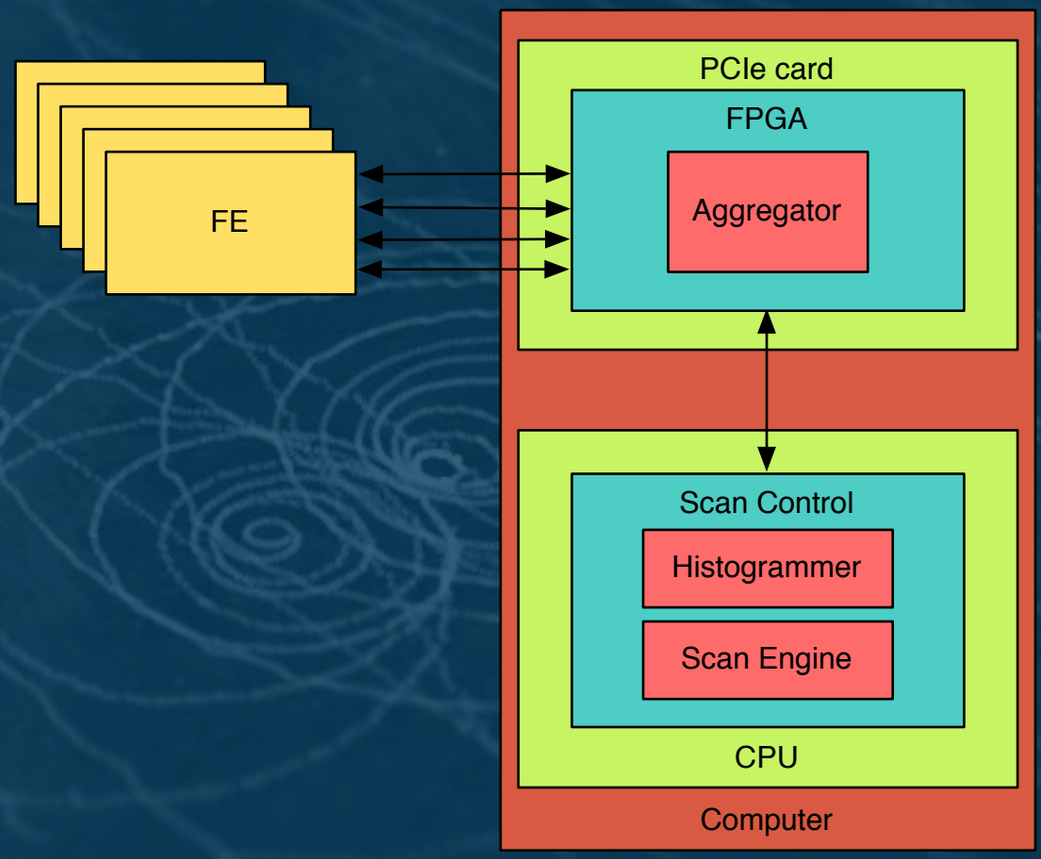
- COTS PCIe FPGA board
- Custom adapter boards connecting to common FMC connector, specific to each FE or purpose

## Firmware:

- Commands are sent via FIFOs
- Data is received, deserialised, decoded and then buffered in DDR RAM
- Chunks of data are transferred via DMA into host memory
- No preprocessing of data performed

## Software:

- Contains all intelligence
- Scan engine performs looping actions, e.g. select pixels, inject & trigger, etc
- Data processing, histogramming and analysis decoupled from scan engine in a modular multi-threaded architecture

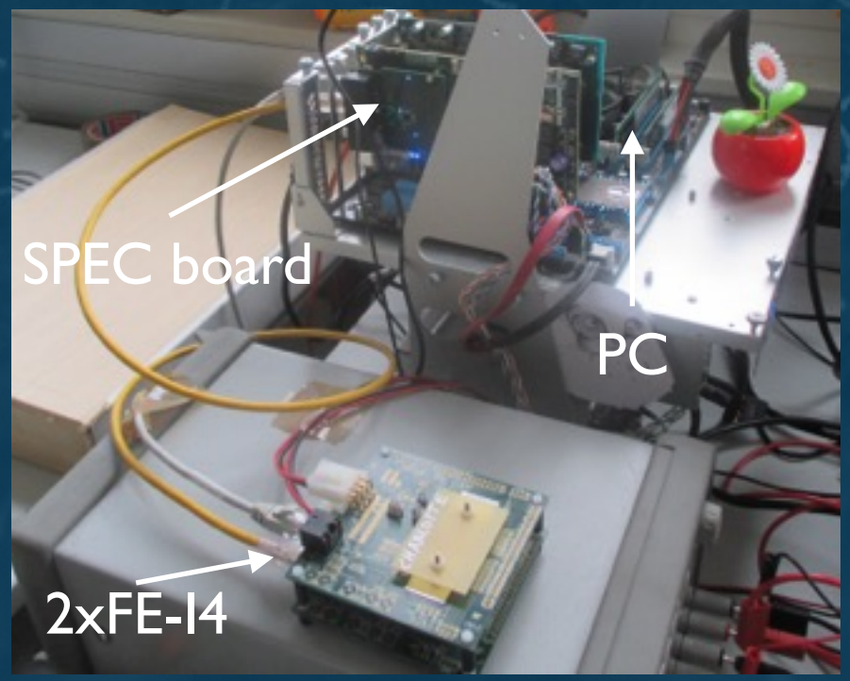


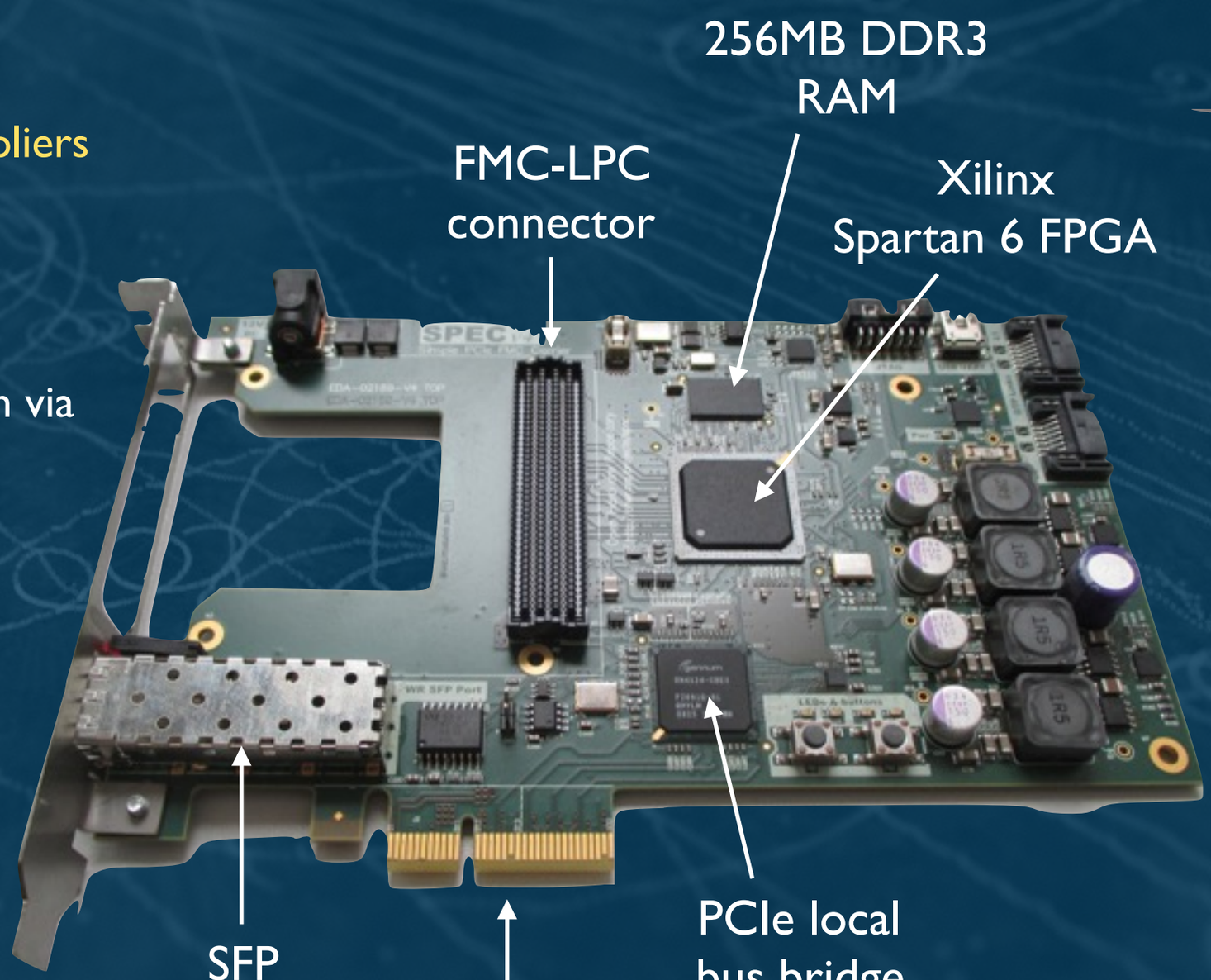

https://github.com/Yarr/Yarr/tree/devel

# Current Hardware

PCIe card:

- Simple PCIe carrier (SPEC) board developed by CERN
- Available from multiple industrial suppliers for about 700$
- Xilinx Spartan 6 FPGA
- FMC-LPC has 34 LVDS pairs, max bandwidth of 1080 Mbps per pair
- Achieving around 3.2Gbit/s bandwidth via PCIe



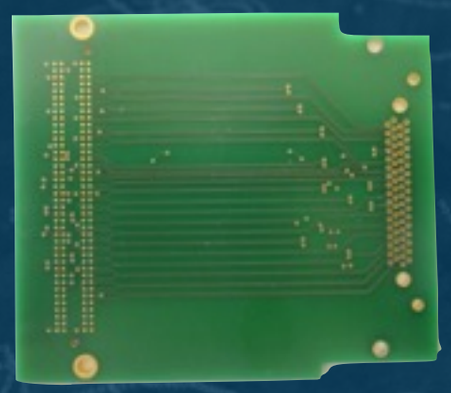




www.ohwr.org/projects/spec/wiki

# FE-I4 & FE65-P2 Adapter Cards

FE-I4:
- Three LVDS interface: Clk, Cmd, DataOut
- Clk/Cmd 40Mhz/40Mbps
- DataOut 160Mbps
- Using RJ45 connector and Ethernet cables

FMC to VHDCI



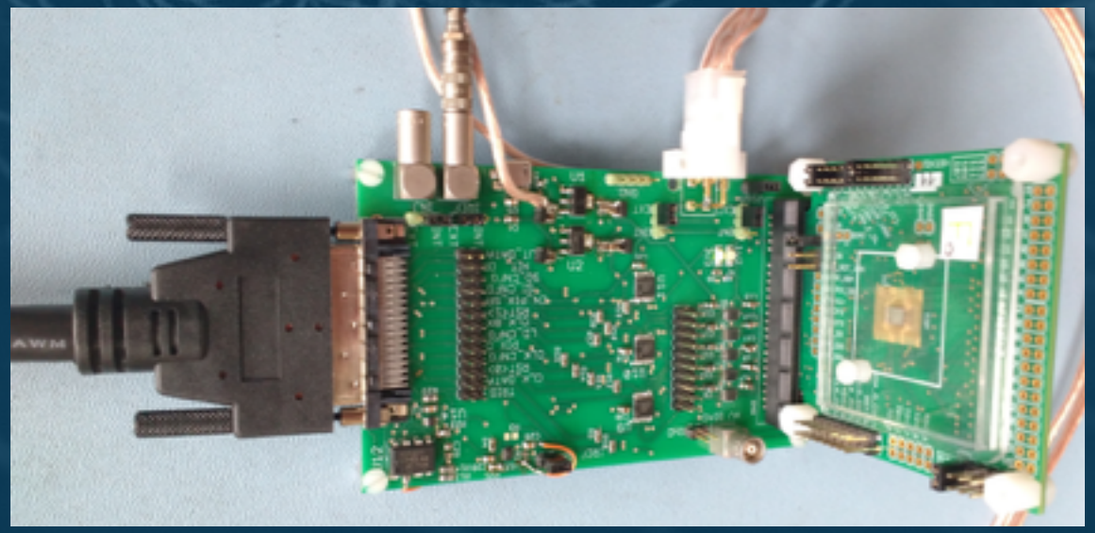
34xLVDS

VHDCI to 8 x RJ45

FMC to Quad RJ45

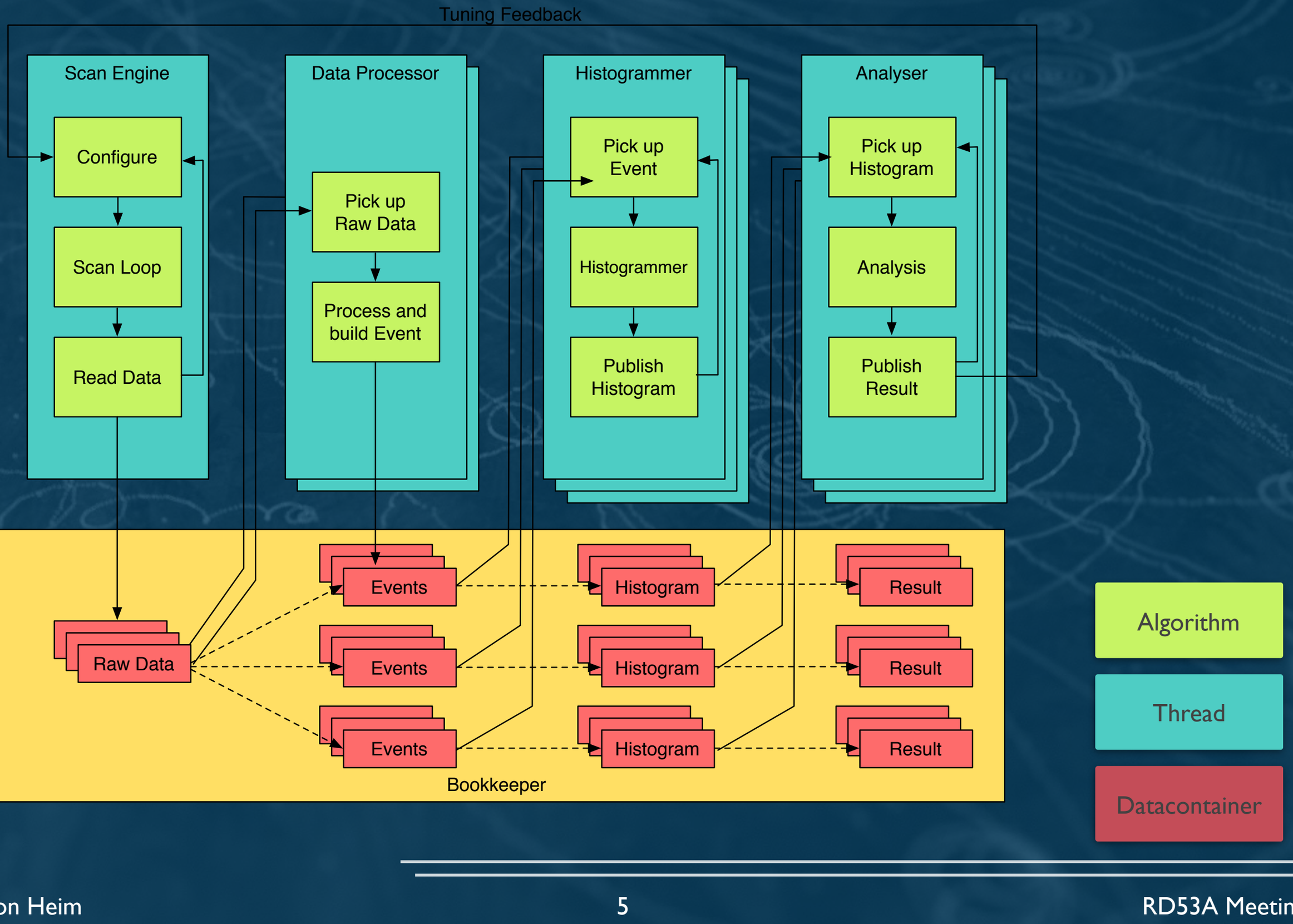
FE65-P2:
- CMOS 1.2V signals
- Total of 10 signals for SPI, trigger and reset
- 3 Clk inputs
- Pseudo differential hitOr and data output
- Needs external reference current

FE65-P2 Adapter Card + Single Chip Card



LVDS → CMOS 3.3V → CMOS 1.2V

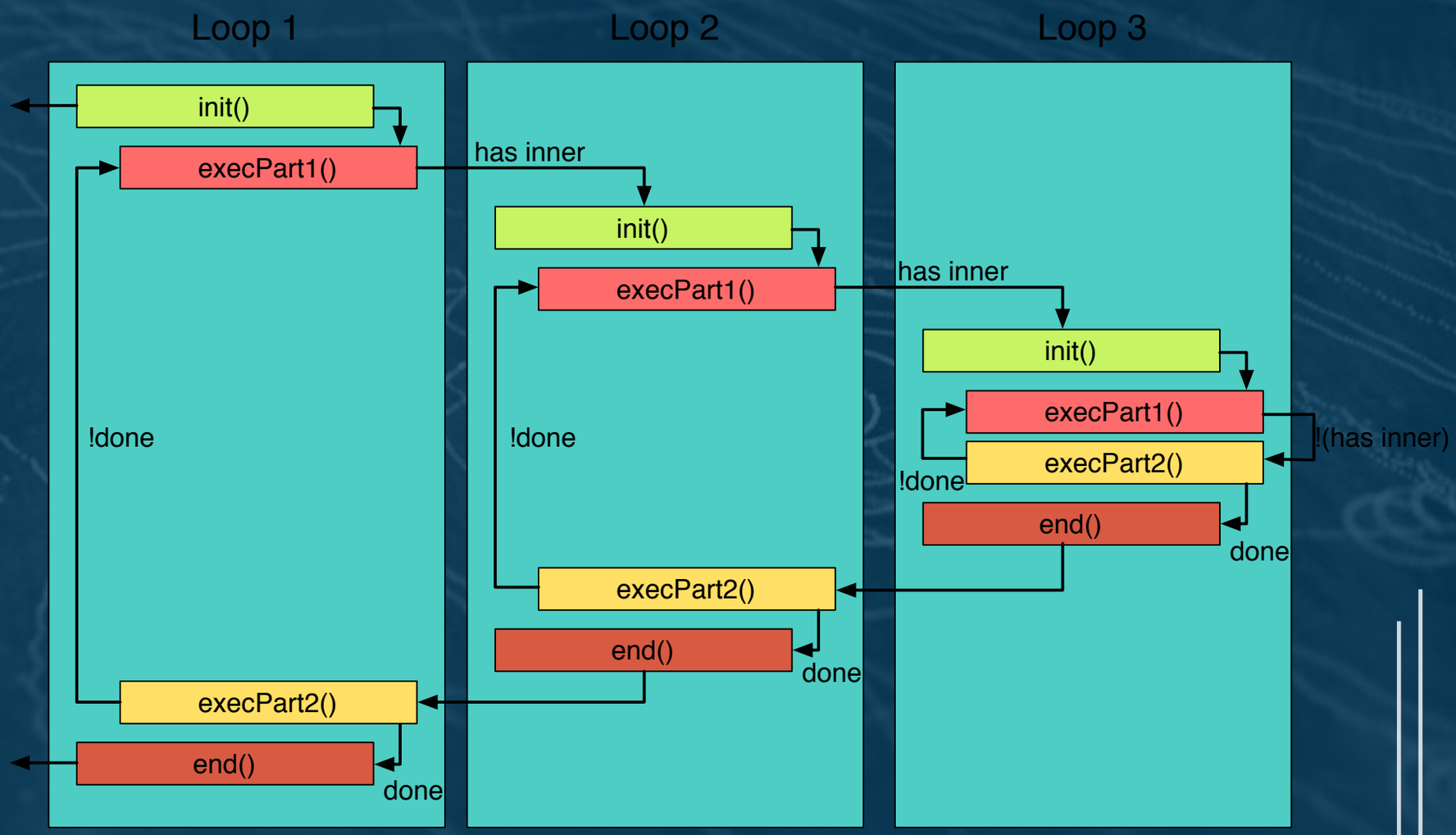
# Software


Tuning Feedback
Scan Engine
Configure
Scan Loop
Read Data
Data Processor
Pick up Raw Data
Process and build Event
Histogrammer
Pick up Event
Histogrammer
Publish Histogram
Analyser
Pick up Histogram
Analysis
Publish Result
Raw Data
Events
Events
Events
Histogram
Histogram
Histogram
Result
Result
Result
Bookkeeper
Algorithm
Thread
Datacontainer

# Scan Engine

Scan:
- Collection of nested loops
- Specified in scan config
- Dynamically constructed at runtime
- No fixed number of loops
- No fixed order of loops

Loop Actions:
- Change registers
- Activate portions of pixels
- Inject & trigger
- Loop over columns



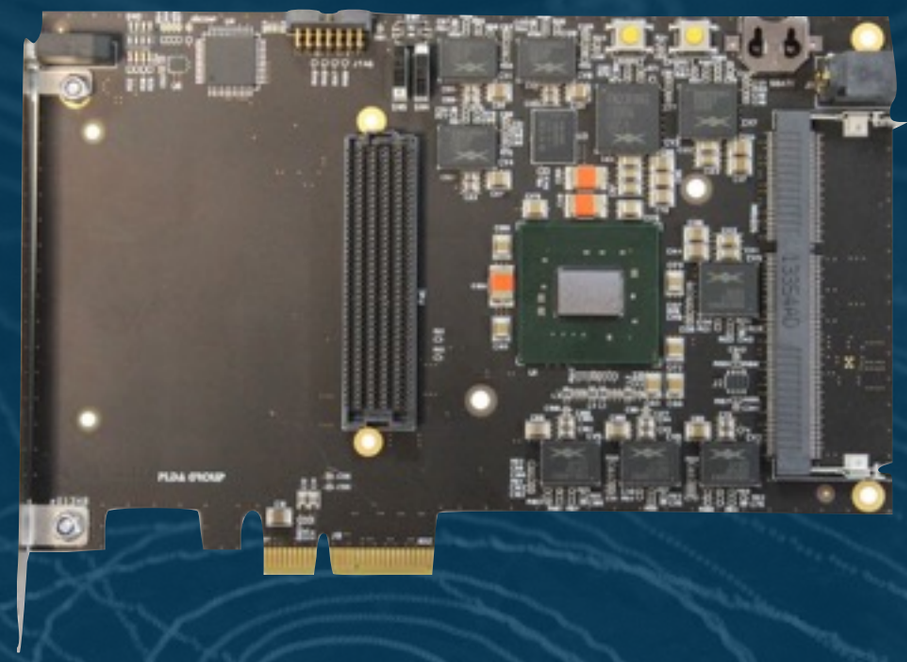
# Integration of FE65-P2

- Pixel chips often work in similar manners:
  - Scans: configure, select portion of pixels, inject & trigger, readout
  - Data taking: receive/generate trigger, readout
- Main difference of FE65-P2 to FE-I4 is the physical interface, which is being adapted to a FE-I4-like serial interface in firmware
- Parts in software specific to FE65-P2: configuration, commands, loop actions/scans and first stage data processing
- Parts in software shared with FE-I4: histogramming, analysis, tuning procedure
- Flexibility in software very useful during chip characterisation

# Debugging capabilities

- Initial chip characterisation != typical chip operation
- Special features in firmware:
  - ChipScope: in FPGA logic analyzer to track en/decoding issues
  - TDC or delay lines with sub ns resolution placable
  - Simple interfacing with external signals, e.g. pulser for injection
- Special features in software:
  - Full raw data stream available → Low level debugging in software
  - Highly flexible scan structure, loops quickly swapped or changed
  - Configuration and commands fully contained in software
  - All tools available via command line → no clumsy GUI handling
- Inclusion of typical test bench hardware via GPIB to USB

# Hardware for RD53A

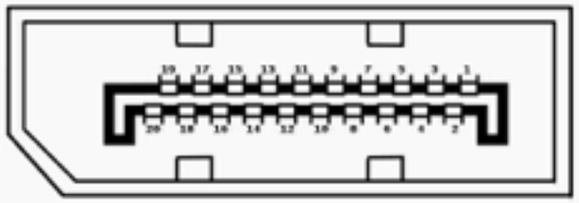


## Hardware:

- RD53A link speed requires new hardware
- Developing on PLDA XpressK7
  - ~1200$ available from multiple distributors
  - Partial FMC-HPC interface
    - 4 x 5Gbit/s links or many <1.2Gbit/s links
  - SO-DIMM for up to 4GB DDR3
  - 4 x PCIe v2 (perhaps v3) ≈ 20Gbit/s
- In the process of migrating current SPEC firmware
- Other PCIe board exists, but are more expensive
- Backwards compatible with old adapter Boards

## Adapter Board:

- Planning to use DisplayPort
  - 4 high speed lanes rated up to 8Gbit/s
  - 1 slow link rated up to 720 Mbit/s
- Has power but only rated for 3.3V/ 500mA
- Cables readily available
- Also compatible with Mini-DisplayPort
- Will already be used for the chip emulator



External connector (source-side) on PCB

| | | |
|---|---|---|
| Pin 1 | ML_Lane 0 (p) | Lane 0 (positive) |
| Pin 2 | GND | Ground |
| Pin 3 | ML_Lane 0 (n) | Lane 0 (negative) |
| Pin 4 | ML_Lane 1 (p) | Lane 1 (positive) |
| Pin 5 | GND | Ground |
| Pin 6 | ML_Lane 1 (n) | Lane 1 (negative) |
| Pin 7 | ML_Lane 2 (p) | Lane 2 (positive) |
| Pin 8 | GND | Ground |
| Pin 9 | ML_Lane 2 (n) | Lane 2 (negative) |
| Pin 10 | ML_Lane 3 (p) | Lane 3 (positive) |
| Pin 11 | GND | Ground |
| Pin 12 | ML_Lane 3 (n) | Lane 3 (negative) |
| Pin 13 | CONFIG1 | connected to Ground[1)] |
| Pin 14 | CONFIG2 | Connected to Ground[1)] |
| Pin 15 | AUX CH (p) | Auxiliary Channel (positive) |
| Pin 16 | GND | Ground |
| Pin 17 | AUX CH (n) | Auxiliary Channel (negative) |
| Pin 18 | Hot Plug | Hot Plug Detect |
| Pin 19 | Return | Return for Power |
| Pin 20 | DP_PWR | Power for connector (3.3 V 500 mA) |

# Software for RD53A

- Use same concept already in place for FE-I4 and FE65-P2
- Integration of FE65-P2 already forced FE abstraction, adding another type of FE very easy
- Performance benchmarks show that a standard modern PC should be able to handle the amount of data
- As there is no processing of either commands or data in firmware, software could interface with chip simulation (via dummy hardware controller)
- Planning on preparing a simplified software chip emulator, this helps during development as software can be tested w/o hardware

# Status & Plans

- One master student currently working on migration of firmware to Kintex 7 platform, should have first benchmark results by December
- One grad student will start in December and prepare the software integration, as well as possible interfacing with chip simulation/ verification
- One undergrad working on cheap Arduino controlled Peltier cooler
- One postdoc will work on the software chip emulator
- Working in close collaboration with Washington group, who is working on the emulator which will also provide transmitter and receiver block (see Logans talk)
- Software is intended to be hardware agnostic, in such a way that the core can be reused with the full scale detector DAQ → wider range of hardware might become available