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SI LAB
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RD53A Test System
Status and Plans

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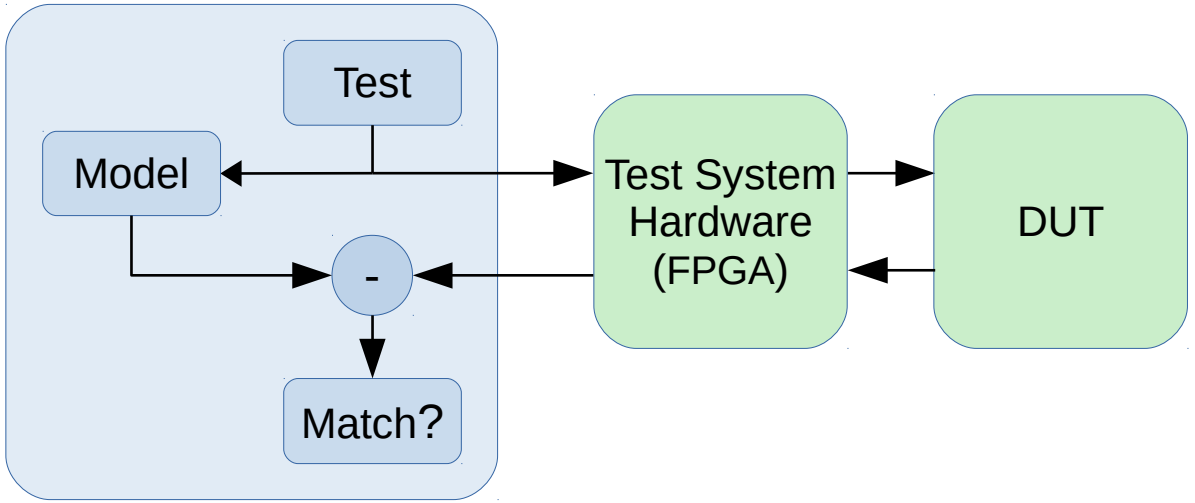
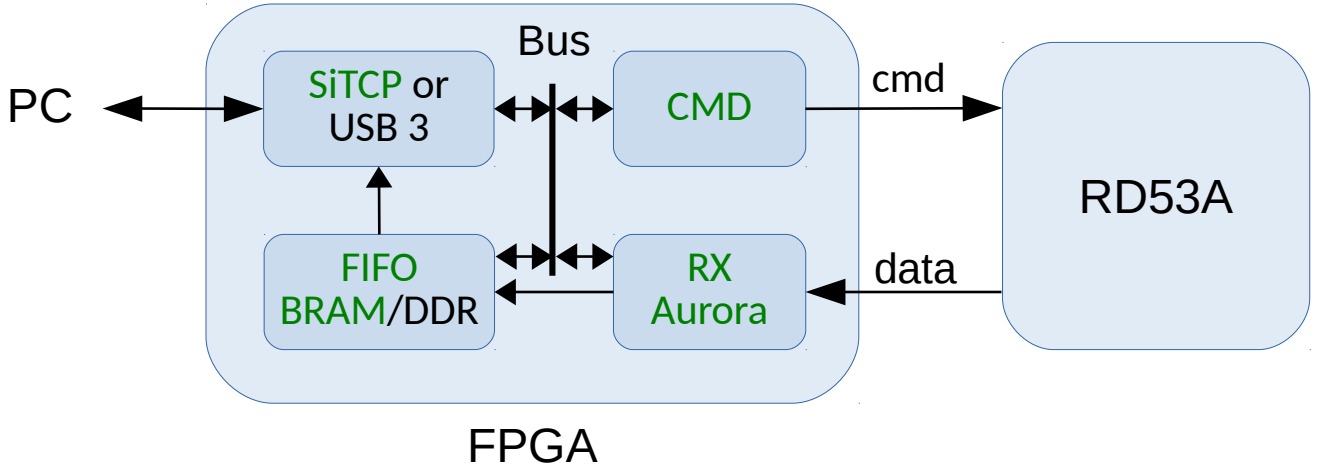
RD53A Test System - Overview

- Development should cover verification phase, first single chip tests and module tests.
- Basic concept:
  - Generate test patterns (e.g. constrained random) or load them from file.
  - Use FPGA to configure DUT and send test patterns.
  - Receive DUT response through FPGA and compare with prediction.



RD53A Test System - Firmware

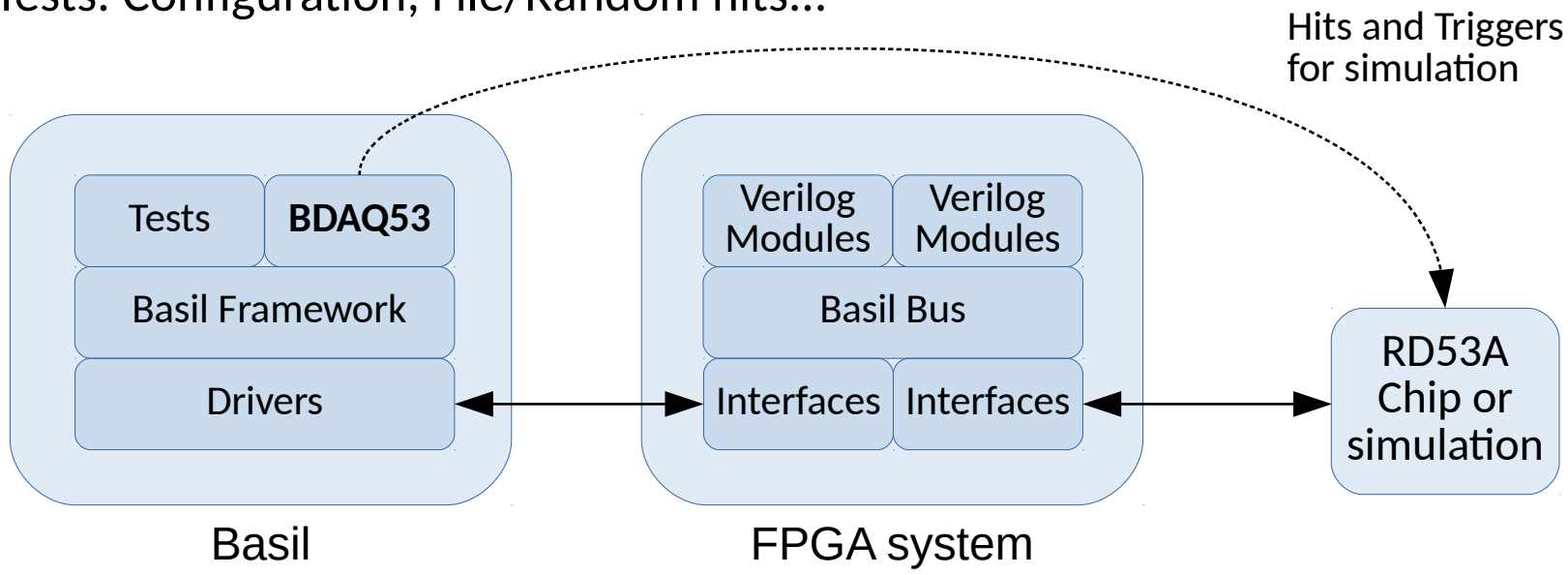
- Verilog modules for FPGA
  - Command encoder “CMD” to configure the chip,
  - Hardware interfaces like DDR3 memory, Ethernet…
  - Aurora protocol, using Multi-Gigabit-Transceivers (MGT) for RD53A data.



  - CMD, RX (single channel): Done, Available on GitLab
  - SiTCP: Project at KEK
  - FIFO: BRAM as Basil module, DDR3: WIP

RD53A Test System - Software

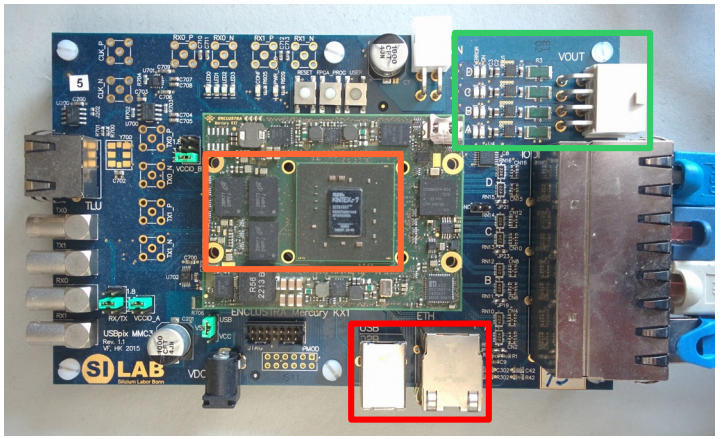
- Existing Python-based DAQ-framework **Basil** can be used for testing.
- With the library **cocotb**, Basil framework allows the same code to be used for the FPGA system and also during verification process.
- Automatic code testing after every commit, using Continuos Integration.
- Already used for verification, test system to be ready when chips arrive.
- Tests: Configuration, File/Random hits…



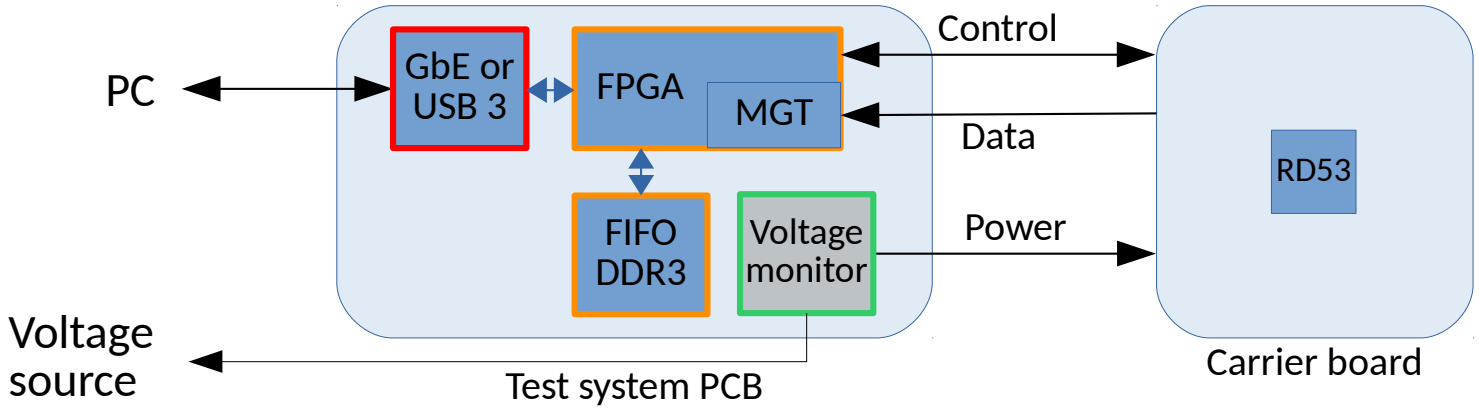
RD53A Test System - Hardware

- New flavor of existing MMC3 PCBs (Kintex 7), which already includes
  - **large memory** (FIFO) ~ 1 GByte for buffered readout,
  - **Gigabit Ethernet** and **USB 3** interface,
  - 2x MGT, voltage and current **monitors.**

  Design will be modified to support:
  - 4x multi-gigabit links (**MGT**: ≤12 Gbit/s each).
- Alternativly: Evaluation board + FMC card.
- Carrier PCB, mostly passive.

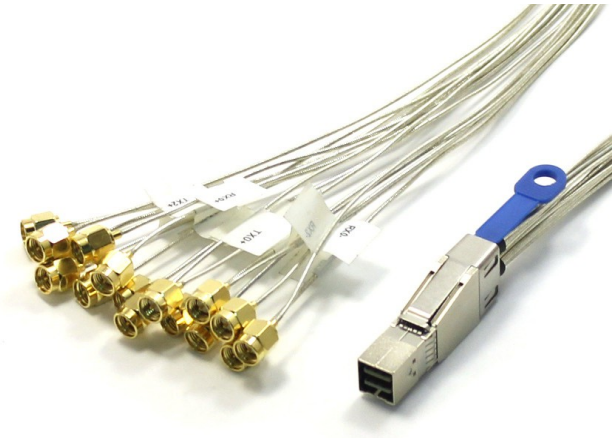


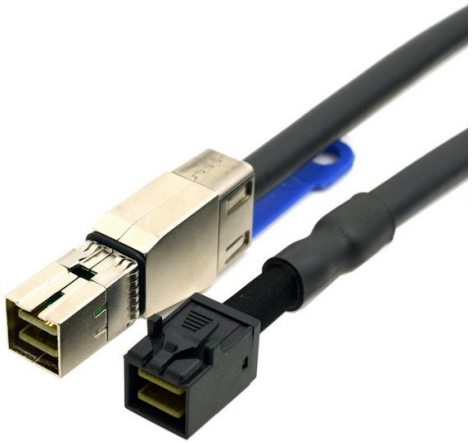
MMC3 setup



RD53A Test System - Hardware

- "Slow" control- and debug signals: Ribbon cable and IDC connectors.
- MGT Requirements:
  - 1 or 4 differential pairs (100 Ohm) per chip, up to 5 Gbit/s.
- Proposed connector for high speed data: Mini-SAS HD
  - Industry standard (SFF-8644) for server storage, up to 8x 12 Gbit/s.
  - “Internal” (plasic) and “external” (metal) variants, small footprint.
  - Widely available and reasonably priced.





RD53A Test System - Status

- FPGA configuration
  - Command encoder: Works with RD53A digital design model
  - DDR3 memory (1 Gbyte): Works on a basic level,
    wrapper for Basil integration: TBD
  - Aurora protocol: Ready on simulation level
  - Ethernet/USB 3: Evaluation
- Software integration
  - Basic commands, register read/write, triggers: Done
  - Design and implementation of tests: WIP
- PCB-Design: Planing

RD53A Test System - Sources

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- Main repository for BDAQ53:
  https://gitlab.cern.ch/rd53/RD53A/tree/master/sim/bdaq53
- Basil Framework:
  https://github.com/SiLab-Bonn/basil
- MMC3 Hardware:
  http://icwiki.physik.uni-bonn.de/twiki/bin/view/Systems/UsbPix
- Cocotb Library:
  http://potential.ventures/cocotb/
- SiTCP Stack:
  http://research.kek.jp/people/uchida/technologies/SiTCP

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Thank you

RD53A Test System - Outlook

- Possible development for large scale testing:
  - Integrated Processor like the open ISA RISC-V.
  - Parametrized threshold/bias tuning can be offloaded into the test system.
  - First tests with RISC-V, interfacing the Basil-bus were successful.