RD53A Emulator Status and Plans

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RD53A Testing Meeting
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Overview

- Motivations for RD53 Emulator
- Collaborators
- Current Implementation
- Development Plans/Testing

Motivations

- Stand in for RD53A chip before it is available.
- Implementation of digital communication blocks on an FPGA – can be used to test with different systems by providing I/O shell decoupled from internal logic blocks
- Can be used to test with various encoding schemes
  - 8b/10b, 64b/66b, Aurora, etc.

Collaborators

- Joe Mayer began work on the emulator (graduated)

- Logan Adams – Graduate student working on emulator
- Dustin Werran – BS/MS student working on emulator
- Douglas Smith – Undergraduate student aiding in local test setup

- Advised by
  - Shih-Chieh Hsu (UW Physics)
  - Scott Hauck (UW EE) – FPGA professor

- Working with Timon and Maurice and others to ensure emulator project is as useful to all as possible

Current Implementation

- Simulation model of RD53A emulator working
  - Using locally designed trigger and command encoding until a more permanent one is made available
  - Currently uses 4 1.25 Gbit links (Need to add 5 Gbit link)
  - Clock and Data recovery and prevention from bit slips as well as channel alignment all implemented
- Model of a “DAQ” system also developed to test communication before working with real next-gen DAQ systems
- Using a Xilinx KC705 FPGA Development Board for testing
  - Provides a variety of digital I/O that can be used to communicate with other boards

Development Plans

- Get current encoding implemented in emulator
- Add 5Gbit link in addition to 4 1.25 Gbit links mode
- Communication on 1 FPGA with our “DAQ” system
  - Loopback test on 1 FPGA
- Communication on 2 FPGAs
  - Communicating with a real readout system such as RCE running on HSIO boards to act as a proof of concept
  - YARR

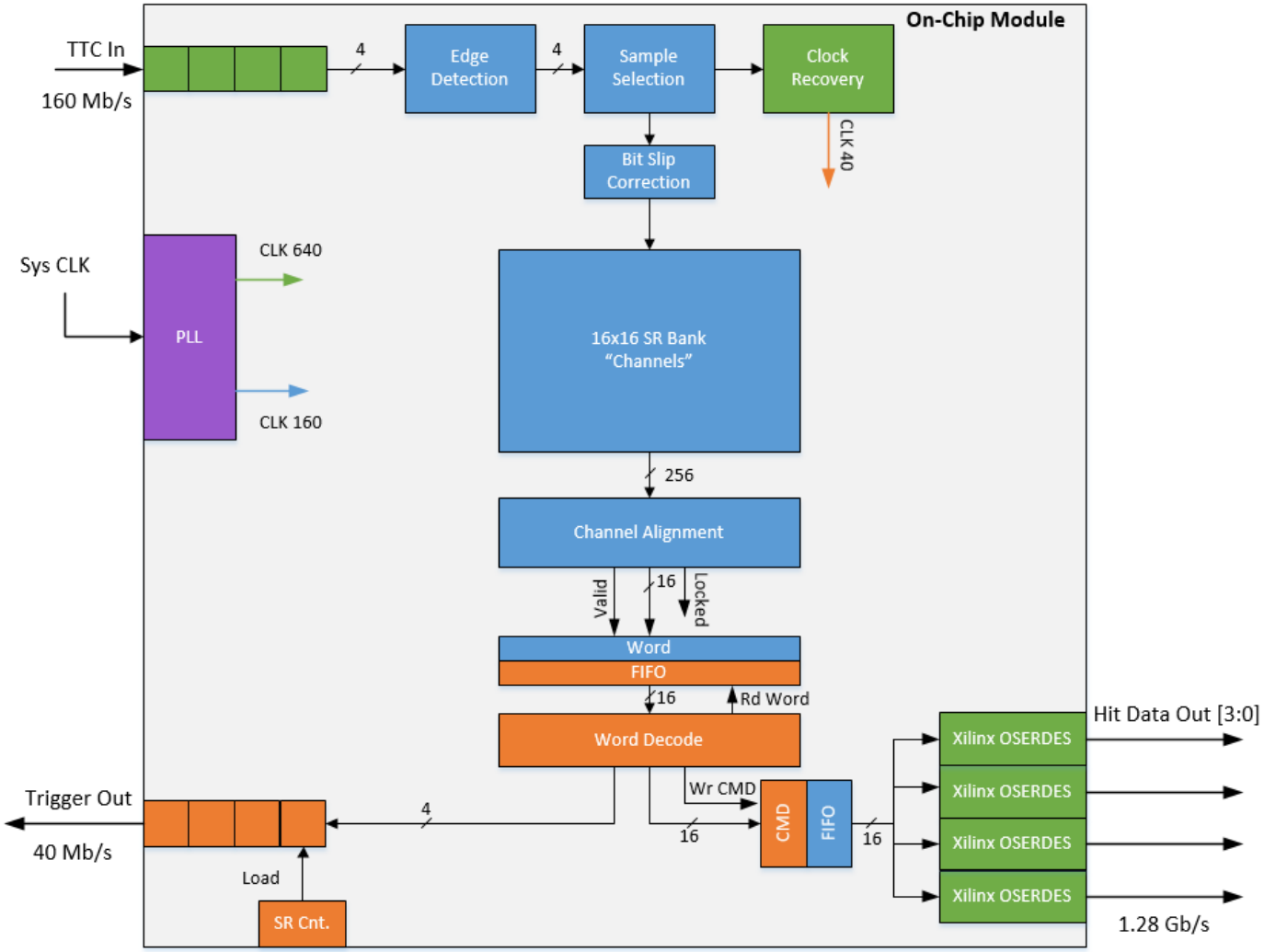
Feedback

- Feedback that would make this more useful to others?
- Currently working to integrate with the RCE readout and HSIO boards in Seattle.
  - Are there other readout systems that would be good to target as well?
- Other changes that would be useful to have in the emulator?

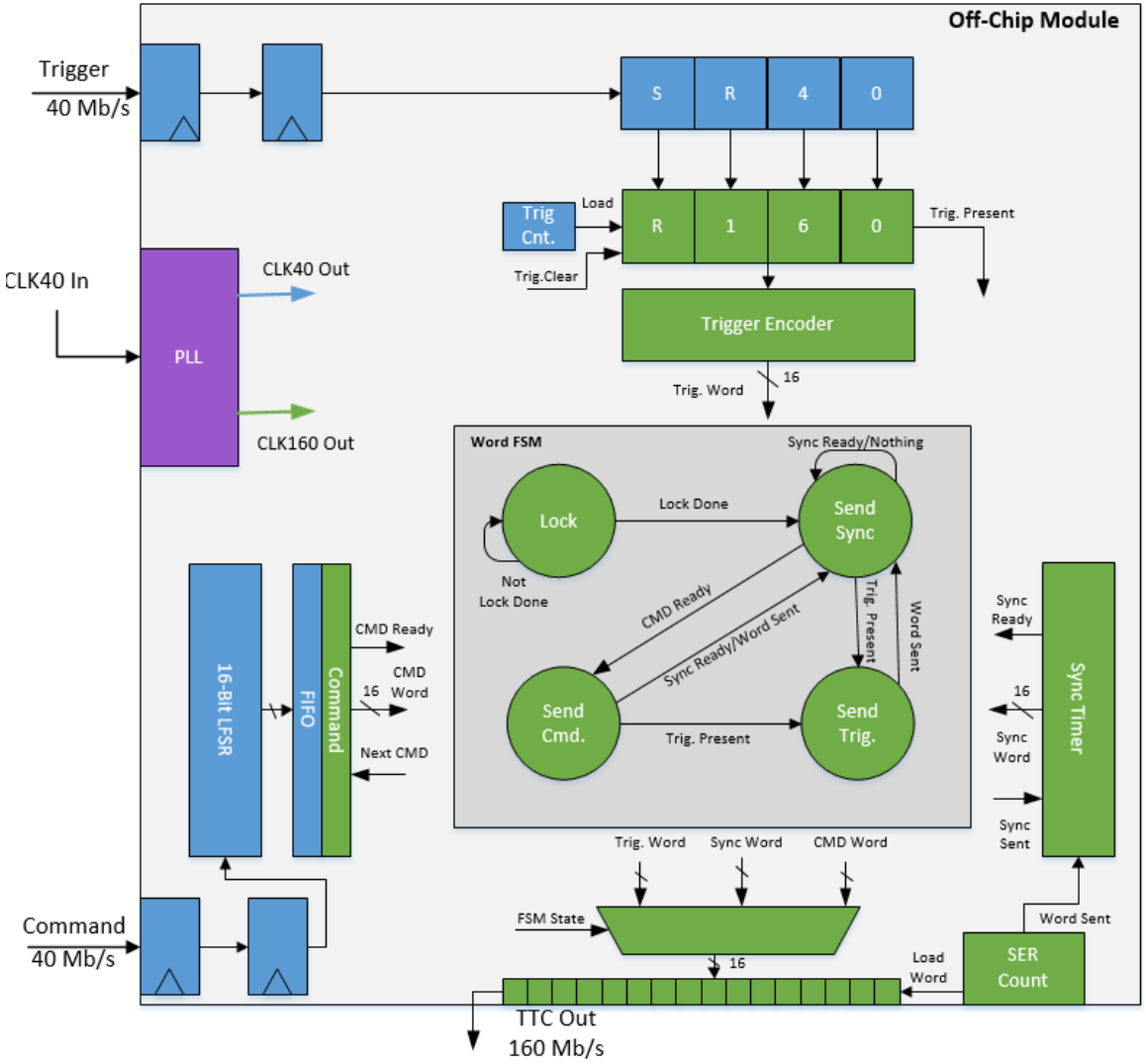
Thanks!

Backup Slides

Emulator System Diagram



"DAQ" Diagram


Off-Chip Module
Trigger
40 Mb/s
S
R
4
0
Trig Cnt.
Load
R
1
6
0
Trig. Present
Trig.Clear
Trigger Encoder
Trig. Word
16
CLK40 In
PLL
CLK40 Out
CLK160 Out
Word FSM
Sync Ready/Nothing
Lock
Lock Done
Send Sync
Not Lock Done
CMD Ready
Sync Ready/Word Sent
Trig. Present
Word Sent
Send Cmd.
Trig. Present
Send Trig.
16-Bit LFSR
FIFO
Command
CMD Ready
CMD Word
16
Next CMD
Sync Ready
16
Sync Word
Sync Sent
Sync Timer
Trig. Word
Sync Word
CMD Word
FSM State
16
Word Sent
Load Word
SER Count
Command
40 Mb/s
TTC Out
160 Mb/s