Lossless data compression for the HL-LHC pixel detector readout

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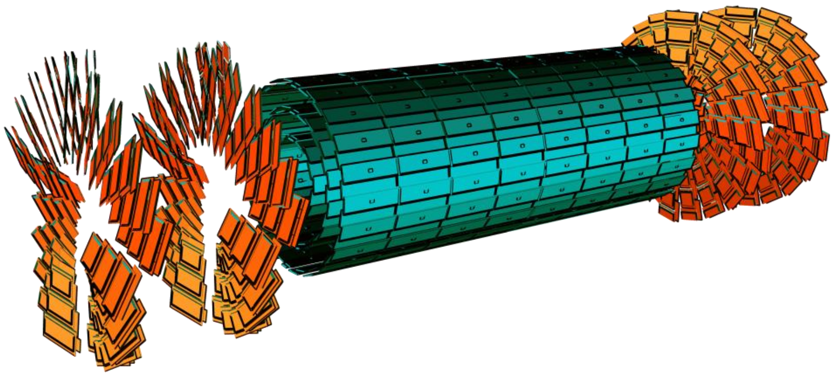
*Supported by the EU FP7-PEOPLE-2012-ITN project nr 317446, INFIERI, "Intelligent Fast Interconnected and Efficient Deices for Frontier Exploitation in Research and Industry"

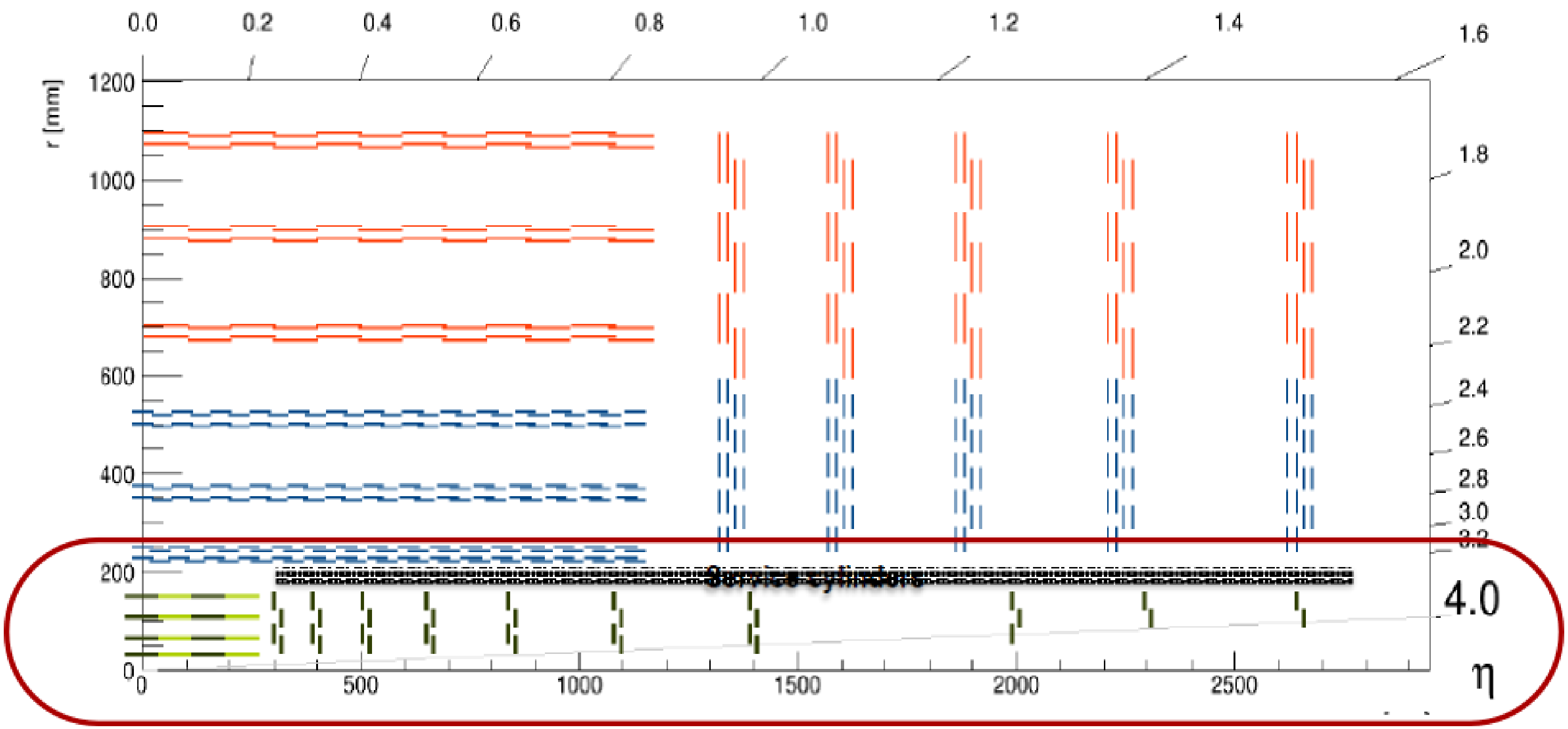
CMS pixel detector

- Close to the interaction point
- High flux of particles
- High amount of data
- Tight space



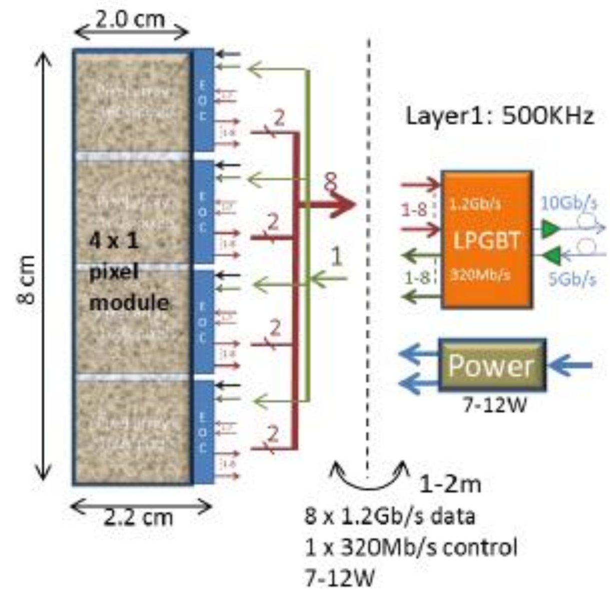
CMS tracker

- 4 Barrel layers
- 10 Forward disks



HL-LHC pixel detector readout chip

- Hit rate estimation for inner barrel layer at 140 Pile-Up is about 3 GHz/cm^2
- Expected high readout rate (~ 4.8 Gbits/s per chip for 1 MHz trigger rate)
- 2.4 Gbits/s max bandwidth per chip (2 E-links)



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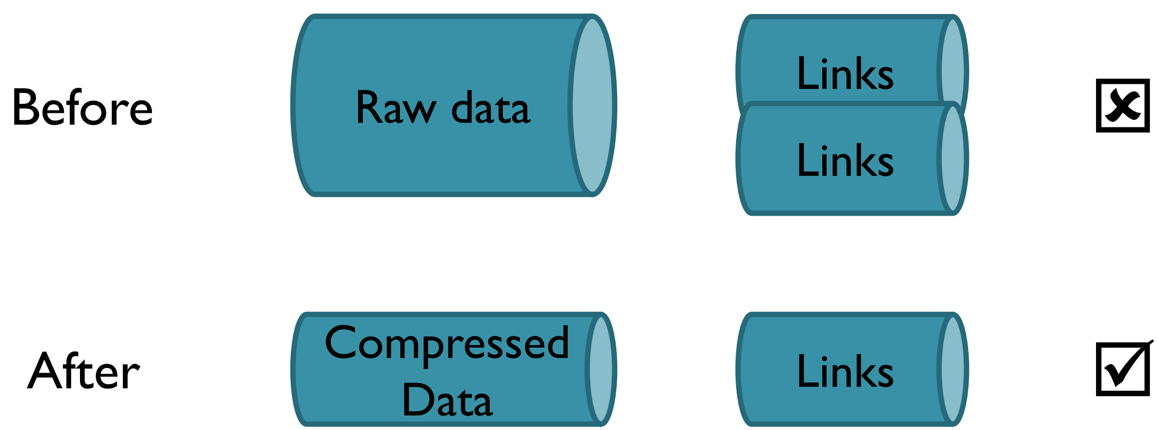
Goal

- An efficient transfer protocol should be developed to collect all measurements and ensure good detector performance
- Lossless compression with decreased output rate to reduce the usage of links
- On-chip compression – RD53 collaboration



Readout format

- Using readout format proposed in the draft of Phase 2 pixel system and read-out chip

Event header 32-bit → Event trailer 32-bit → Hit data …

Event header: BX-id, event ID, chip address, status

Event trailer: Event size, check sum, status/error flag,…

- Default hit data representation:
  - (30 bits/pixel)

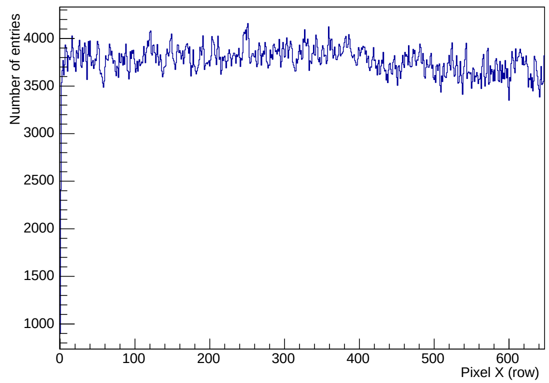
Pixel 1
24 bit Address
5 bit ADC
1 bit flag
→ *Pixel 2* … *Pixel N*

Compression scheme

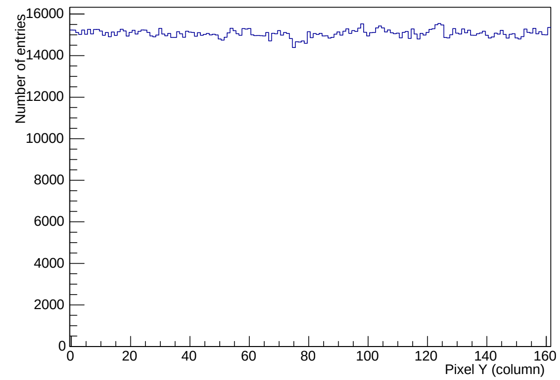
- Main domains
  - Data representation
    - How the data are accessed
  - Encoding
    - Actual data encoding

Characteristic Distributions

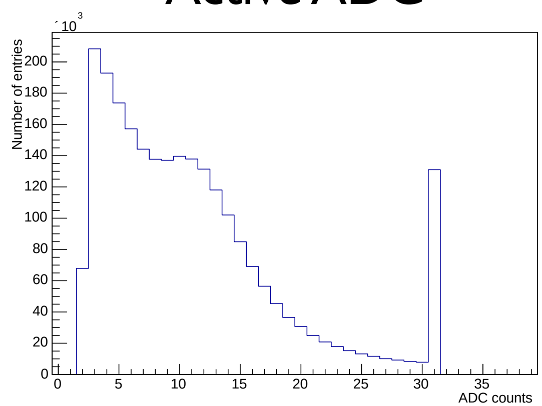
Pixel X



Pixel Y



Active ADC



Representations

- Group pixels in 2x2 pixel regions
  - Format: {PRaddr, ADC0, ADC1, ADC2, ADC3,}
  - Low compression
  - Very simple
- Delta representation
  - Calculate Δx and Δy for every active pixel
  - $\Delta x = x_n - x_{n-1}$, $\Delta y = y_n - y_{n-1}$
  - Good compression
  - Requires additional logic

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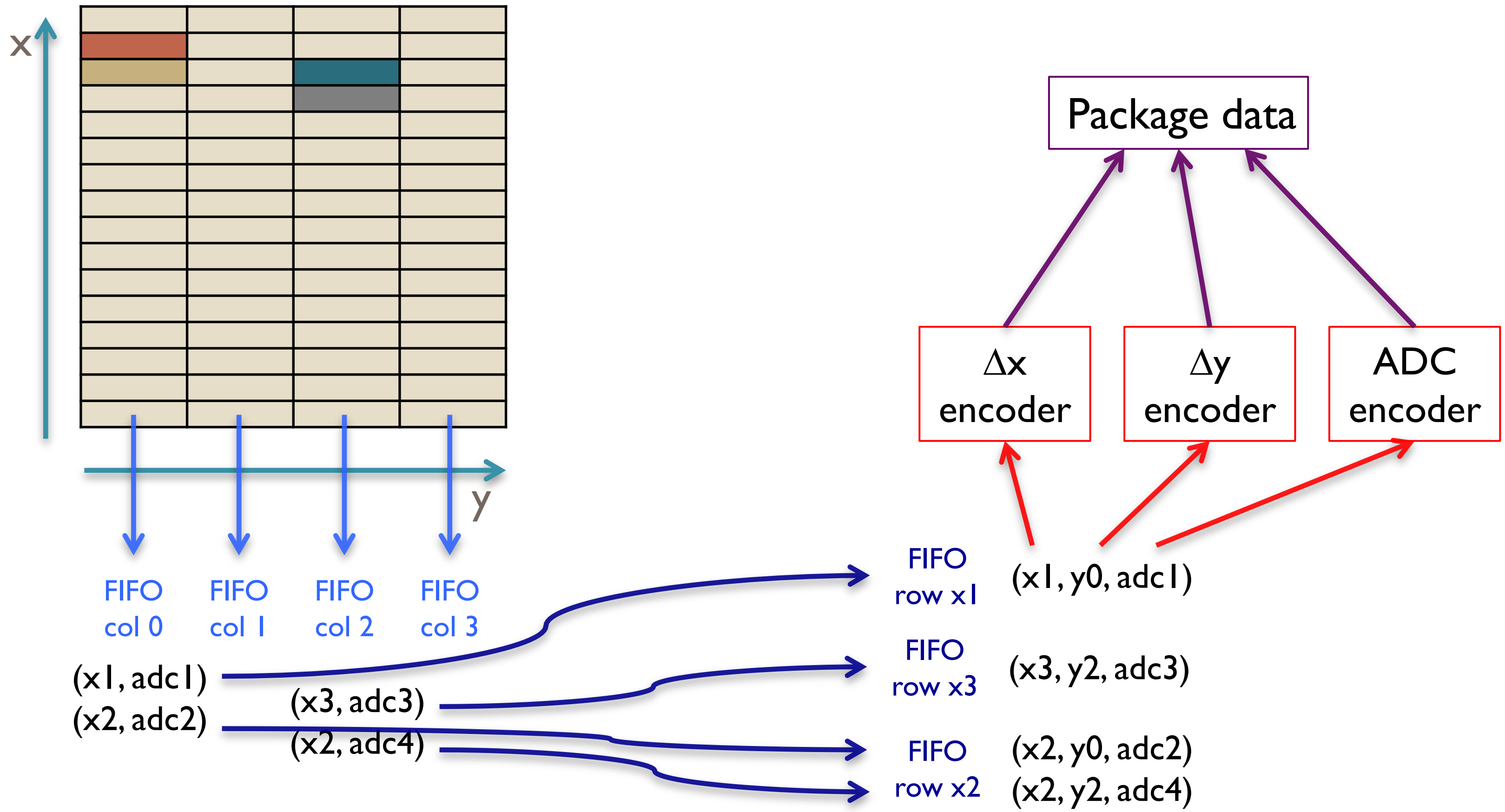
Delta representation (ordering by rows)

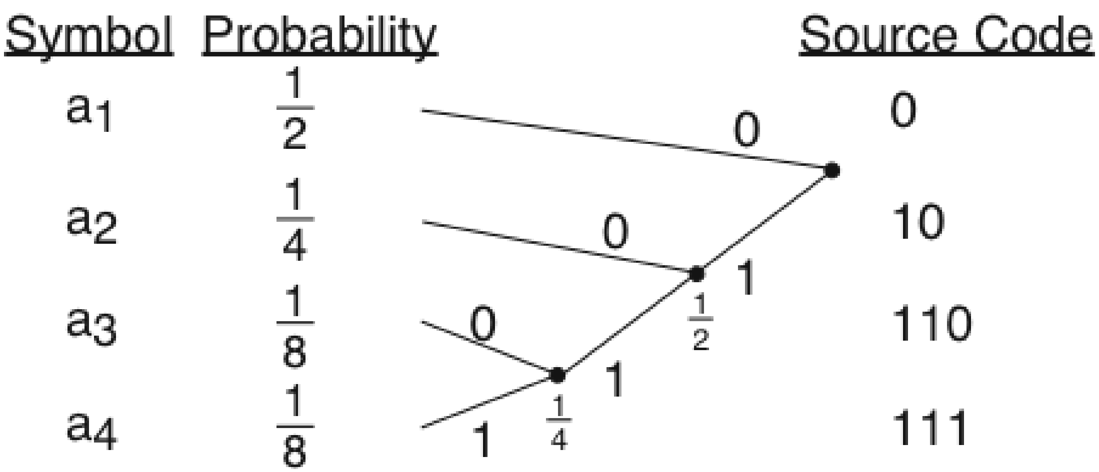


Encoder

- Simple compression technique
  - Reduced logic
  - Reduced need for power/area
  - Minimum computation time
- Huffman
  - Simple
  - Fast

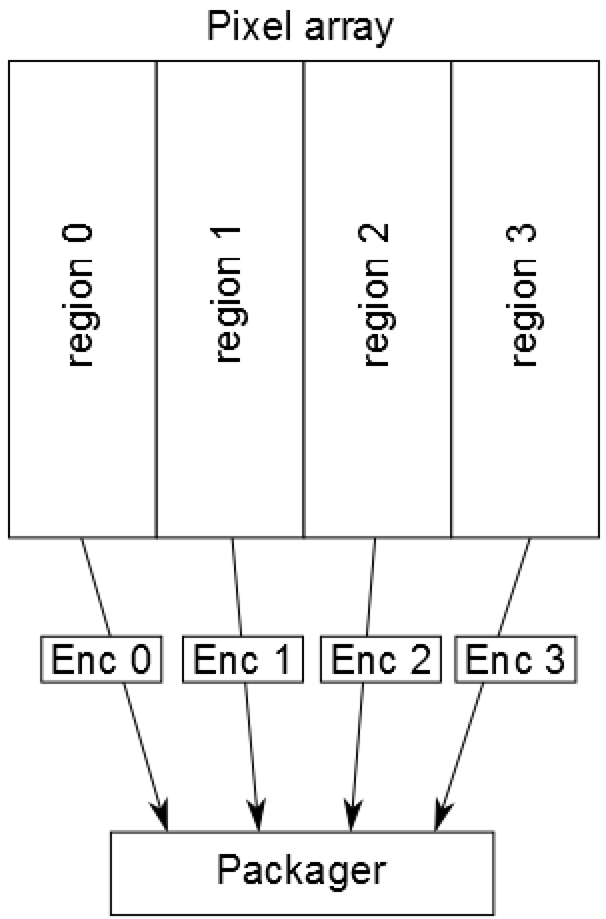
Huffman coding

- Prefix coding
- Assigns shorter codes for more probable symbols



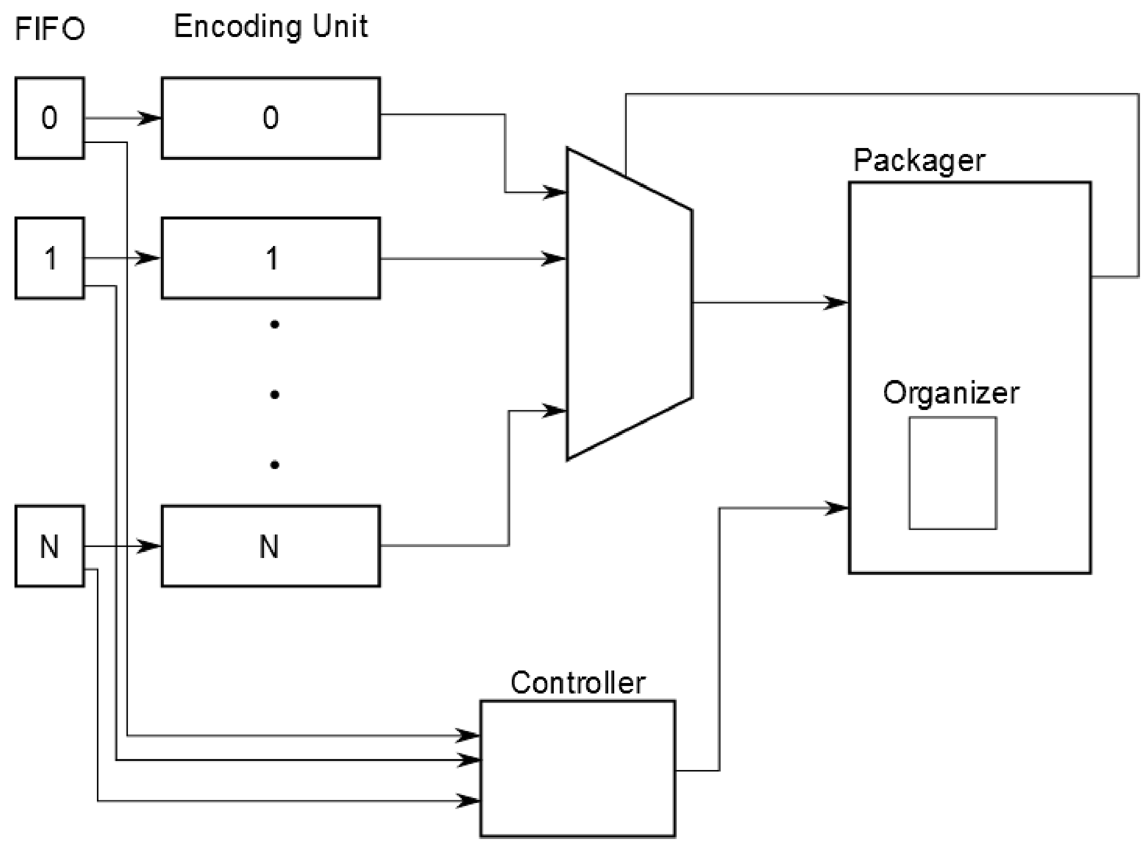
Data flow

- Timing requirements
  - 160 clk cycles available
- Huffman processes 1 symbol per clk
- Pixel array divided in regions
- Encode in parallel
- Merge data in packager



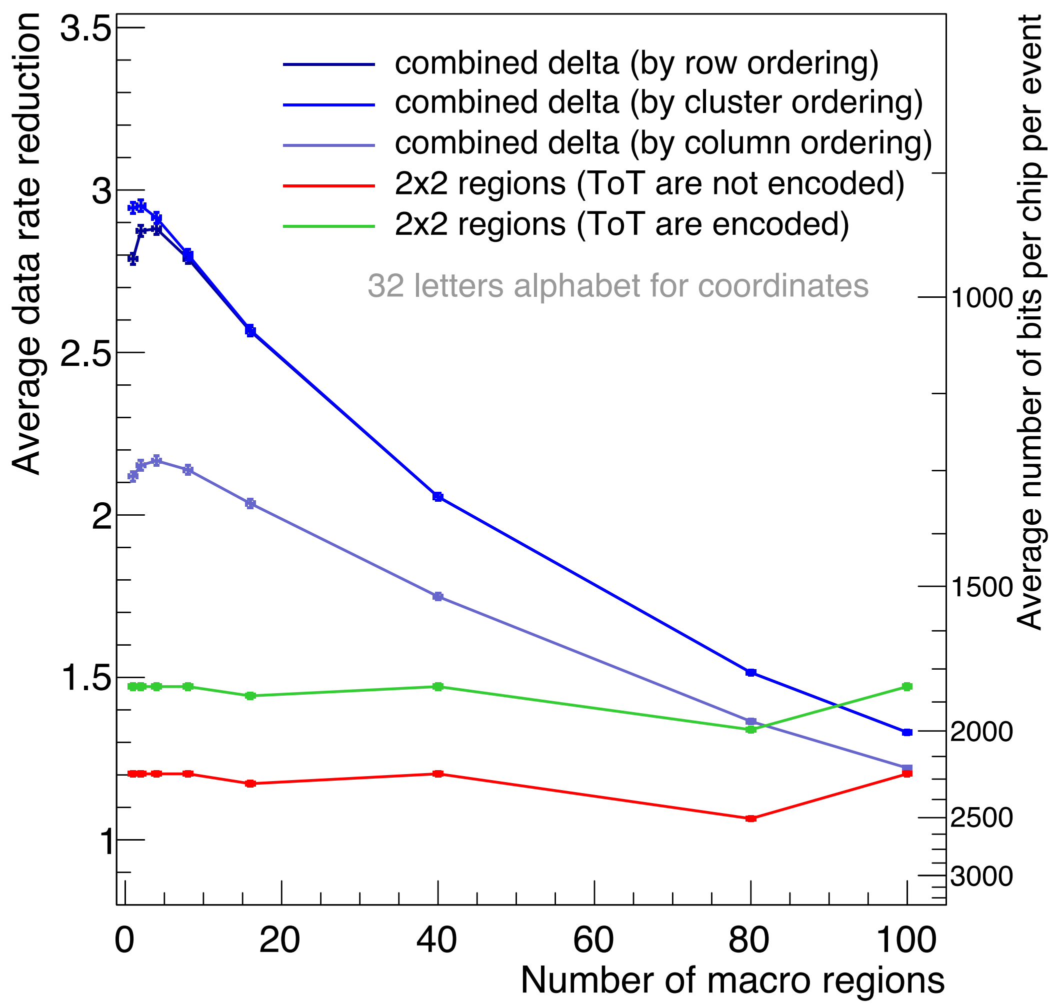
Compressor architecture

- N Encoding Units for N regions
  - encoder_adc
  - encoder_dx
  - encoder_dy
- Packager
  - Final packet
- Organizer
  - Organizes the data in to 32-bit words

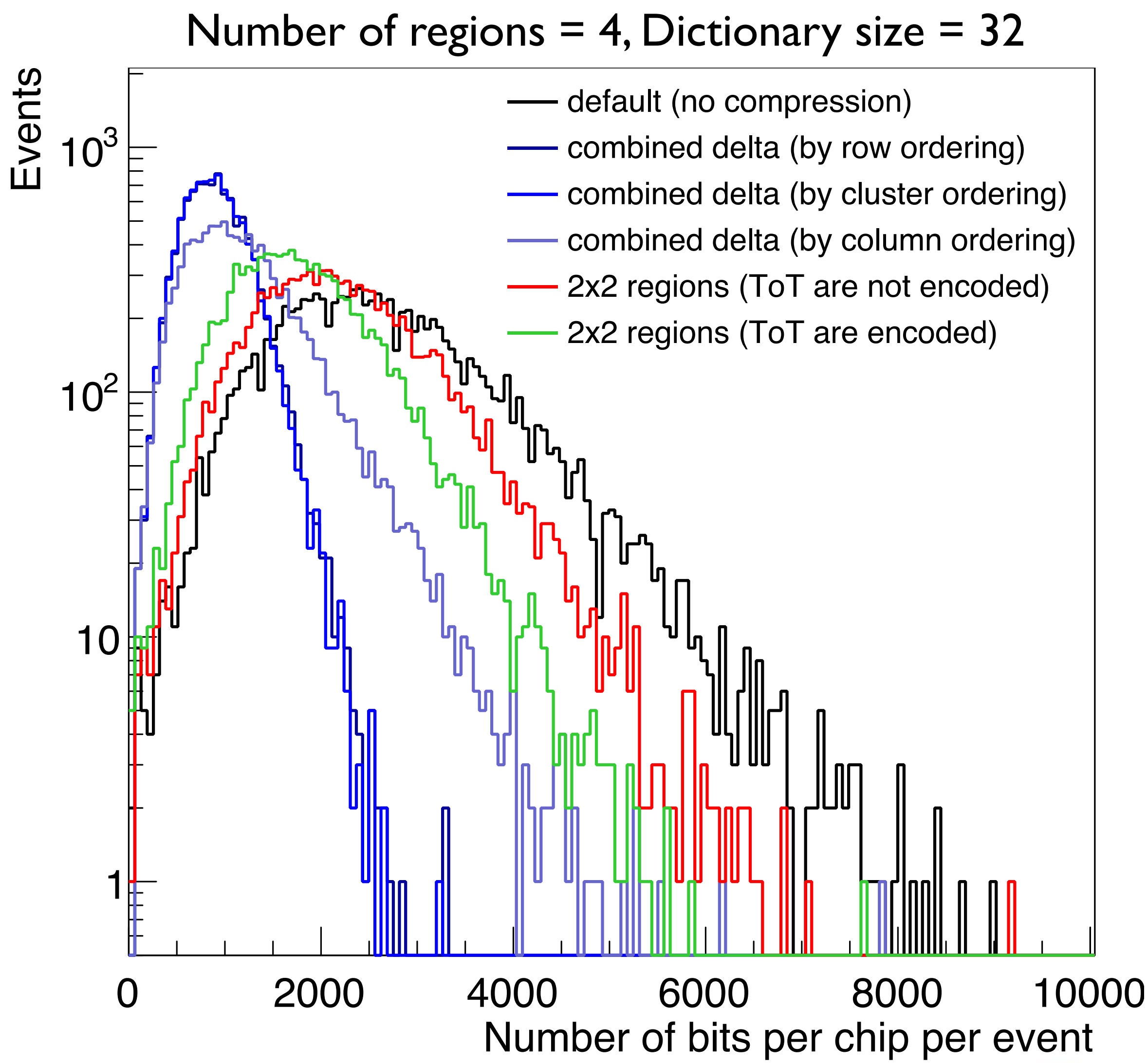


Compression performance

As a function of number of macro-regions



Compression performance



Synthesis results 65nm

- Compressor unit
  - Power ~1.93 mW (@160 MHz)
  - Area ~ 11000 um^2

Instance	Cells	Leakage Power (nW)	Dynamic Power (nW)	Total Power (nW)
Top_compressor	4410	3892.184	1933083.865	1936976.049

Instance	Cells	Cell Area	Net Area	Total Area
Top compressor	4410	10926	0	10926

Conclusions

- Compression ratio up to ~2.9 with Huffman coding depending on configuration
- Combine pixels in 2x2 regions for a simpler solution/implementation
  - ~1.2 without compressing ToT
  - ~1.5 with compressed ToT
- Optimize compression for each region (Barrel, Forward disks) to increase performance

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Thank you!!!