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Young Scientist Forum : Online track reconstruction using Kalman Filters on FPGAs

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The significant instantaneous luminosity planned at the High-Luminosity LHC will present a challenging environment for online track reconstruction.
Hardware acceleration of tracking algorithms on parallel architectures is an attractive solution to meeting latency restrictions in online systems.
Here we present an FPGA implementation of the Kalman Filter for fitting and cleaning tracks.
The implementation has been developed targeting a Xilinx Virtex 7 FPGA.
A High Level Synthesis language, MaxJ, was used to simplify the implementation of the algorithm compared to conventional FPGA programming techniques.
A single iteration latency of 210 ns is achieved at a clock frequency of 240 MHz.
Due to the small resource usage of the matrix maths, 36 independent Kalman Filter nodes operate in the chip.
Operation pipelining enables the processing of multiple data simultaneously within a node.
The implementation has a theoretical upper limit of 1 billion track fits per second for a 6 layer tracker.
At the data rate observed in high pile-up Monte Carlo data, with a preceding track finding stage, we fit 23 million tracks per second, with spare capacity.
Here we present the algorithm, its performance and applications, including at different levels of online reconstruction.

Author: SUMMERS, Sioni Paris (Imperial College (GB))

Presenter: SUMMERS, Sioni Paris (Imperial College (GB))

Track Classification: 9 : Real Time Pattern Recognition