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L1 track trigger for the CMS HL-LHC upgrade using AM chips + FPGA

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The increase of luminosity at HL-LHC will require the introduction of tracker information at Level-1 trigger system in CMS to maintain an acceptable trigger rate to select interesting events despite the one order of magnitude increase in the minimum bias interactions. To extract in the required latency the track information a dedicated hardware has to be used. We present the tests of a prototype system (Pattern Recognition Mezzanine) as core of pattern recognition and track fitting for the CMS experiment, combining the power of both Associative Memory custom ASIC and modern Field Programmable Gate Array (FPGA) devices. The mezzanine uses the latest available associative memory devices (AM06) and the most modern Xilinx Ultrascale FPGA. The results of the test for a complete tower comprising about 0.5 Million patterns will be presented using as input simulated events in the upgraded CMS detector. We will show the performances of the pattern matching, track finding and track fitting, along with the latency and processing time needed.

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