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Level 1 track trigger for the ATLAS High Luminosity Upgrade

Design and simulated performance

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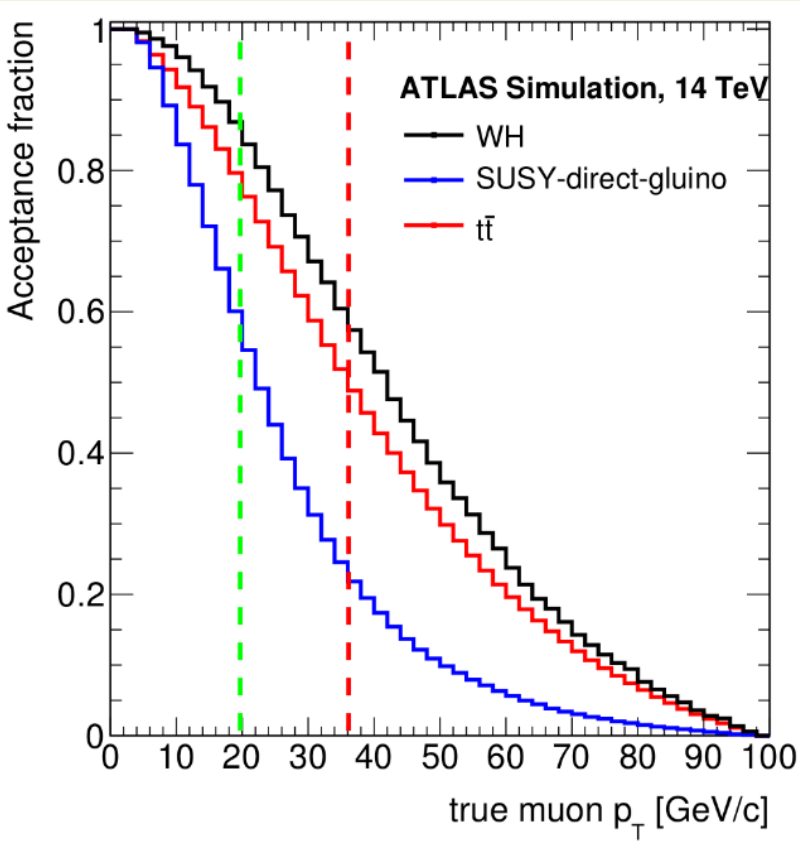
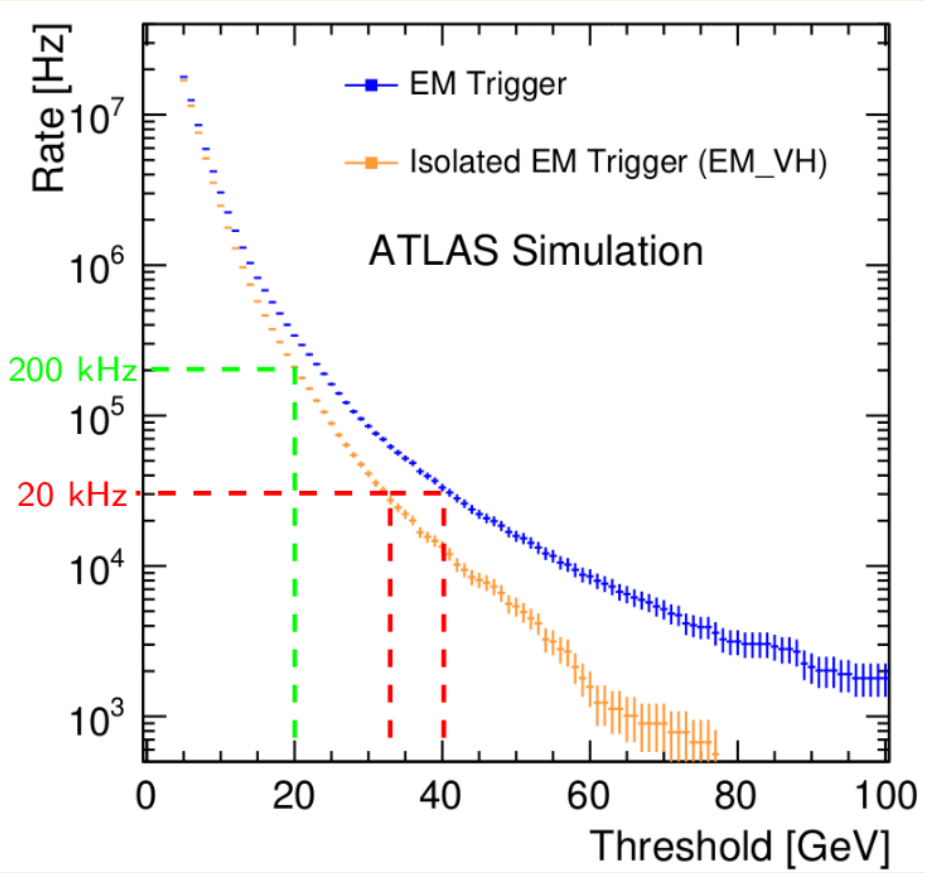
Introduction

- Track triggering for the ATLAS Phase-II upgrade (HL-LHC).
- 5-7 times increase in luminosity => need a trigger upgrade.
- Level 1 track: Fast regional tracking with near-offline resolution.
- Using the strip and pixel detectors of the Inner Tracker (ITk).
- Pattern matching in Associative Memory (AM) + track fit in FPGA.

Trigger requirements





=> If we are forced to increase the trigger p_T threshold to lower the rate, we will not benefit from the higher luminosity!

Further reading: LHCC-I-023, LoI for the Phase-II Upgrade

Trigger overview

- Level-0 (L0): 1st level muon and EM calorimeter trigger.
- Single level trigger with the option to evolve to a two-stage trigger:
  - L0-only: Run a L0 trigger *only*, with full detector readout. Run regional tracking as part of the Event Filter (EFTrack).
  - L0/L1 option: Move to using regional readout initiated by L0 *and* add regional track triggering as an extra level: L1Track.

Requirements for L1Track (1/2)

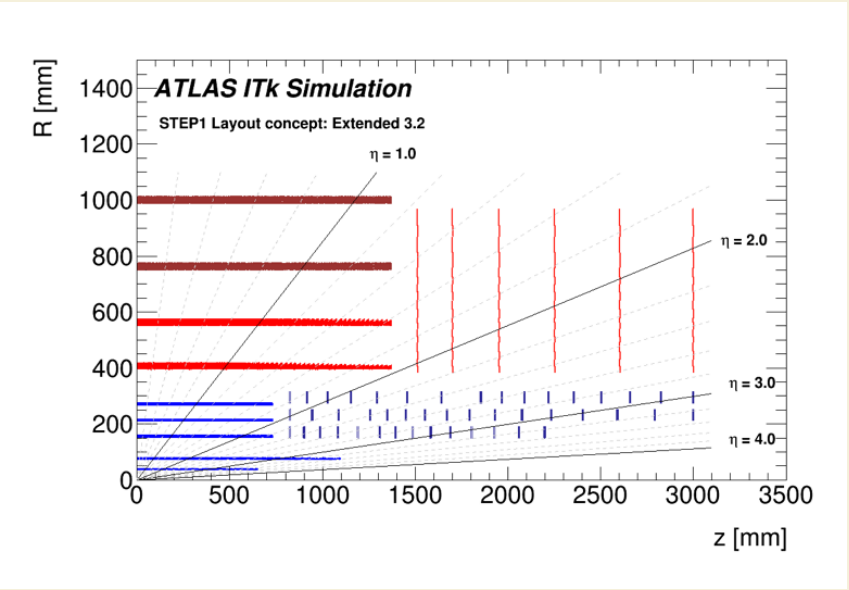
- Maintain 20 GeV c^{-1} thresholds for single leptons at the High Level Trigger.
- Reduce rate for hadronic triggers (jets and taus).
- Modest rate reduction of 3-5 between L0 and L1.
- Latency at L0 $<$ 10 µs limited by pixel readout.
- Latency at L1 $<$ 35 µs depending on L0 rate.

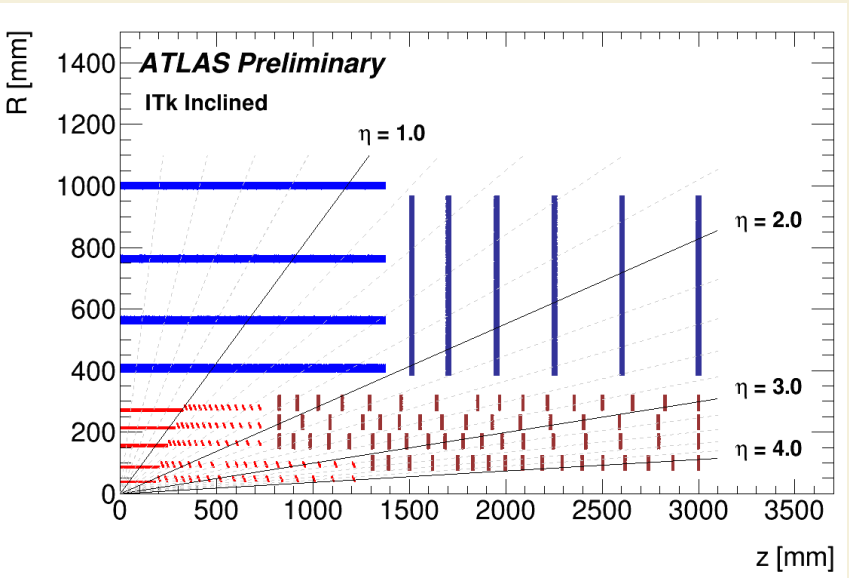
Requirements for L1Track (2/2)

- Reconstruction performance:
  - Track p_{T} down to
    - 4 GeV for L1Track
    - 2 GeV for EFTrack (these two trigger options explained later)
  - 95 % reconstruction efficiency compared to offline tracks.
  - Worst case z_0 resolution of 10 mm.
- Hardware:
  - Pattern matching constrained by AM size.
  - Track fitting constrained by FPGA size and speed.
  - ATLAS require that L1Track and FTK++ use the same hardware.

Inner tracker (ITk) layout

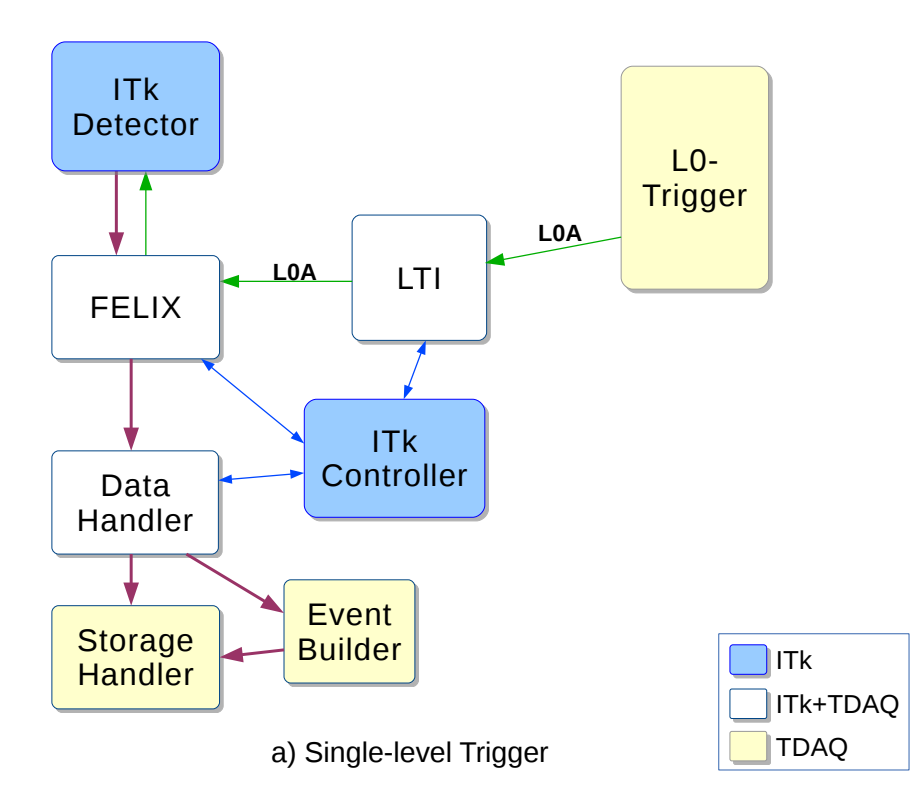
- Brand-new, all silicon.
- No self-seeded track trigger.
- Layout not finalized.
- Extended layout:
  - Strip: 4 barrel layers.
  - Pixel: 5 barrel layers.
  - Coverage to $|\eta| < 3.2$ to 4.0.
- Inclined layout:
  - Tilted pixel layers.
  - Coverage to $|\eta| < 4.0$.
- L1Track will use a mix of strip and pixel layers.
- The inner pixel layers have too high occupancy to be useful to L1Track.





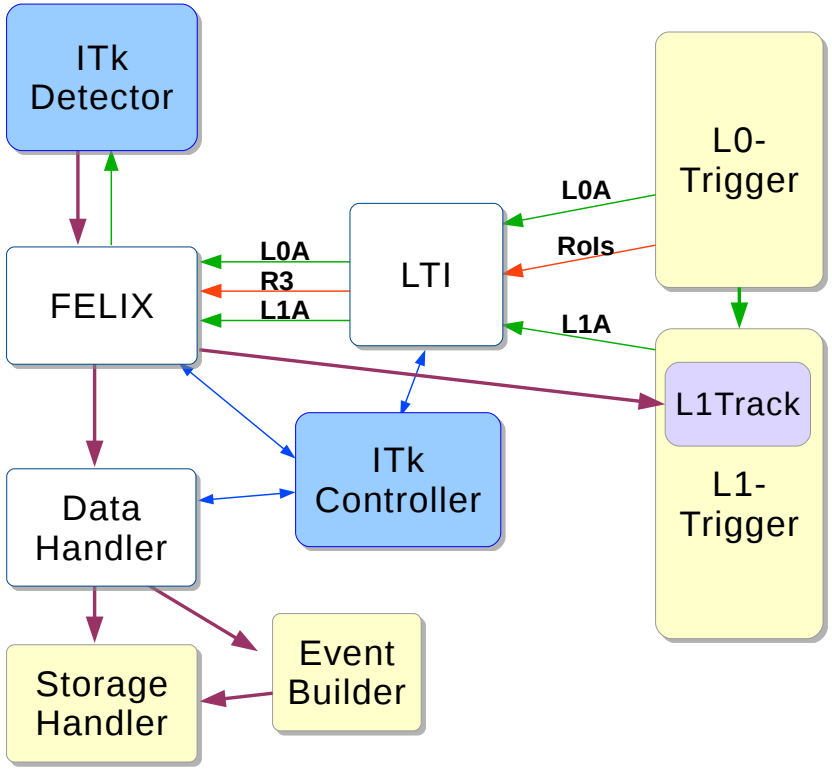
Baseline trigger architecture

- Single-level L0-only mode.
- Full detector readout at 1 MHz (max).
- “L1Track” will run as part of the Event Filter (EFTrack).



Evolved trigger architecture

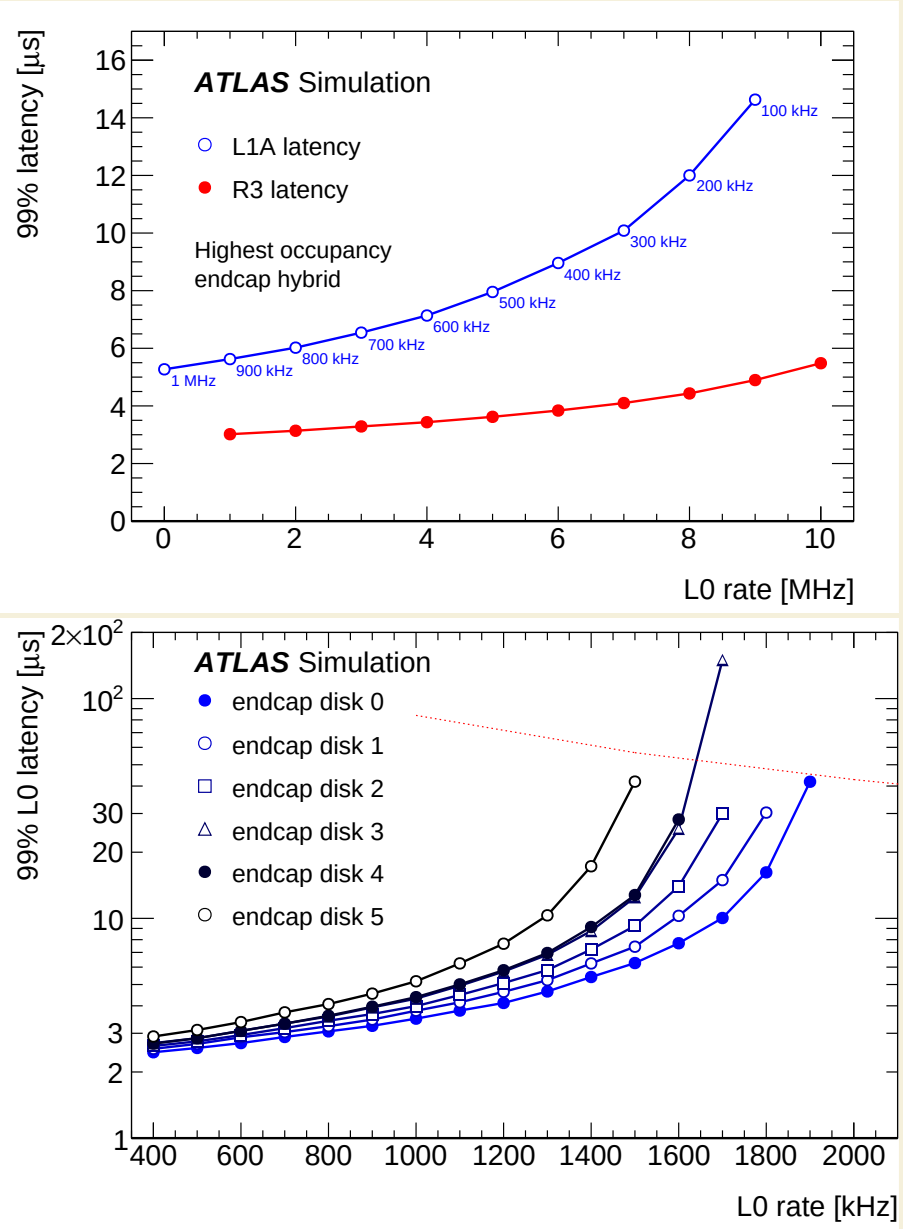
- Optional evolution to a two-level L0/L1 trigger mode.
- L0A initiates data storage in FE ASICs.
- R3 initiates regional readout ($< 10\,\%$) of the ITk Strip detector.
- L1A initiates readout of strips + outer pixels.
- 2-4 MHz L0 regional readout rate.
- 600-800 kHz L1A rate.



b) Two-level Trigger with L1Track Option

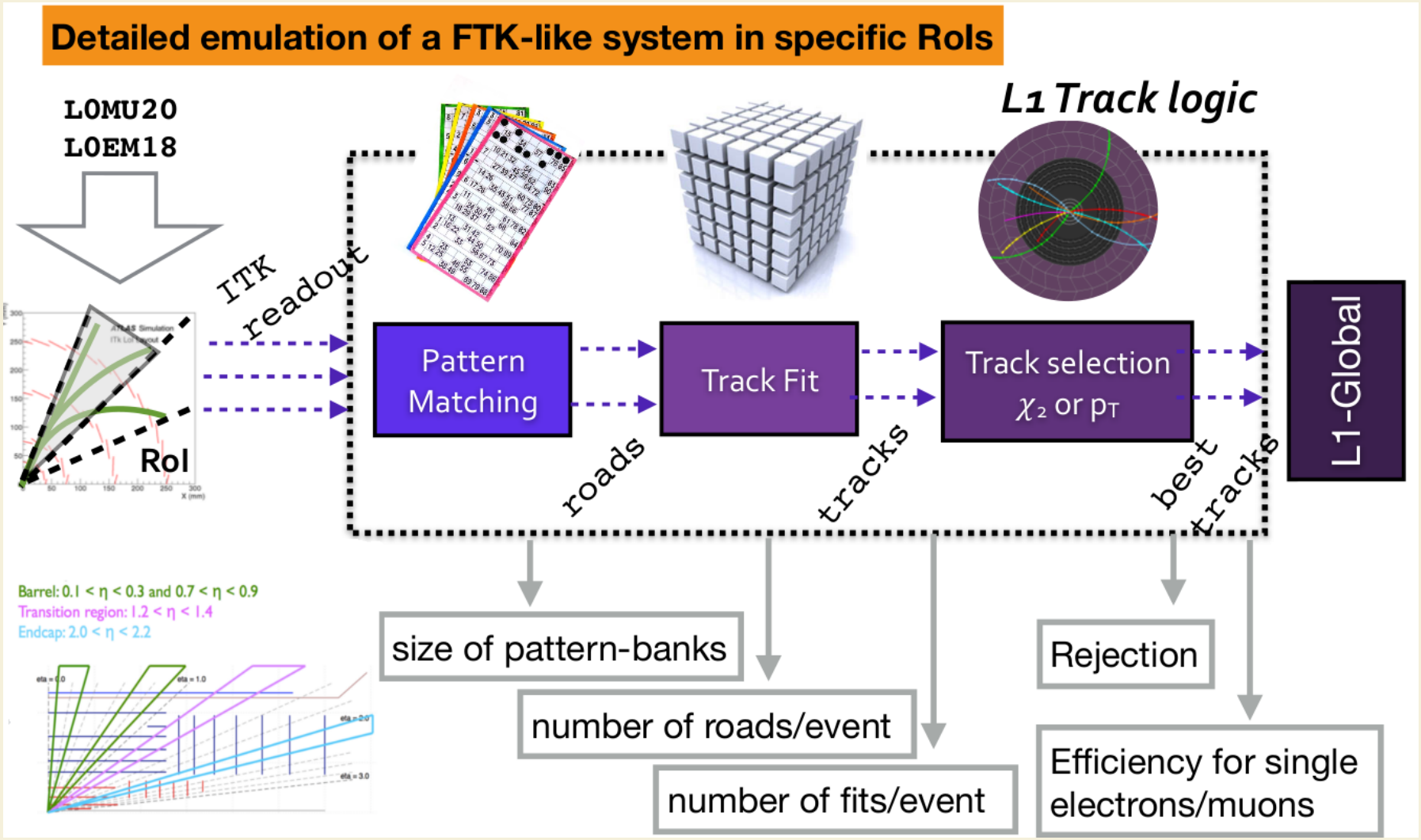
Readout latencies in the ITk strips

- Total rate fixed to 1 MHz.
- Showing worst case module.
- Regional Readout Request (R3) latency is well under control.
- => readout latency well under control.



Emulation of the L1Track trigger

- Emulation of the strip readout board in production + upcoming 1 MHz pixel readout.



Credit: Francesca Pastore

Associative Memory (AM)

Input pattern

1	0	1	0

	Data				Address	
	0	1	1	0	0	0
	0	1	1	1	0	1
Match	1	0	1	0	1	0
	1	0	0	1	1	1

Output

With *don't care bits* (X):

Input pattern

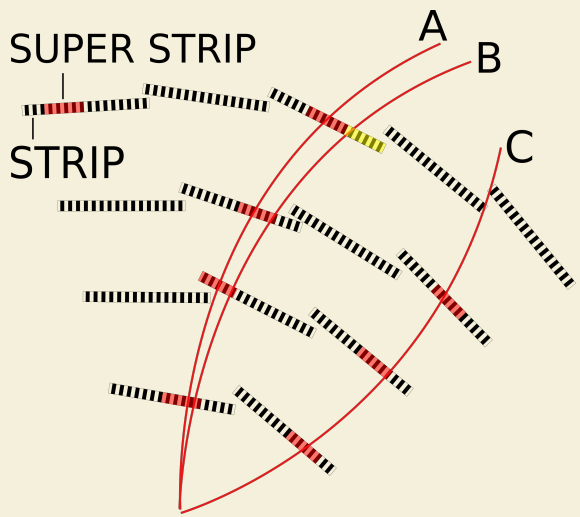
0	1	1	0

	Data				Address	
Match	0	1	1	X	0	0
	0	1	X	X	0	1
	1	0	1	0	1	0
	1	0	X	X	1	1

Output

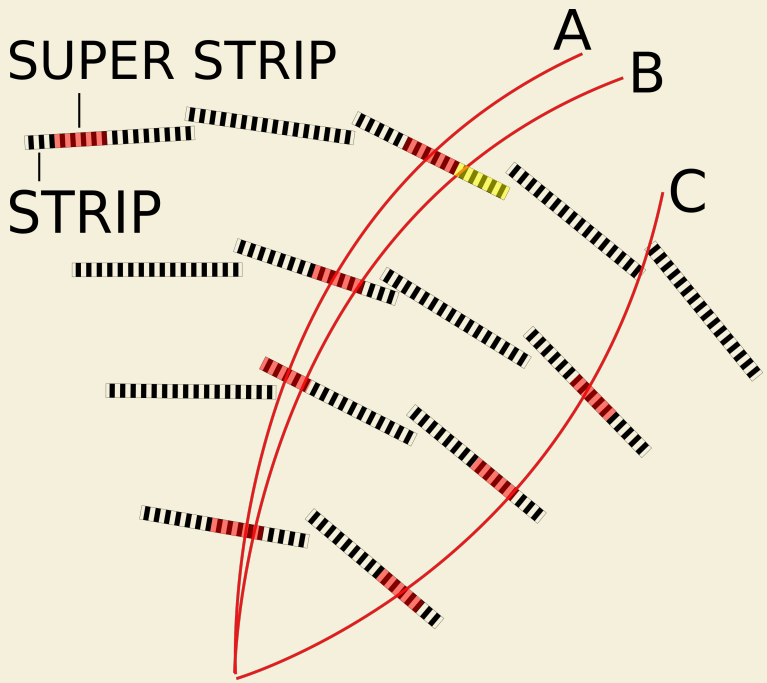
The pattern matching step

- Pixels and strips are combined to coarser-resolution *super-strips*.
- Using 8 detector layers of which 1 or 2 are outer pixel layers.
- AMs containing patterns of super-strip hits from simulated tracks.
- Outputs *roads* to the track fitting step.
- Each $\Delta\eta = 0.2$ by $\Delta\phi = 0.2$ RoI trained separately.
- Assuming we can have 1M patterns per RoI.
- Patterns trained using 30M single muons:
  - $4 < p_{\mathrm{T}} < 400\,\mathrm{GeV}$.
  - $|d_0| < 2\,\mathrm{mm}$.
  - Flat in $1/p_{\mathrm{T}}$, η, ϕ, z_0, and d_0.
- Evaluate using muons embedded in minimum bias of pile-up 200.



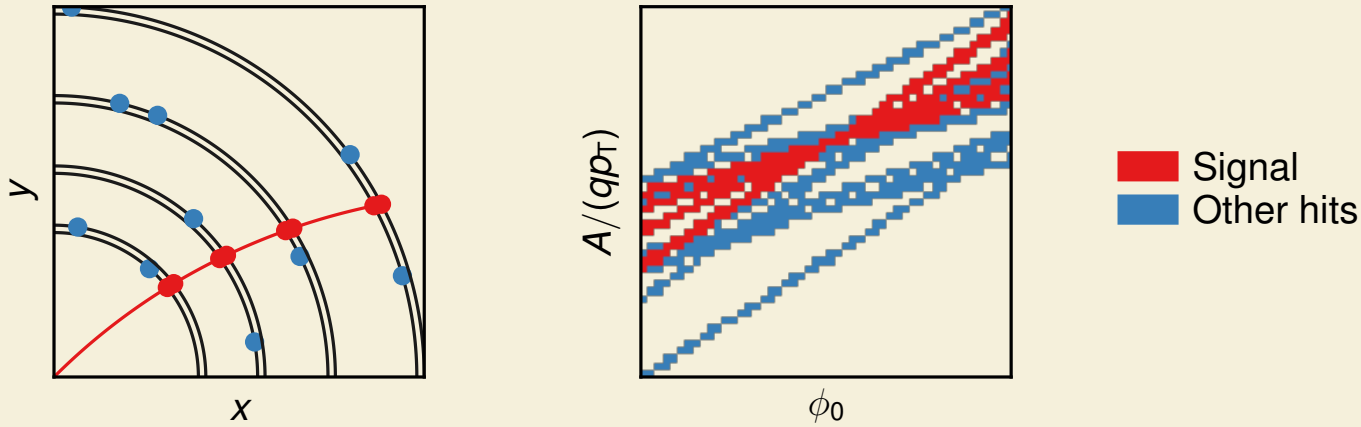
Optimization of pattern banks

- *Don't care bits* are used to combine similar patterns (track A and B)
- Tracks with a missing hit in one or two layers are handled using *wild card* layers (track C).
- During training the same patterns can appear more than once => order patterns according to occurrence and save top 1M.

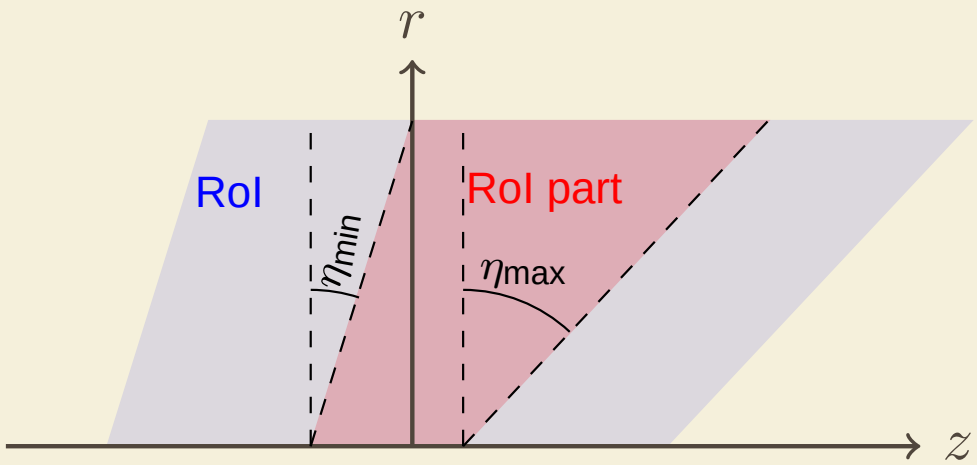


Alternative: Hough transform

- Alternative to pattern matching using AM. Parallel study.
- Parametrize curves and “accumulate” possible track parameters for all hits: $\frac{A}{qp_T} = \frac{\phi_0 - \varphi}{r}$.



- Reduce parameter space occupancy by splitting up z_0.



Hough transform performance

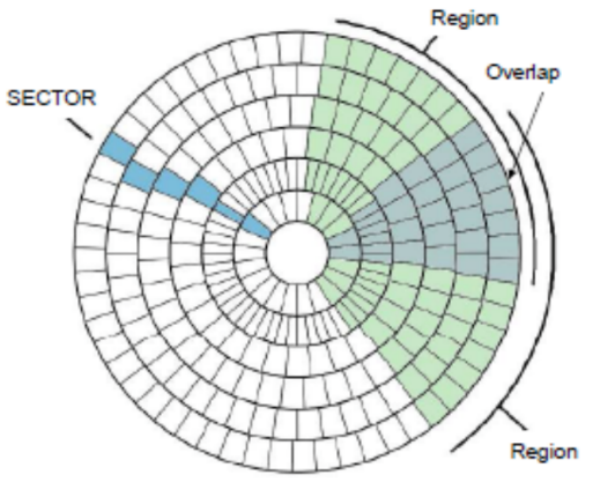
- 8 strip layers.
- Central barrel region of $0.1 < \eta < 0.3$ and $0.3 < \phi < 0.5$.
- Single muons embedded in minimum bias of pile-up 200.
- => Efficiency of 98.3 %.
- Can be implemented in an FPGA
- => eliminating need to transfer data from AM to FPGA.

Further reading: ATL-DAQ-PROC-2016-034

The track fitting step

- Uses full-resolution hits from roads selected by the pattern matching.
- Linear interpolation, track parameters stored in banks (LUT).
- Train using muons, like for the pattern matching.
- Derive the 5 track parameters (p_i) + χ^2 from cluster positions (x_j).
- Unique constants (C_{ij}, q_j) for each sector (a set of ITK modules).
- Can select tracks based on χ^2 and track parameters at a later stage.
- Has been shown to be robust against pile-up.
- Expect 2 fits/ns from the FPGA.

$$p_i = \sum_{j=1\ldots N} C_{ij}\, x_j + q_i$$



Matching + fitting performance

- For L1Track, i.e. L0/L1, $p_{\mathrm{T}} > 4\,\mathrm{GeV}$
- Central barrel region of $0.1 < \eta < 0.3$ and $0.3 < \phi < 0.5$.
- 8 detector layers.
- Efficiency and number of fits for single muons in pile-up 200:

Detector layers	Matching eff.	Fitting eff.	$< N_{\mathrm{fits}} >$
Strip only	99.4 %	99.5 %	114
Strip + 1 pixel	99.5 %	99.7 %	331

- Track parameter resolution:

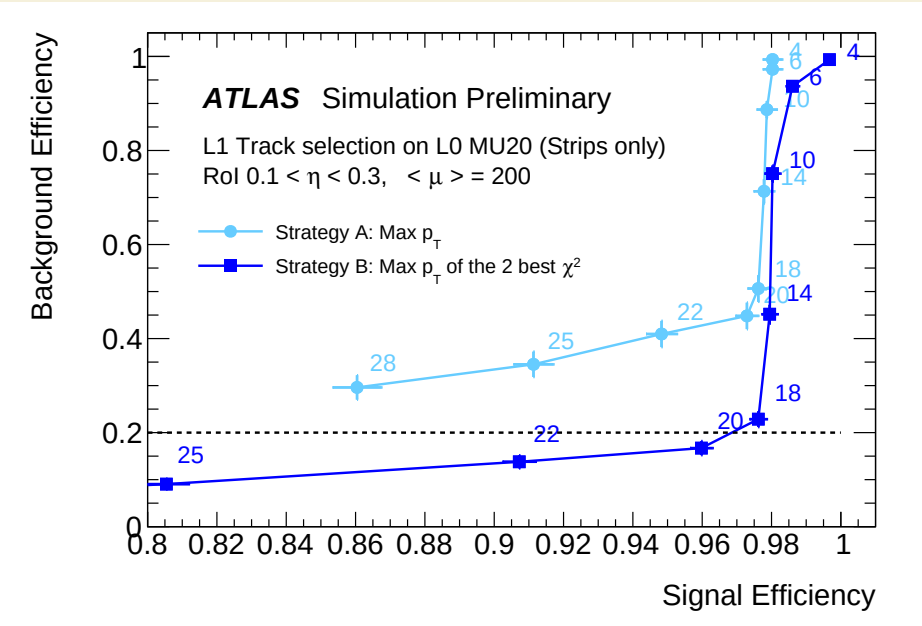
Layout	q/p_{T} (GeV^{-1})	ϕ (rad)	η	d_0 (mm)	z_0 (mm)
Strip only	0.003	0.001	0.002	0.3	1.7
Strip + 1 pixel	0.003	0.001	0.001	0.2	0.3

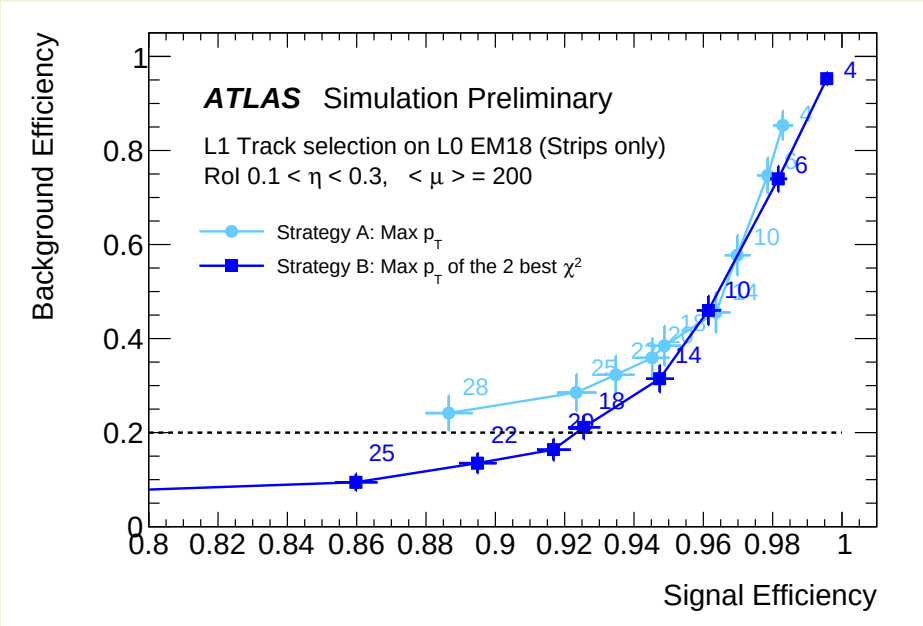
- No big differences between the proposed ITk layouts (extended vs. inclined).
- New results public soon.

Further reading: ATL-DAQ-PROC-2016-013

Track selection: performance

- Performance of matching + fitting + selection in central barrel region.
- Strips only.
- Two simplistic selection strategies studied:
  - Strategy A: Max p_T.
  - Strategy B: Max p_T of the 2 best χ^2.
- The markers in the figures show the p_T cut.



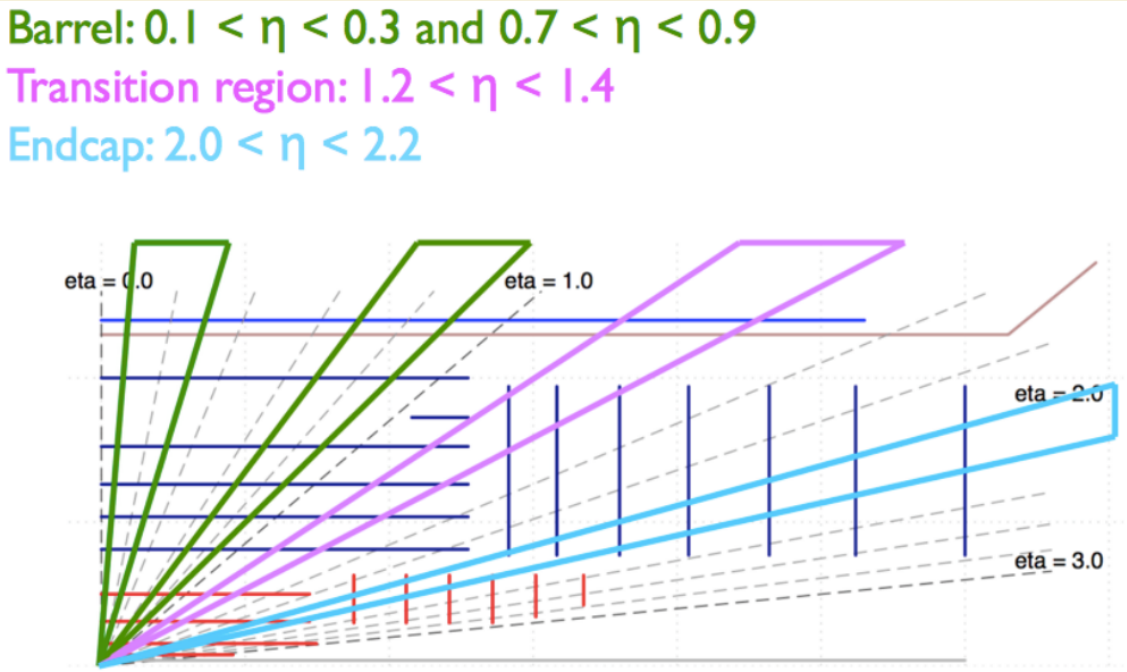


Summary

- Architecture:
  - L0-only: EFTrack at Event Filter.
  - L0/L1: L1Track pre-seeded by calo and muon trigger.
- L0 latency in both architectures $< 10\,\mu s$.
- L1Track:
  - L1Track seeded in RoIs passed by muon and calo triggers.
  - Pattern matching using AM, 99.5 % efficiency.
  - Alternative matching using Hough transform, 98.3 % efficiency.
  - Track fitting => track parameters + χ^2, 99.7 % efficiency.
  - Track selection using p_T and χ^2.
- Total efficiency after track selection:
  - Muon: Close to 98 % with 80 % background rejection.
  - Electron: Close to 93 % with 80 % background rejection.

Outlook

- We have studied pattern matching in several η regions for the new layouts. Results will soon be published.
- All studied regions reach approximately 99 % efficiency with 1M patterns.
- Fit studies are ongoing in these regions.
- Study alternative track selection strategies.



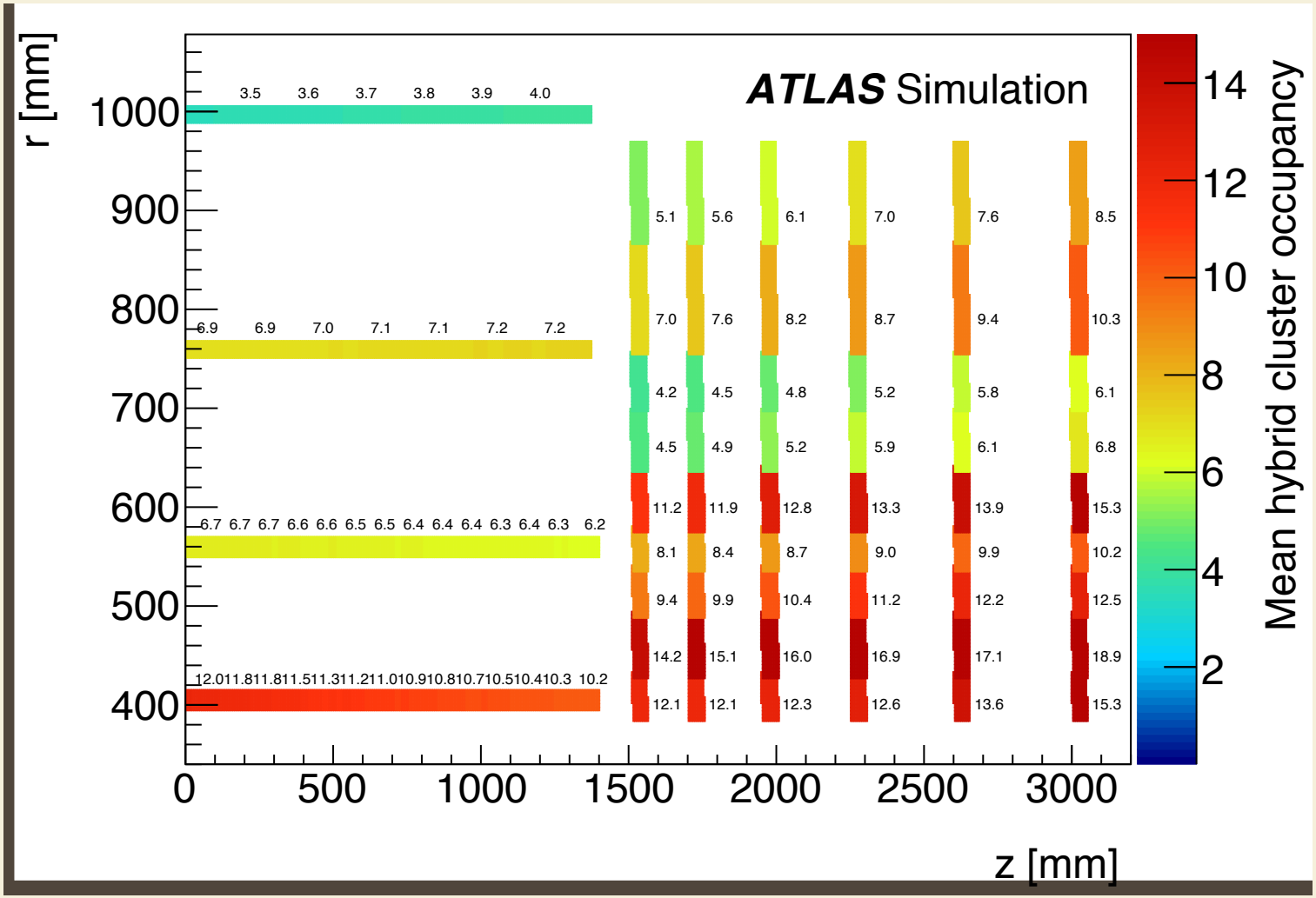
Backups

Comparison of Hough and AM

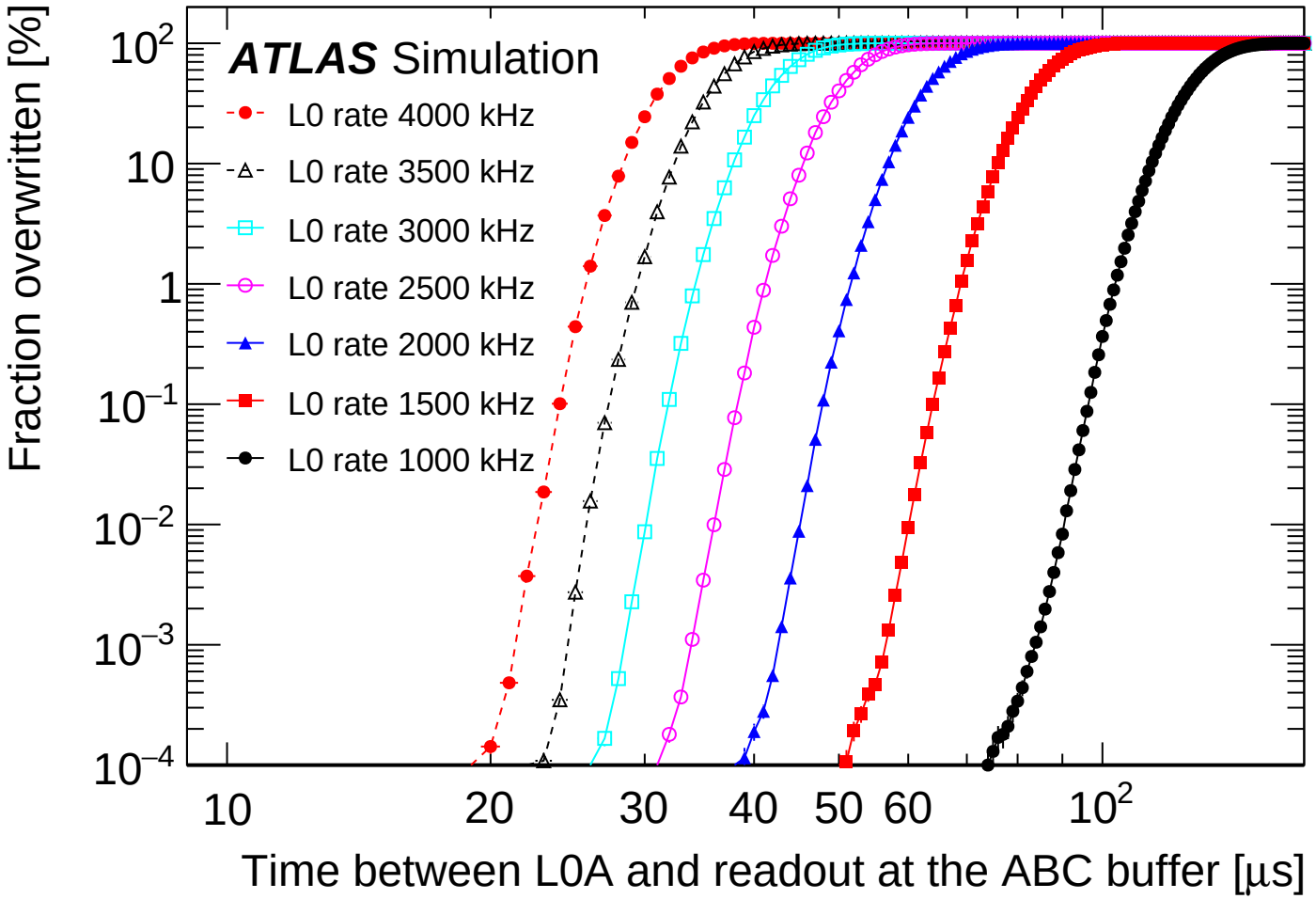
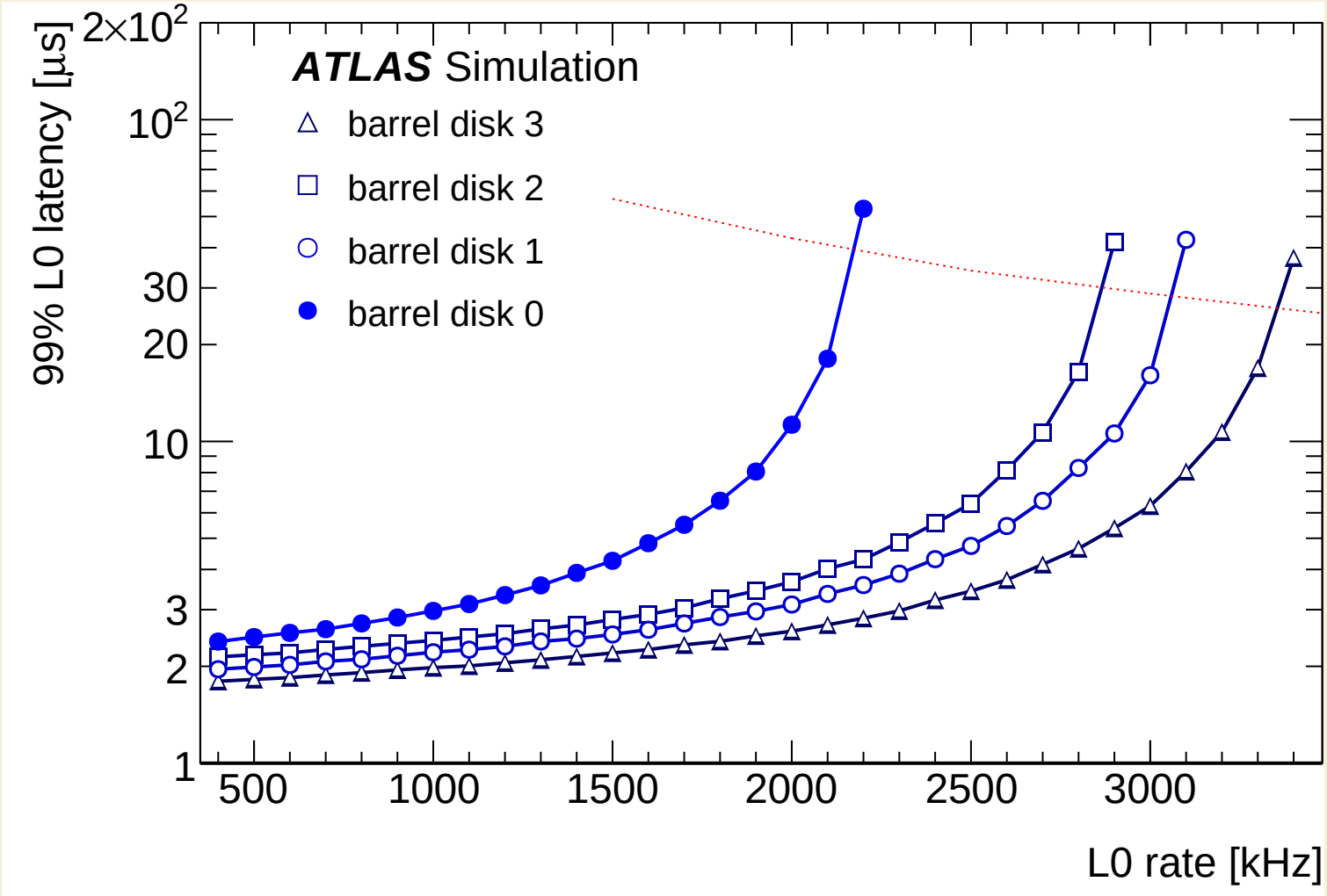
	Efficiency		Number of fits	
Sample	Hough	AM	Hough	AM
Min. bias	-	-	344	170
Muon	98.3 %	99.4 %	2	11

Further reading: ATL-DAQ-PROC-2016-034

Strip occupancy



Strip buffer overwrite



Strip barrel buffer overwrite