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Young Scientist Forum : High precision timing with HVCMOS MAPS Censors

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There is an increasing demand for precision time measurement in particle physics experiments, to reject pile-up as efficiently as possible. This translates into projects of precision timing tracker/preshower detectors at LHC experiments, in the frame of high luminosity upgrades (Phase 2 HL-LHC). There is little doubt that these techniques, if they can be used successfully at HL-LHC, will enter the arsenal of standard instrumentation for high occupancy environments like the one expected at FCC-hh.

Operating the LHC with more than 200 collisions per crossing of protons bunches, as it is foreseen from 2025 onward (HL-LHC phase), will greatly complicate the analysis, particularly in the forward regions, where it will be very difficult to link the tracks with the primary vertex (associated with the only interesting collision) and thus to prevent the formation of fake jets created by the random stacking (or pile-up) of tracks from several secondary vertices. A solution proposed to fight against this pile-up effect in the forward regions (pseudo-rapidity greater than 2.4) is to measure very accurately the time of arrival of the particles just before they enter the endcap calorimeter. This allows to reject by the time of flight technique the tracks associated with secondary vertices spread longitudinally over a distance of about 20 cm at the centre of the detector. A time resolution of a few tens of ps with a spatial granularity better than a few mm will be needed to obtain a fake jet rejection rate that is acceptable for physics analyses. Such performances should be obtained with a detector capable of withstanding the very important radiation levels (similar to the levels the outermost layers of the tracker will have to survive) expected in this part of the detector.

The main characteristic of the HV-HR CMOS monolithic technology is that it enables the integration in a single IC of the detection part (polarized diode) together with the needed stages of the front-end electronics for signal treatment and data sparsification. HVCMOS silicon sensors allow the application of a very strong electrical field in the depleted zone of the charge collection diode. This has several advantages. It opens the possibility to have a very large depleted region, which enables to reach a detection efficiency very close to 100% for a single particle, with good signal to noise ratio, enabling good time measurements without in-situ amplification of the deposited charge. Another advantage of HVCMOS technologies is its low cost, since these technologies are widely used in the automotive industry, where the cost has been pushed down by the high production volumes. This also implies that going from a small demonstrator to a full scale detector should in principle be easy, once the demonstrator performance is validated.

Simulation studies based on the HV-HR CMOS LFOUNDRIY 150 nm technology design kit have shown that a resolution of the order of 50 to 80 ps per MIP impact point can in principle be reached for MAPS pixels sensor of 1 mm pitch. We will present here the simulation results of the performance, and the architecture of a demonstrator chip, featuring a few rows and columns of individual pixels. Each pixel is equipped with a fast preamplifier, discriminator, and ancillary electronics to identify the position of the pixel hit, DACs to configure the discriminator, plus an injection chain to calibrate in-situ the performance of the readout electronics. At the time of the workshop, the chip will hopefully be in final submission stages.

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