Silicon tracking at CLIC, current overview and technology prospects

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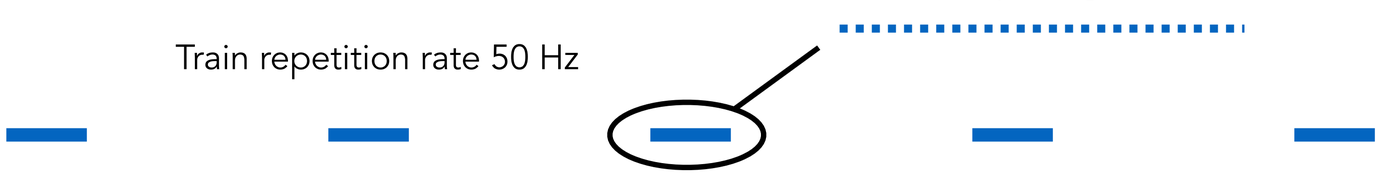
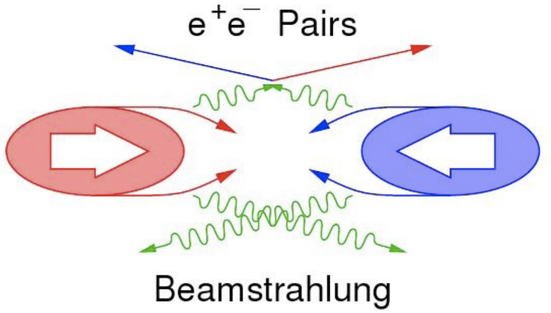
on behalf of the CLICdp collaboration

CLIC environment

- The CLIC environment has a great influence on the detector design
  - Bunch trains consisting of **312 bunches** (156 ns length) collide at **50 Hz**, large period of inactivity
  - Typically only 1 hard interaction per bunch train

- However…
  - High bunch density leads to beam-beam interactions, producing e^+e^- pairs and $\gamma\gamma$ => hadron backgrounds
  - Significantly lower radiation levels than for hadron colliders, no need to operate cold



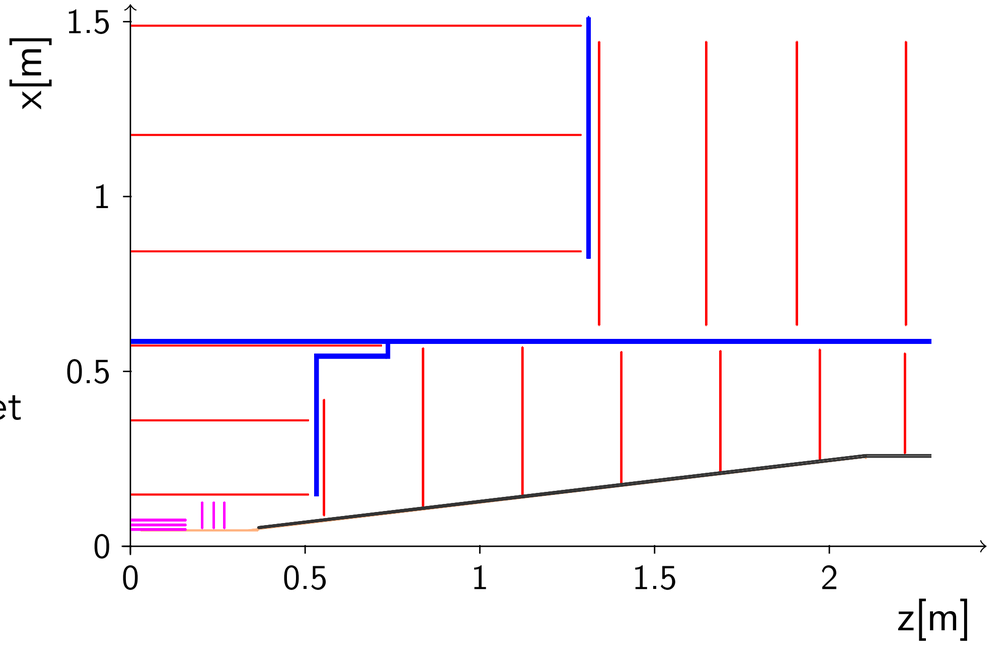


Overview of the tracking system

- CLIC detector is envisaged to contain all-silicon tracking detectors, with a vertexing detector and inner + outer trackers
  - Pixellated vertex detector close to the interaction point, inner radius set by background levels
  - Large tracking volume with short strips/long pixels

- Some common requirements for all silicon detectors
  - Fine time-slicing of 10 ns to reduce beam-induced backgrounds
  - High granularity to keep occupancies below a few %
  - Low material budget

- Overall size set by momentum resolution, with 4 T solenoid magnet

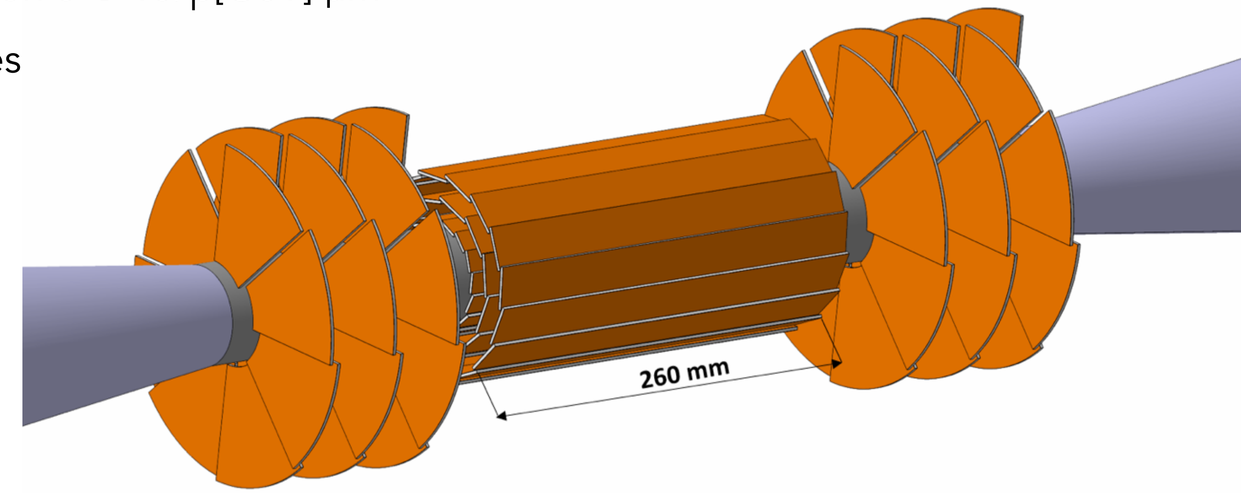


Vertex detector

- The vertex detector for CLIC has to be extremely low mass, 0.2 % X_0 per detection layer
  - Remove cooling pipes, replace with *forced air flow* => limit power consumption (power pulsing)
  - Arrangement of the detector into *double layers*, to allow sharing of support structure

- The current design has a radiation length of 0.4 % X_0 per double layer, with demanding performance requirements
  - A single hit resolution of ~3 μm, for transverse IP resolution $5 \oplus 15/p[\text{GeV}]$ μm
  - Fast signal generation and time-stamping into 10 ns slices
  - Low power consumption of 50 mW / cm^2

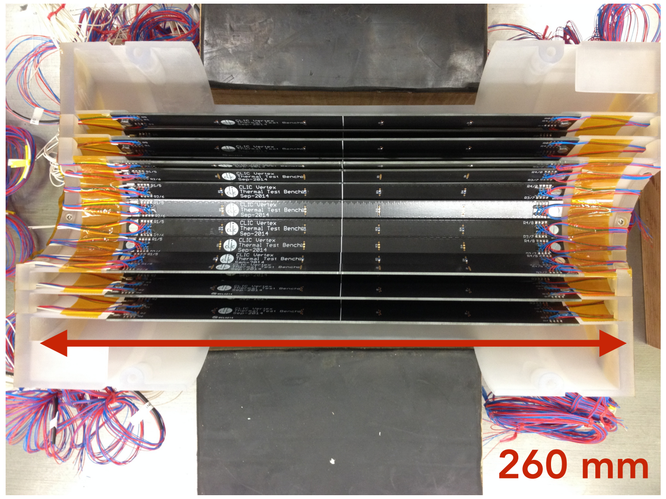
- Current technology baseline **hybrid pixel detector**
  - Pixel size of 25 μm × 25 μm
  - ASIC thickness of 50 μm and sensor thickness of 50 μm

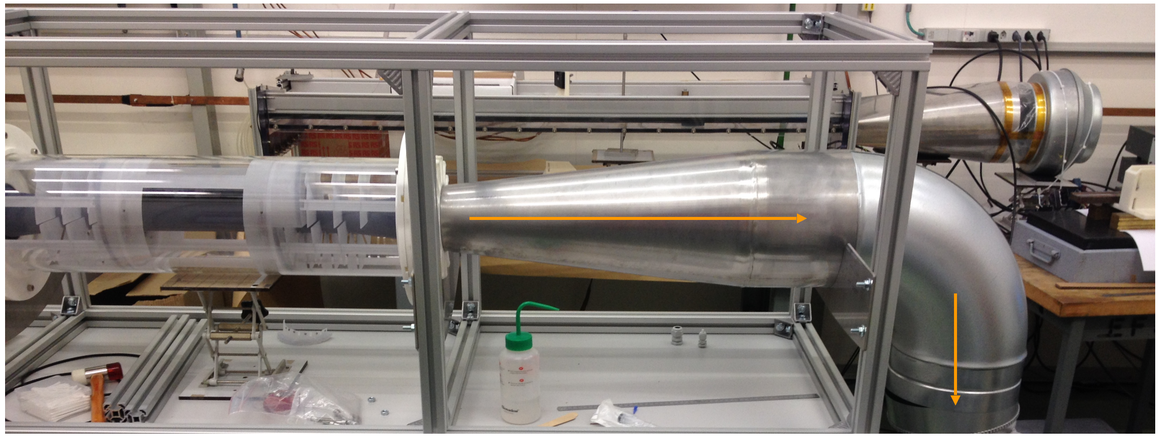


Vertex detector layout

- Main steps have been to prove the air cooling option using realistic power consumption numbers
  - Finite element calculations of the proposed layout
  - Thermal mockup constructed to demonstrate cooling and compare to simulation (similar to STAR)

- Mockup shows air cooling works with power budget of 50 mW / cm^2



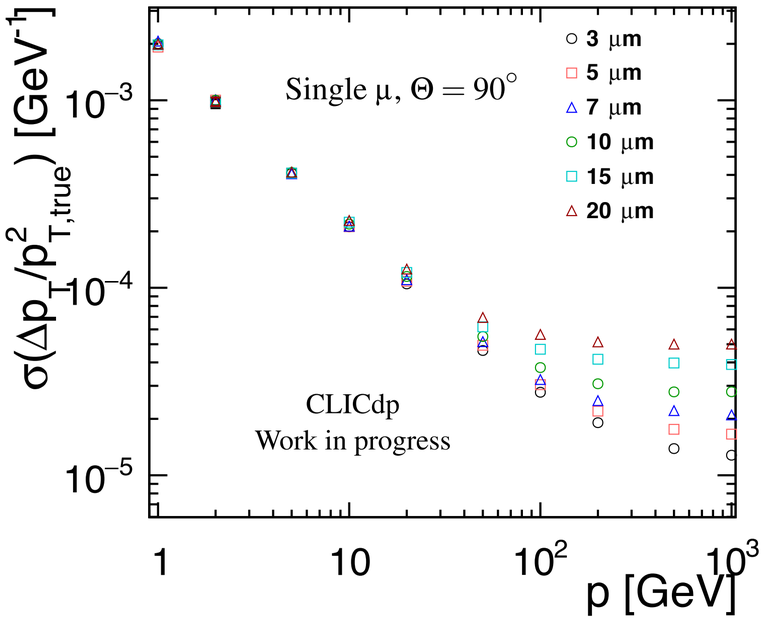


Tracker

- Large tracking volume proposed: area of silicon ~100 m^2, outer radius 1.5 metres, barrel length 2.5 metres

- Material budget for the tracker is 1-2 % X_0 per layer
  - Air cooling not feasible in such a large volume => water cooling
  - Power budget of 100-150 mW / cm^2
  - Momentum resolution of $\sigma_P / p_T^2 \sim 2 \times 10^{-5}$ GeV^{-1}
  - Single hit resolution of 7 μm in the bending plane

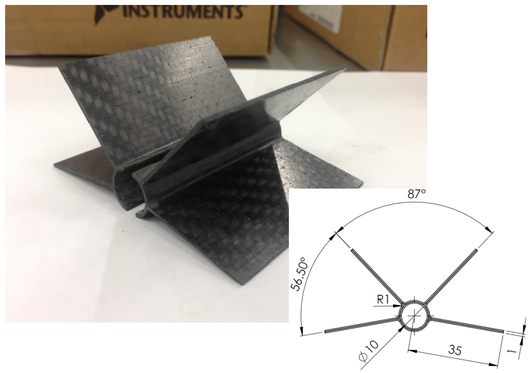
- Current technology baseline **monolithic CMOS**
  - Long pixels with maximum size of 30 μm × (1-10) mm
  - Sensor thickness of 200 μm

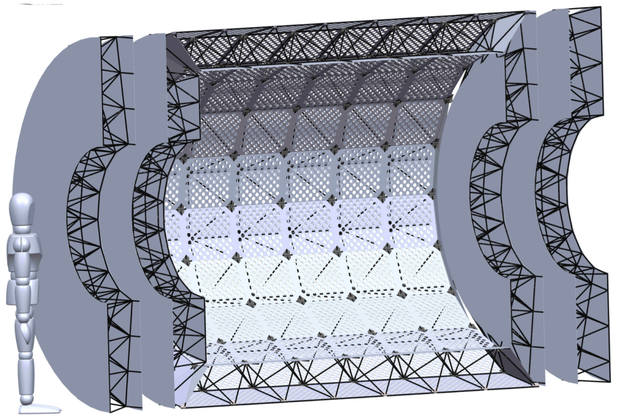


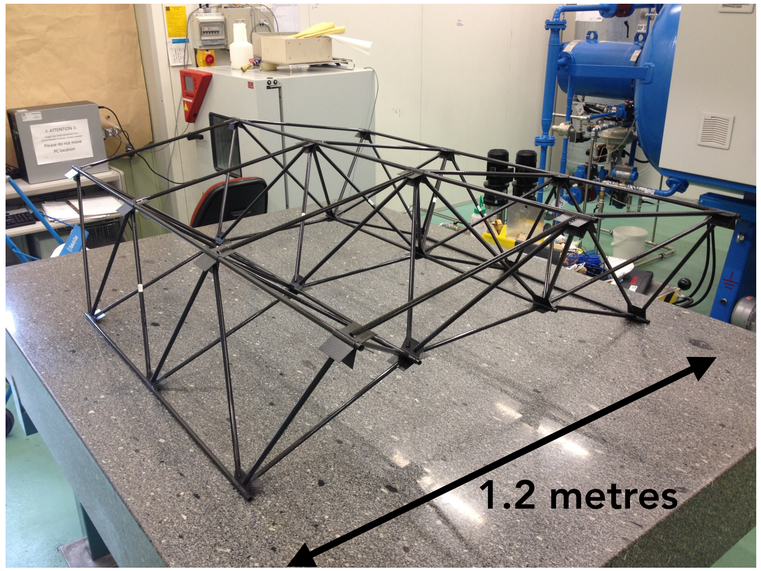
Tracker layout

- In a similar vein to the vertex detector, proof of concept prototyping to confirm material budget assumptions
  - Construction of a section of the barrel region, to compare finite element calculations with measurements
  - Connecting nodes developed and fabricated, off-the-shelf carbon fibre tubes connecting
  - Stiffness achieved with low mass structure, total weight 926 g (70 % tubes, 26 % nodes, 4 % glue)

- Simulation results for deformations give acceptable performance with total mass of the support structure of 0.125% X_0







Emerging silicon technologies

- In the last (~5) years many novel detectors have been designed taking advantage of recent commercially available CMOS processes
  - Plethora of new devices, many with only subtle differences, processes typically differ by Foundry and technology size…

- CLIC has been heavily involved in several of these areas, which are also of interest for high luminosity LHC upgrades, as well as more broadly to HEP and medical imaging

LEP era

=>

LHC era

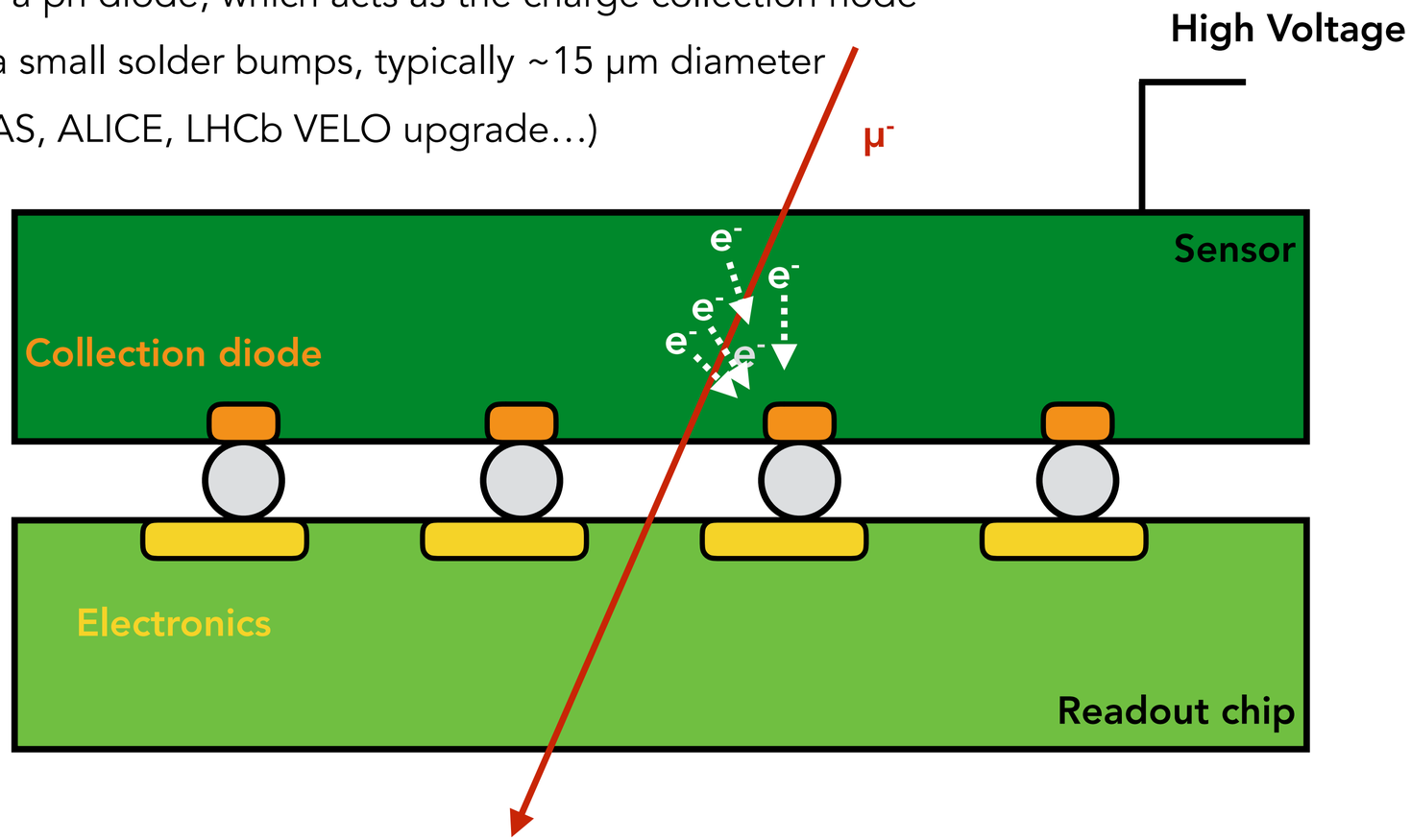
=>

HL-LHC-and-beyond era

Emerging silicon technologies

- **Conventional hybrid pixel detector**
  - Sensor (high resistivity) typically consists of a pn diode, which acts as the charge collection node
  - Readout chip (low resistivity) connected via small solder bumps, typically ~15 μm diameter
  - Widely used in particle physics (CMS, ATLAS, ALICE, LHCb VELO upgrade…)
  - Small cell sizes $\mathcal{O}$(50 - 250 μm)
  - Extensive functionality on-pixel

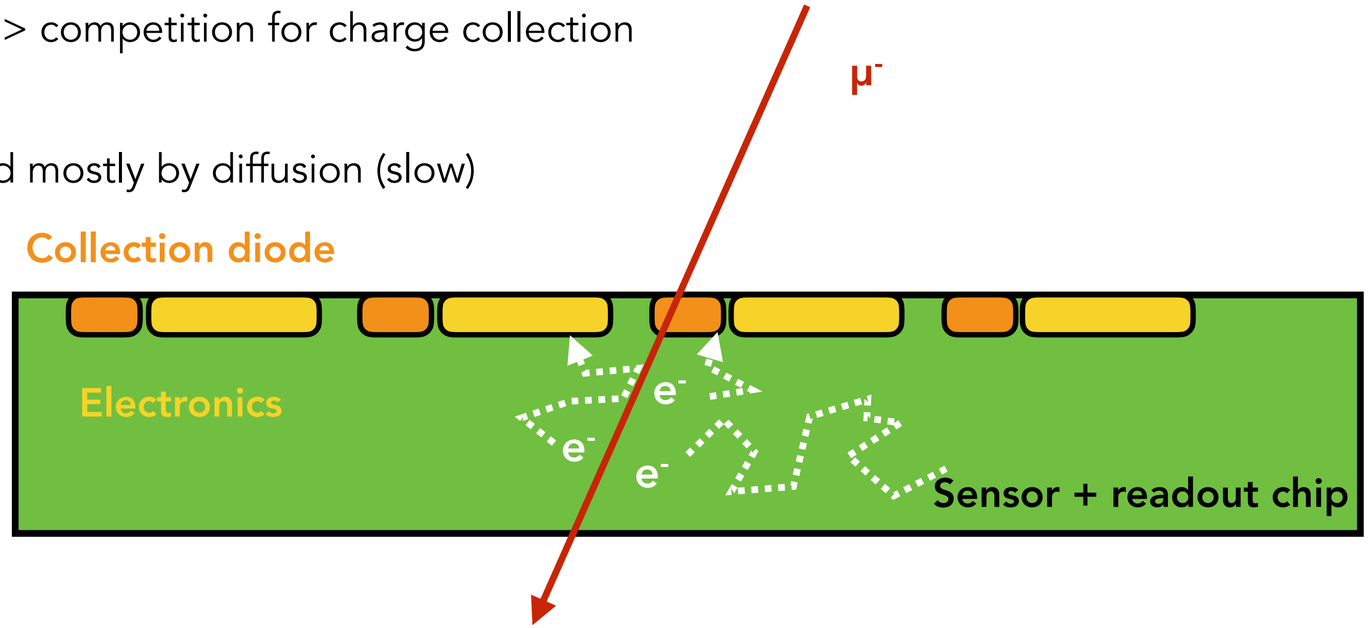
- But…
  - Bump bonding still costly
  - Limit on device thickness for stability
  - Currently limiting on pixel pitch



Emerging silicon technologies

- **Monolithic Active Pixel Sensors** - electronics and sensor are both deposited on silicon wafers, why not do both?
  - Integrated sensor + readout => lower mass, no bump-bonding
  - Widely used in digital cameras (check your smartphone!)

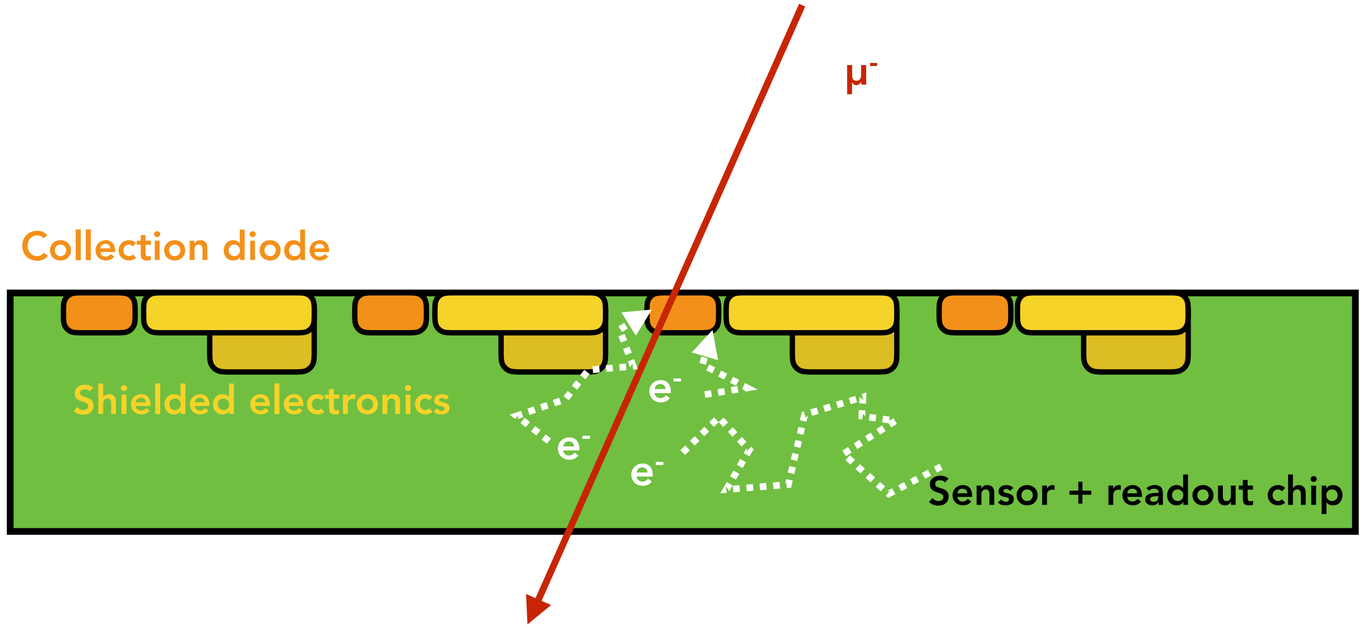
- What's the catch?
  - Electronics consist of n-wells and p-wells => competition for charge collection
  - Typically low on-pixel functionality
  - **Limited depleted region**, charge collected mostly by diffusion (slow)



Emerging silicon technologies

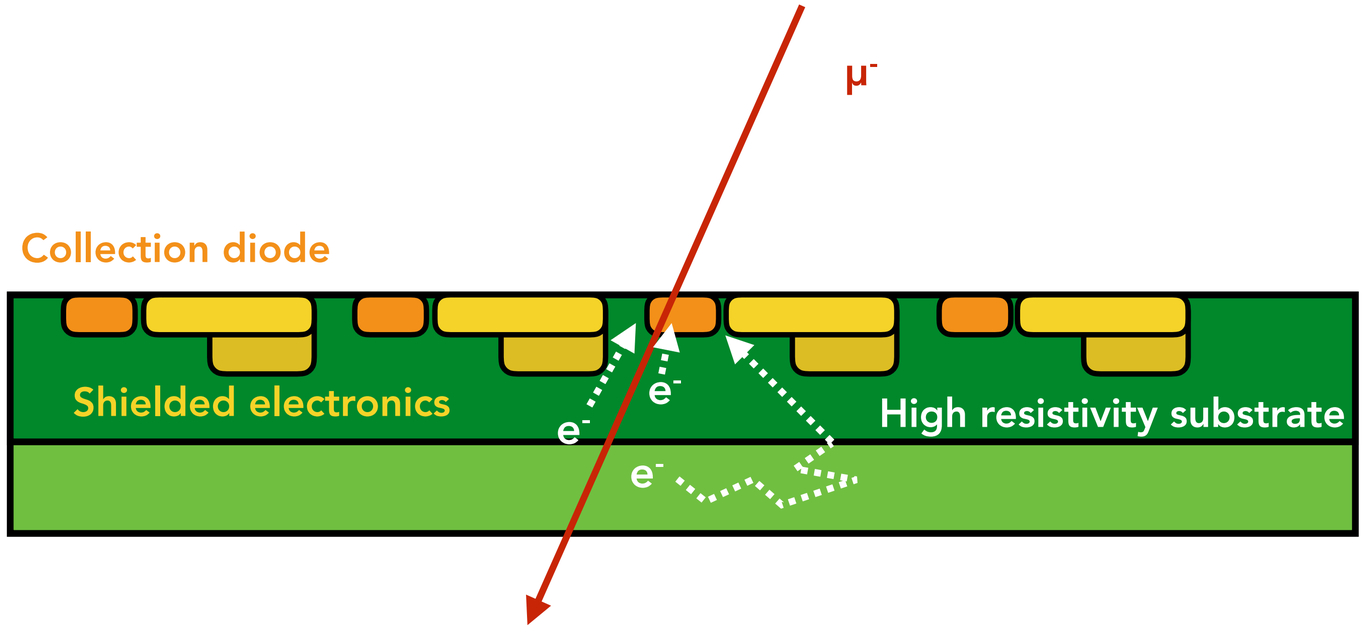
- What can we do better?
  - **Shield electronics in order to prevent charge being collected where you don't want it**

- But…
  - Charge collection still by diffusion



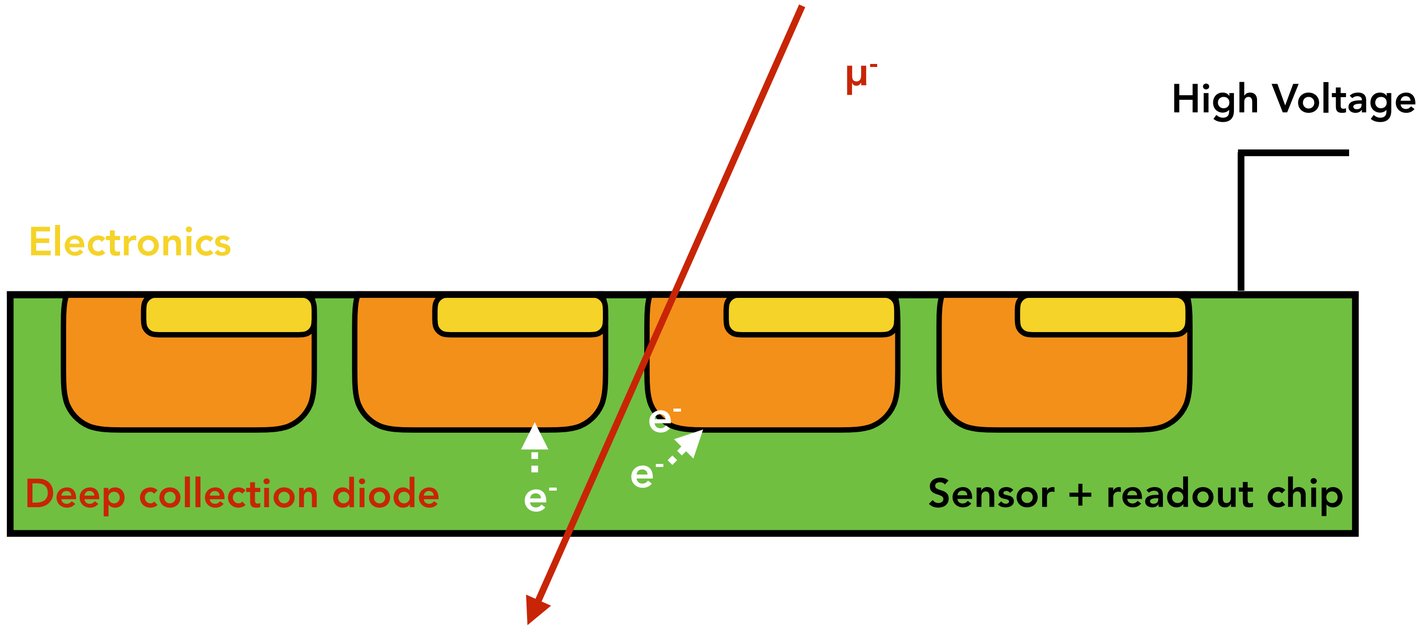
Emerging silicon technologies - **High Resistivity (HR) CMOS**

- What can we do better?
  - Shield electronics in order to prevent charge being collected where you don't want it
  - **Extend depletion region: use a high resistivity substrate to extend built-in depletion**



Emerging silicon technologies - **High Voltage (HV) CMOS**

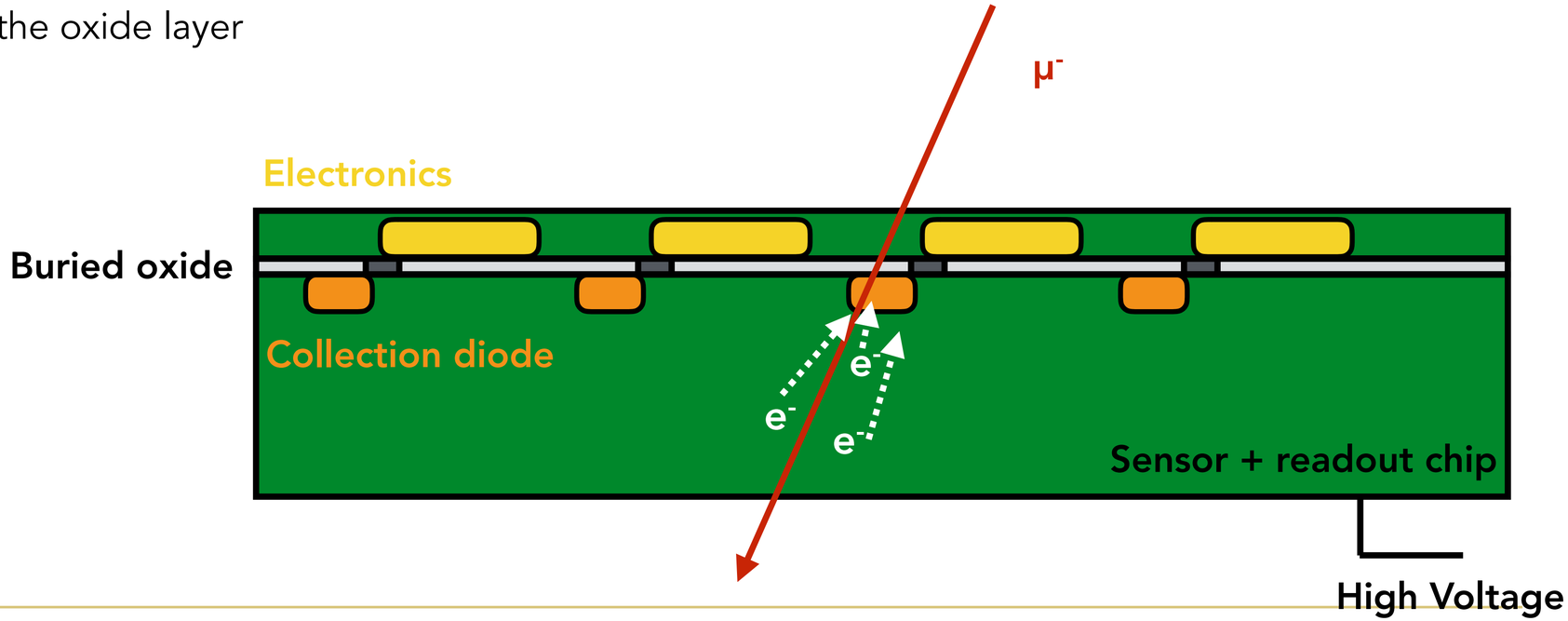
- What can we do better?
  - Shield electronics in order to prevent charge being collected where you don't want it
  - **Extend depletion region: apply a bias voltage**
  - Need to shield electronics from high electric field => move inside the collection diode. Allows a high voltage (~100 V) to be applied to the substrate



Emerging silicon technologies - **Silicon on Insulator (SOI)**

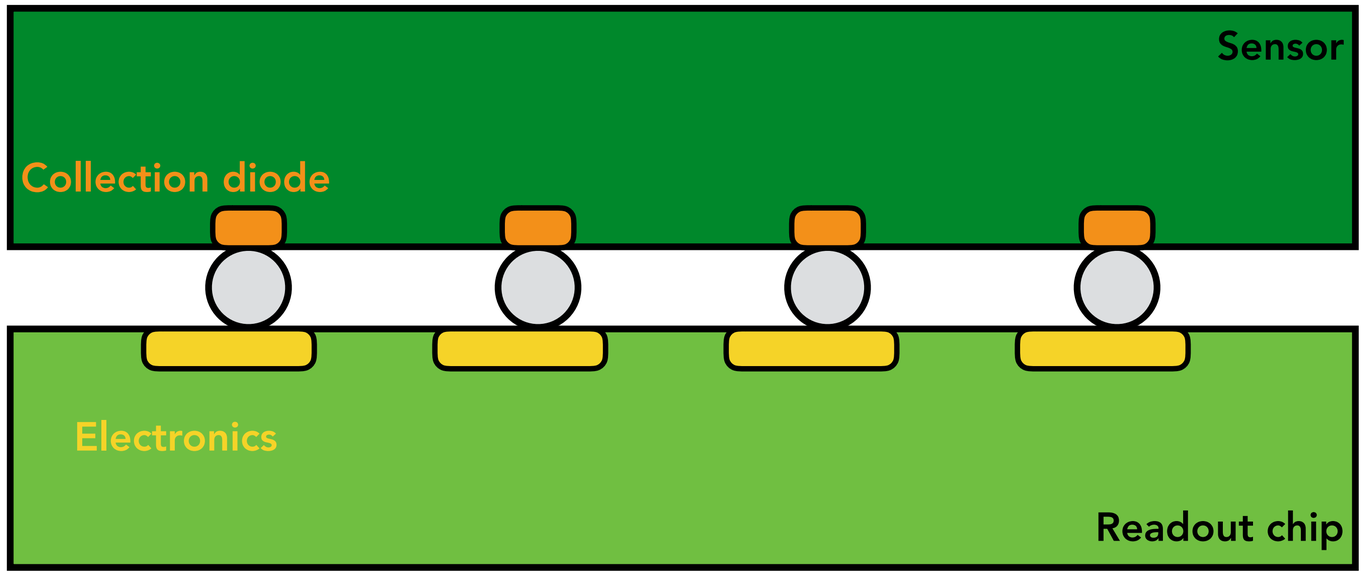
- Another approach to isolate the electronics and collection diode
  - **Readout electronics don't need much space - why not just separate two regions of the silicon?**

- Silicon oxide can be used as an insulation layer to prevent interference between the sensor and electronics
  - Full CMOS on the upper silicon layer, conventional planar silicon sensor underneath
  - Connection through ***vias*** in the oxide layer



Emerging silicon technologies

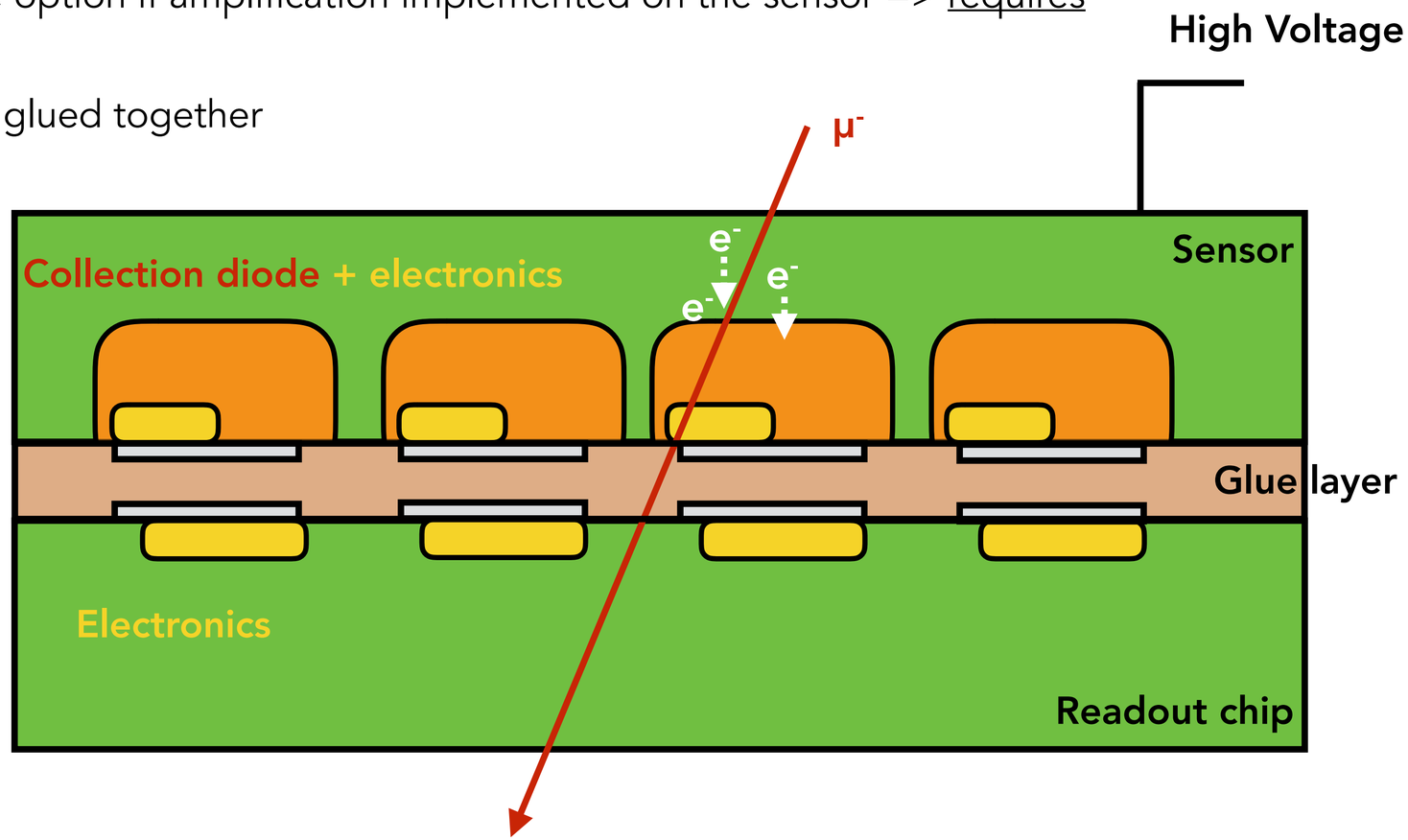
- Conventional hybrid pixel detectors still have advantages
  - Technology size can be much smaller (cf. 65 nm) than those available in integrated technologies (HR- or HV-CMOS)
  - Integrated devices still suffer from noise injected into the sensing diode - limit to on-pixel functionality possible



Emerging silicon technologies - **CCPD**

- **Another solution available: capacitive coupling of the sensor to the readout**
  - Given small pixel capacitance only a viable option if amplification implemented on the sensor => requires integrated technology (HR- or HV-CMOS)
  - Avoids bump-bonding, devices are simply glued together

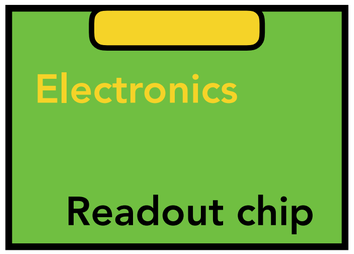
- **Capacitively Coupled Pixel Detectors**



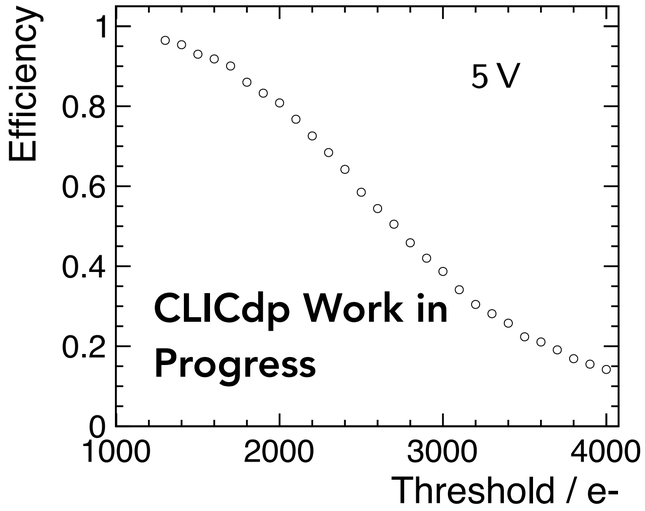
CLICpix

- Prototype readout chip for the CLIC vertex detector, for capacitively coupled HV-CMOS sensors and thin (50 µm) planar sensors
  - One of the first readout chips for HEP designed and produced in 65 nm
  - Providing feedback for high-luminosity LHC projects, RD53

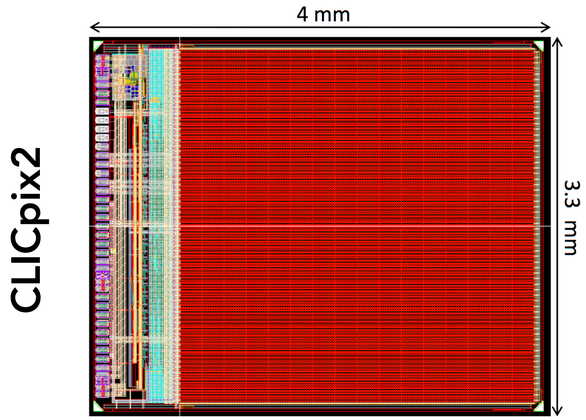
- Chip is an evolution of the Medipix/Timepix family of ASICs, with similar design
  - Amplifier + discriminator on each pixel, 25 µm × 25 µm pixels
  - In-pixel measurement of both charge and particle arrival time
  - Shuttered readout with power pulsing of the pixel matrix, to match the CLIC beam structure



- Many results produced with the current chip, improved design has recently been fabricated (results expected soon!)

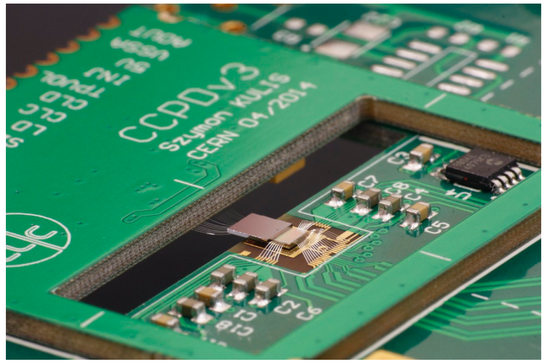


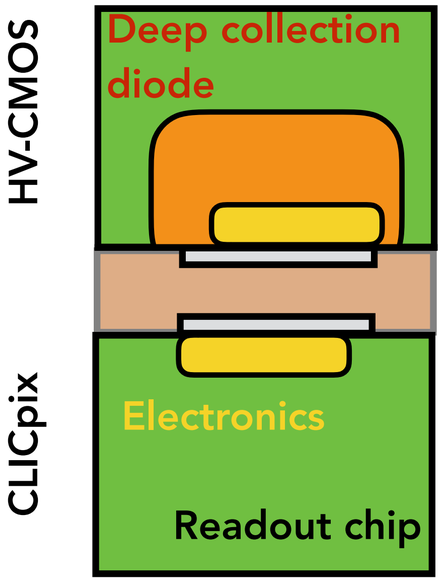
50 µm sensor on CLICpix



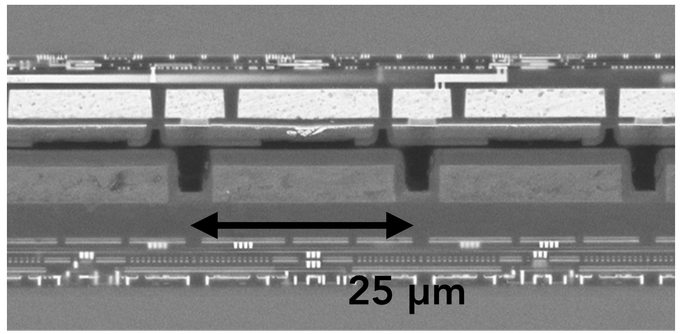
HV-CMOS sensors

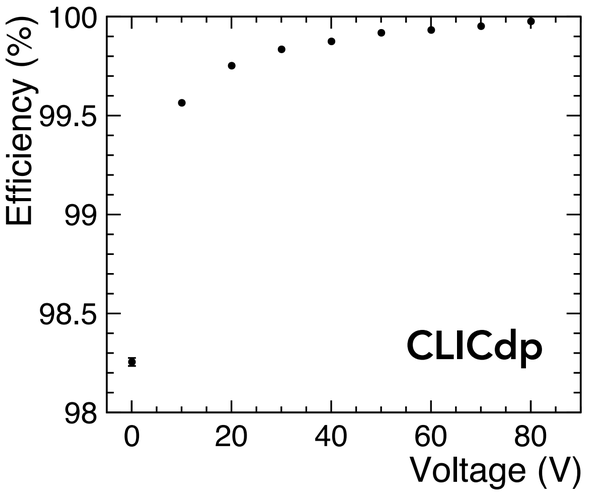
- In-depth studies of HV-CMOS devices have been carried out for CLIC, with knock-on contributions to high-luminosity LHC (ATLAS upgrade)
  - Proof-of-concept results on capacitively coupled pixel detectors showed high detection efficiency and reliable operation
  - Detailed fabrication studies carried out, for extrapolation to detector-scale production





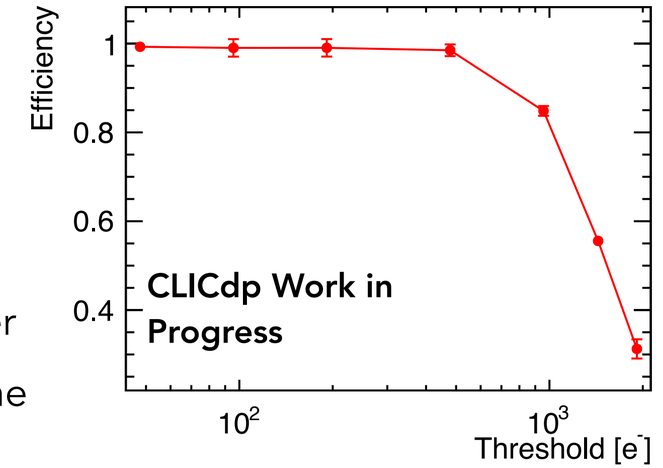
- Common chip development with ATLAS
  - CCPD family, one of the first HV-CMOS chips developed for HEP
  - New ASIC produced in collaboration with the Medipix group - C3PD

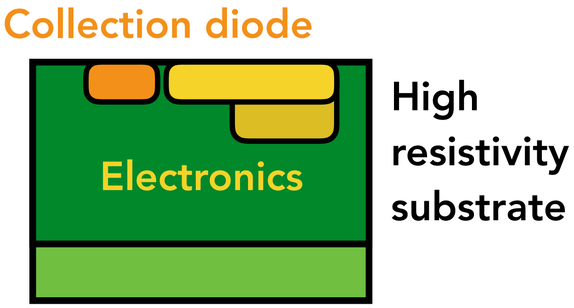


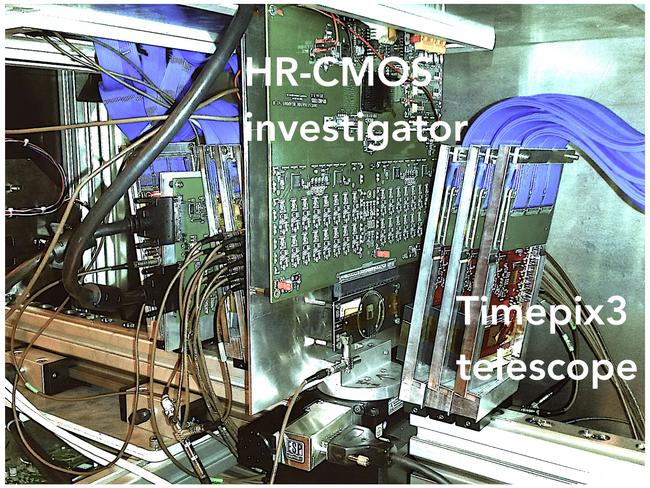


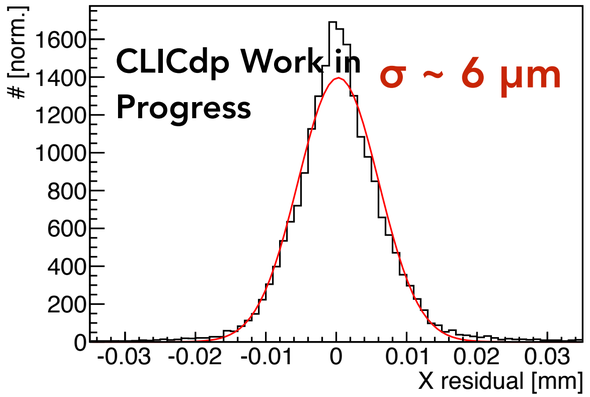
HR-CMOS

- Existing devices fabricated with HR-CMOS used as a test-bed for several experiments (ALICE, ATLAS upgrade)
  - Prototype chip does not yet contain full readout electronics - in-pixel amplifier is read out by an external ADC
  - Extensive measurement in lab and beam tests, backed up by simulation
  - Promising results have led to consideration of the technology for the CLIC tracker
  - Full chip layout with integrated readout being developed in collaboration with the Medipix group and ALICE



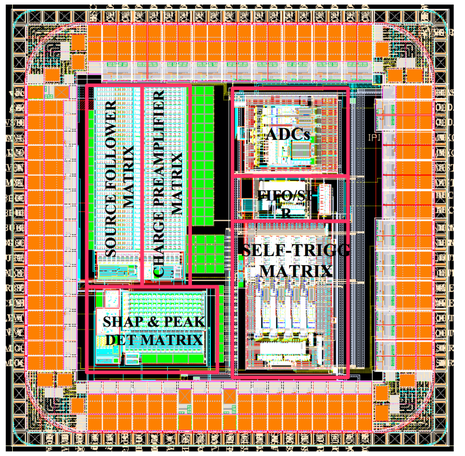


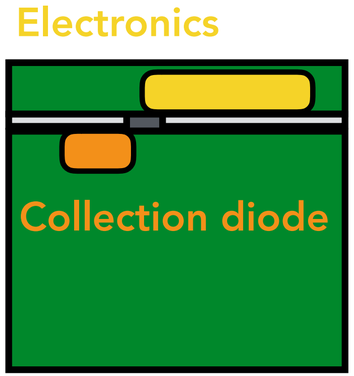




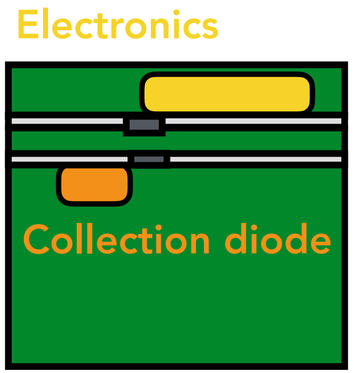
SOI

- SOI development ongoing in several groups worldwide
  - Assemblies have been produced to test several architectures (CLIC + more general HEP)
  - Different readout schemes, methods of in-pixel signal processing
  - Samples studied in testbeam at the SPS, analysis ongoing
  - Promising results, chips fully functional and good single hit resolution measured
  - Double SOI process also considered, for improved radiation tolerance

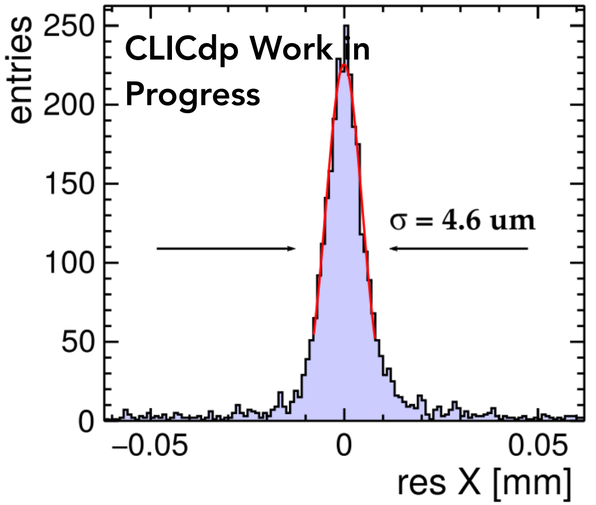




Buried oxide



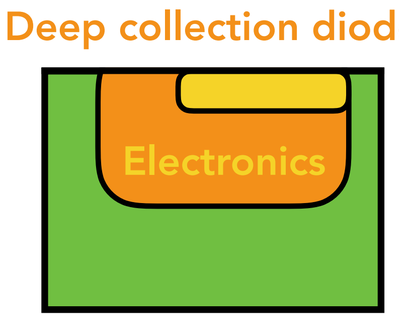
Buried oxide
2nd Buried oxide

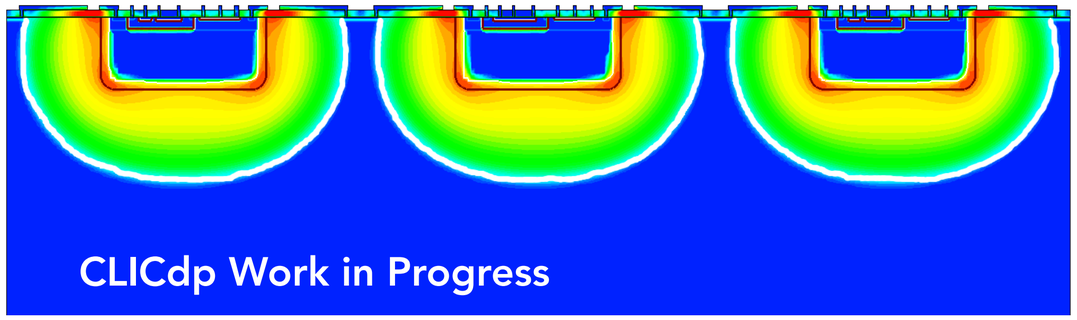


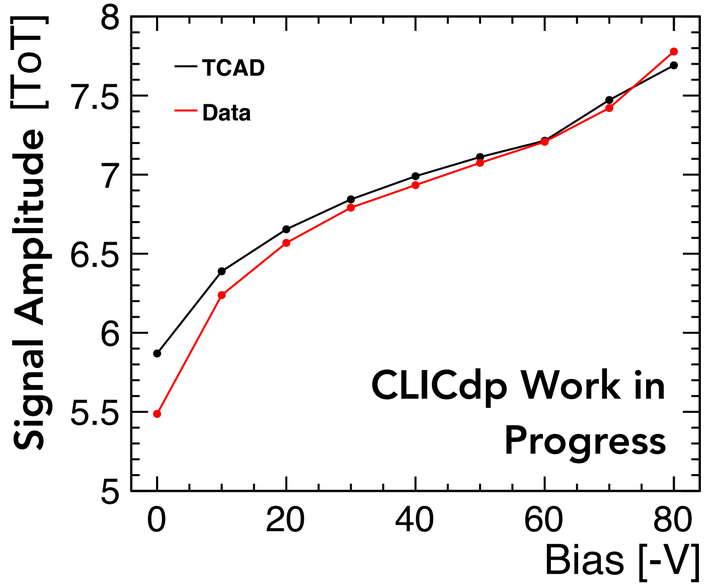
Simulations - TCAD

- Understanding of lab and beam measurements aided massively by TCAD finite element simulations
  - Ability to disentangle intrinsic sensor performance and electronics effects
  - Leakage current and breakdown points predicted well for implemented pixel geometry
  - Observed charge collection in HV-CMOS devices only accounted for with avalanche/charge multiplication models

- Results from simulation have fed into the design process for subsequent chips
  - Optimisation of the chip layout to improve breakdown characteristics
  - Additional submissions with higher resistivity substrates

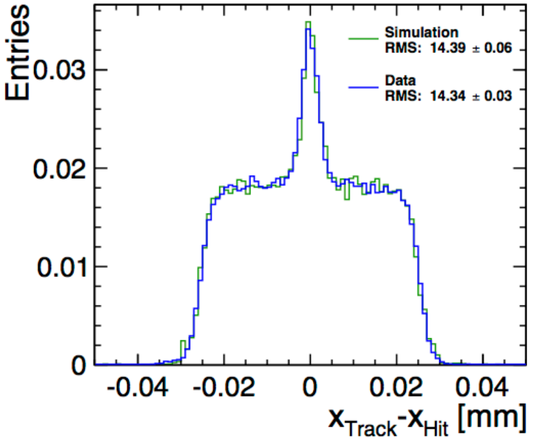


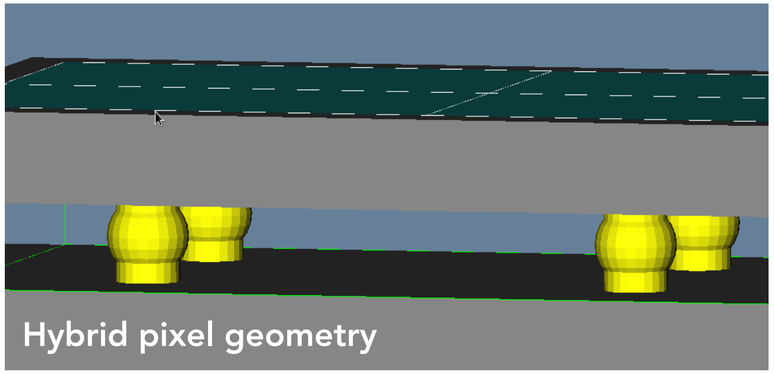


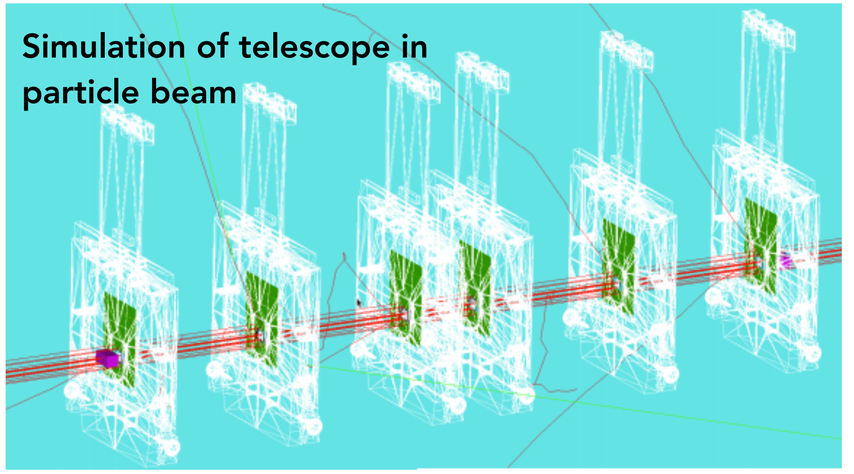


Simulations - Geant4

- In addition to TCAD, full Geant4-based simulations of detectors and set-ups have been developed as part of the CLICdp project
  - Contributions to open-source software suite **Allpix**, in use in several collaborations both inside and outside HEP
  - Provides a simple interface to produce commonly used detector geometries
  - Detailed simulation of electric field and magnetic field effects, charge carrier propagation
  - Currently being upgraded: watch out for allpix^2



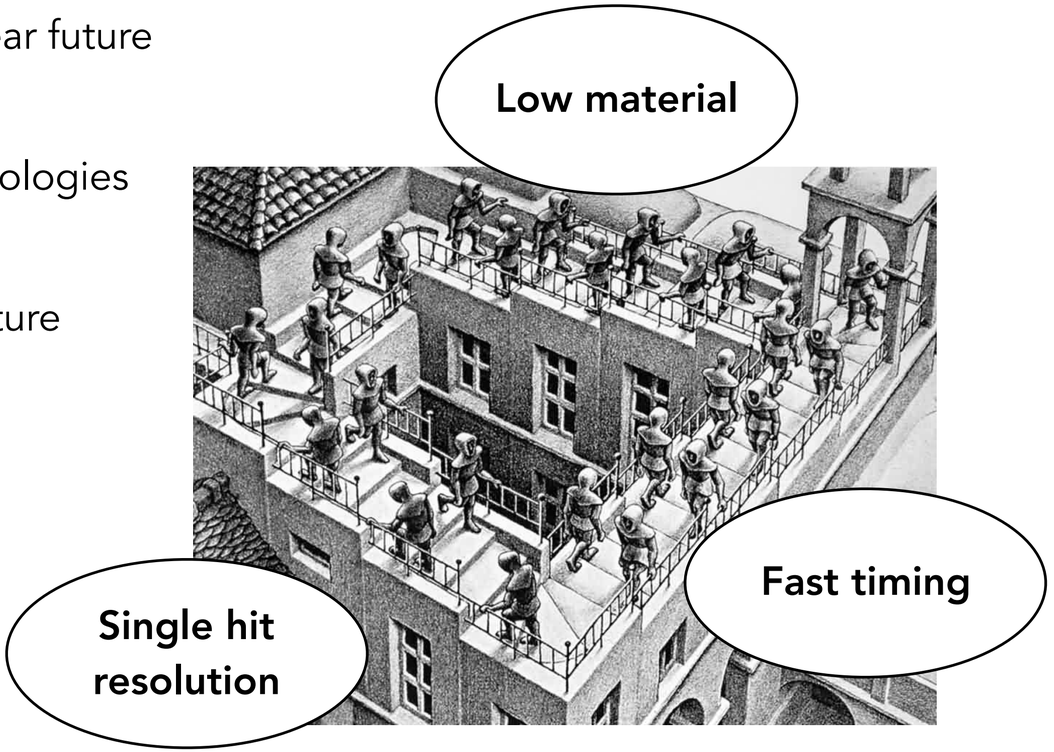

Hybrid pixel geometry



Future work

- Where are we now in terms of silicon?
  - Each of the requirements are achievable individually, trick is to reach all at once!
  - CLICpix with either HV-CMOS or planar silicon sensor getting close to vertex requirements
  - Dedicated monolithic chip for the tracker to be produced in the near future

- CLIC silicon R&D touches on many areas, helping to push new technologies
  - Overlap with HL-LHC detector upgrades
  - Keep a close eye on developments in CMOS processing for the future



Future work

- Where are we now in terms of silicon?
  - Each of the requirements are achievable individually, trick is to reach all at once!
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Thank you for your attention!