



An overview of CMOS sensor technologies for CLIC

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Overview

- Motivation

- The processes:
 - 180 nm HV-CMOS
 - 180 nm HR-CMOS

- Experience

- Design considerations

- Summary

- Future steps



Motivation

- Monolithic detectors can potentially offer:
 - Lower cost, as the bump bonding process is avoided
 - Low input capacitance → reduced power consumption for a given SNR and bandwidth

- Studied processes at CERN Microelectronics group:
 - 180 nm HV-CMOS process with deep n-well as collecting electrode
 - 180 nm HR-CMOS process with charge collection on epitaxial layer

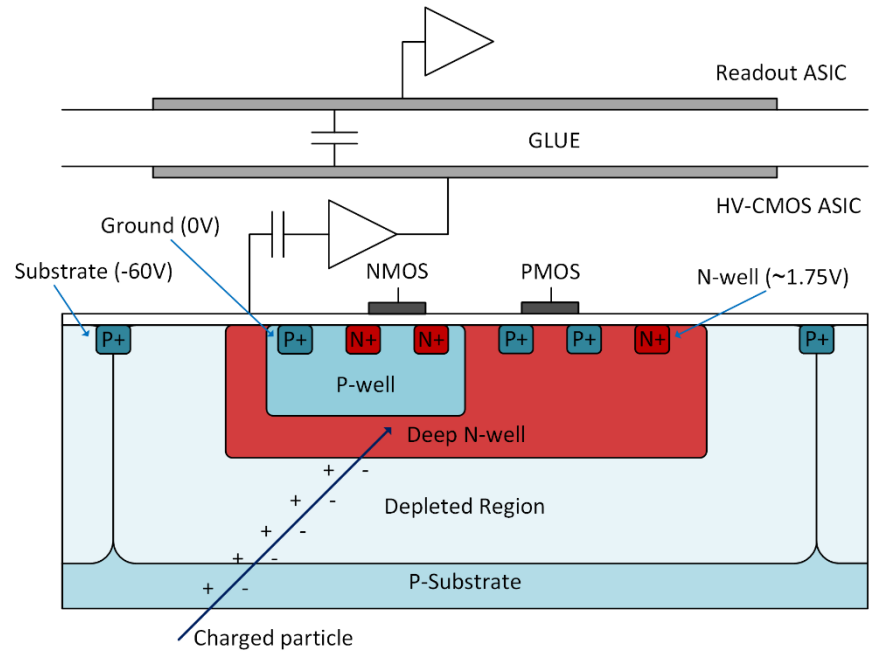
- The above-mentioned processes are being studied in the context of HEP applications:
 - CLIC vertex and tracking detector
 - Upgrade of the Inner Tracking System of the ALICE experiment
 - ATLAS Phase II Upgrade
 - and more...

- Requirements for a monolithic chip for the CLIC silicon tracker:
 - 7 μm single point resolution in one dimension
 - 1 – 10 mm strip length
 - Energy measurement with approximately 5 bit precision
 - 10 ns time slicing, with a counter depth of approximately 8 bit
 - Silicon thickness $\leq 200 \mu\text{m}$
 - Power consumption $< 150 \text{ mW/cm}^2$ (after power pulsing)

The processes – 180 nm HV-CMOS

- 180 nm HV-CMOS process with deep n-well as collecting diode
 - Every P+ diffusion is capacitively coupled to the n-well, which is also the sensor's cathode
 - Therefore, all PMOS devices can be a source of noise injection to the sensor

- Experience using this process: HV-CMOS sensor chips designed to be capacitively coupled with CLICpix/CLICpix2 readout chips
 - CCPDv3 (I. Peric)
 - C3PD

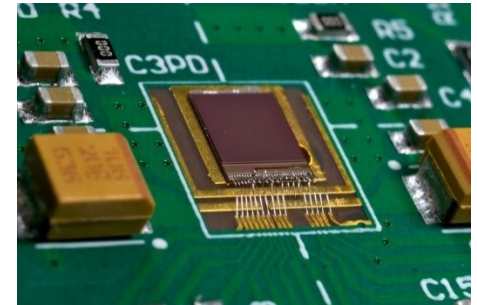
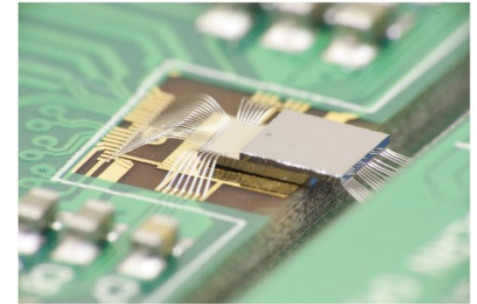


Experience with 180 nm HV-CMOS process

- CCPDv3 (I. Peric): Starting point for studying this concept and process
 - 64x64 square pixels with 25 μm pitch
 - Tested with CLICpix readout chip [1]

- C3PD: Architectural changes implemented in order to minimize power consumption and to improve speed
 - 128x128 square pixels with 25 μm pitch
 - Stand-alone test performed
 - Standard (250 μm) and thinned-down (50 μm) samples have been successfully tested
 - To be tested with CLICpix2 readout chip
 - 1st submission: standard resistivity for the substrate ($\sim 20 \Omega\text{cm}$)
 - 2nd submission: 20/80/200 Ωcm substrate resistivity (Samples to be received in the coming months)

- Main limitation by design:
 - Every PMOS device is capacitively coupled to the sensor
 - For the case of C3PD the number of PMOS devices used has been minimized, resulting to a minimum coupling to the sensor
 - But in order to have a monolithic device, fully complementary circuitry is necessary (digital CMOS devices)
 - Different ways have been studied in order to overcome this problem [2]
 - Complications added at system level

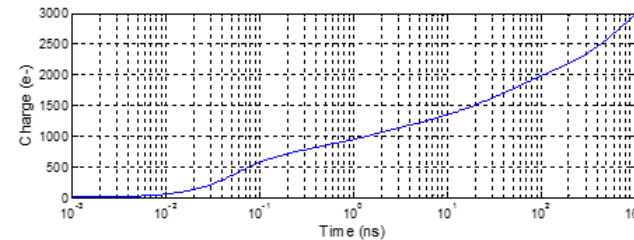
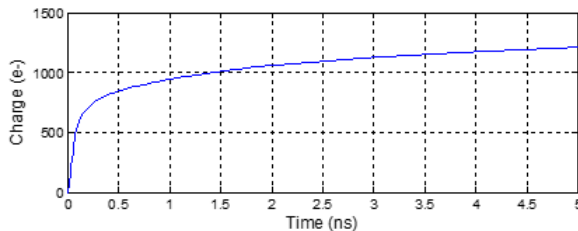
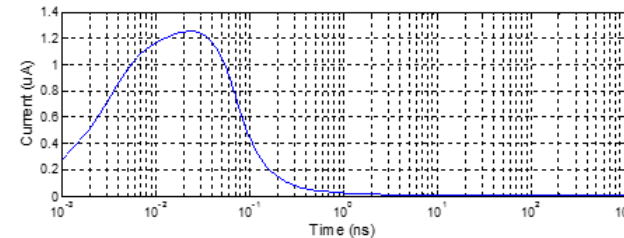
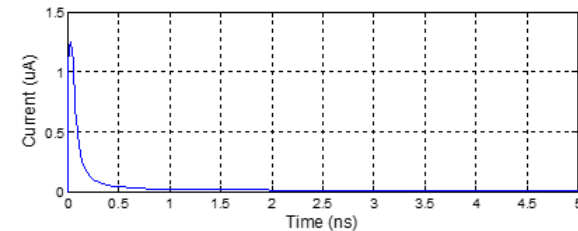
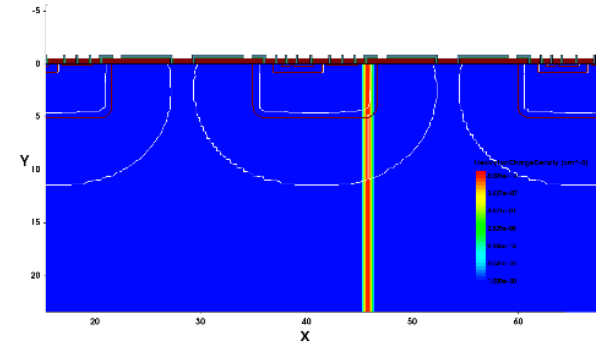


Photos: S. Kulis

Experience with 180 nm HV-CMOS process

- According to TCAD simulations [3], the expected depletion depth would be $\sim 10 - 15 \mu\text{m}$
 - For the standard substrate resistivity, and a reverse bias of -60 V

- Deposited charge for a MIP varies from 2900 to 3700 e^- (depending on position of the hit)
 - Fast component, collected by drift, followed by a slow component, which is collected by diffusion



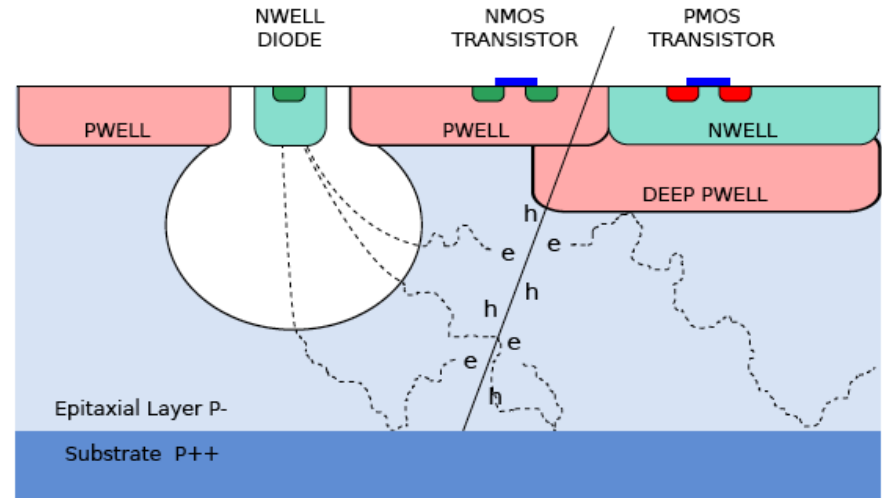
Simulations: M. Buckland

The processes – 180 nm HR-CMOS

- 180 nm CMOS process with charge collection on epitaxial layer
 - Small n-well as collecting electrode
 - Small input capacitance
 - Circuits placed in a deep p-well, separated from collecting electrode
 - PMOS devices can therefore be used with this technology without being coupled to the sensor
 - CMOS digital logic is possible to be implemented in this process

- High resistivity epitaxial layer (1 – 8 kΩcm)
 - 15 – 40 μm thickness

- Experience using the process:
 - ALICE Investigator chip
 - ALICE ALPIDE chip



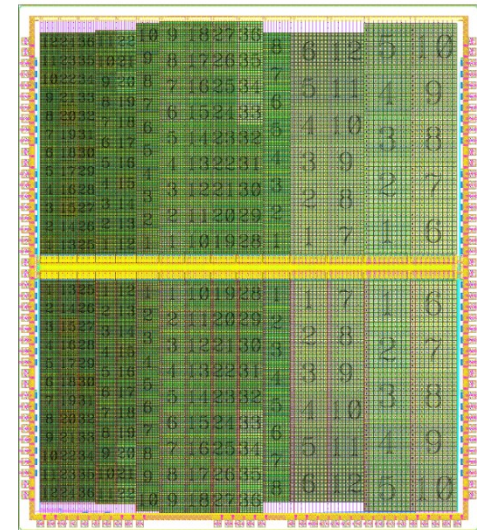
W. Snoeys et al.

- The ALICE Investigator chip [4]:

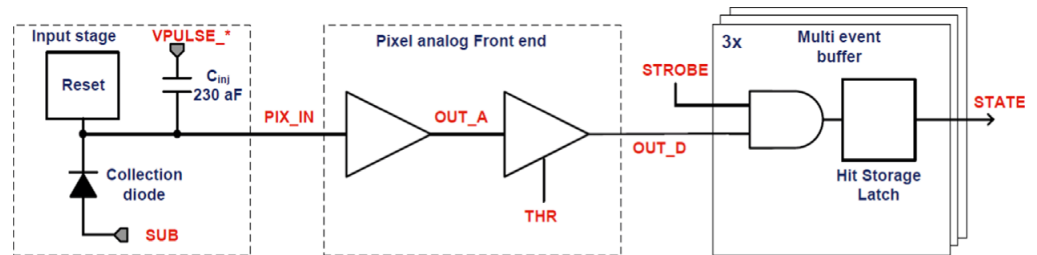
- 2x134 mini-matrices with different pixel pitch (20 – 50 μm) and collecting diode geometries
- Analog-only signal monitoring (direct readout)
- To serve as a research vehicle to better understand the technology potentials

- The ALICE ALPIDE chip [5]

- A monolithic active pixel sensor chip designed for the upgrade of the ALICE ITS
- Samples thinned down to 50 μm have been tested
- Analog front-end power consumption: $\sim 40 \text{ nW/pixel}$
 - For 2 μs peaking time
- Capacitance of the sensing diode: $\sim 2.5 \text{ fF}$ [5]
- Fully monolithic pixel (pixel size: $\sim 30 \times 30 \mu\text{m}^2$), comprising:
 - Sensing diode
 - Front-end amplifier
 - Comparator
 - Digital logic



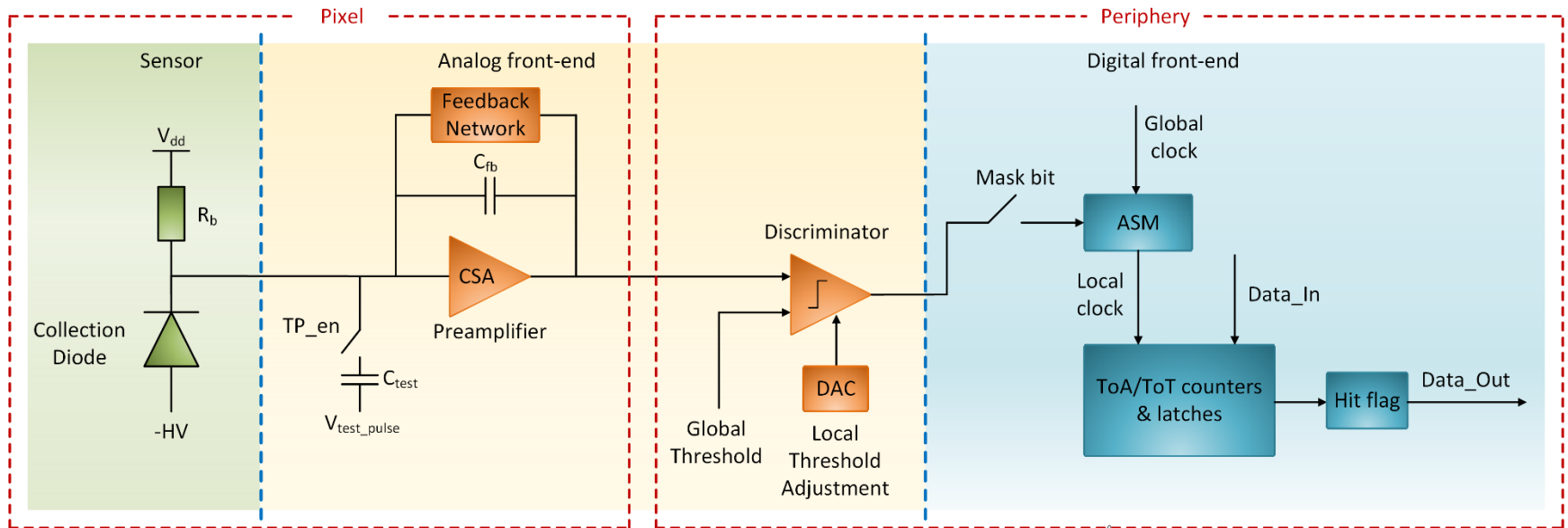
Investigator chip



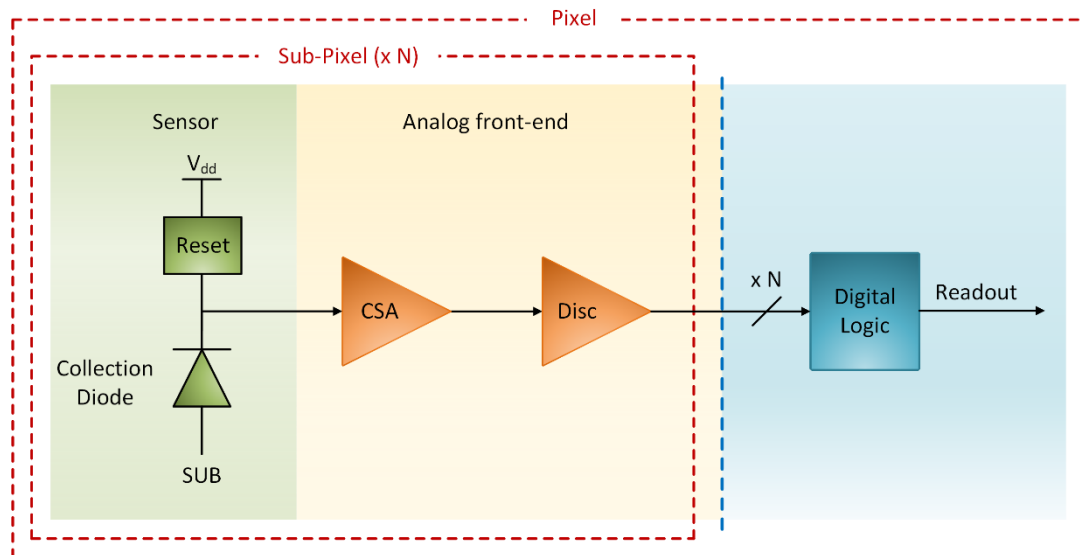
Block diagram of the ALPIDE pixel

Design considerations – 180 nm HV-CMOS

- For the HV-CMOS implementation:
 - Only the charge sensitive amplifier may be placed in the pixel, as a way to avoid unwanted noise injection
 - Discriminator and digital logic are placed in the periphery (end-of-column) so that the coupling from the PMOS devices to the sensor is avoided
 - An implementation similar to *MuPix* chip [2], where each pixel in the matrix corresponds to a digital pixel in the periphery



- For the HR-CMOS implementation
 - The pixel can be segmented into sub-pixels (for example measuring $\sim 30 * 30 \mu m^2$), each one including a collecting diode and analog front-end
 - The reason for this is that for longer pixels the charge collection is expected to become slower
 - Charge collection as a function of the pixel pitch to be studied
 - The output of each preamplifier is discriminated. Discriminated signals can be combined in order to extract the timing and energy information required for the long pixel
 - Digital logic can be shared among all sub-pixels





Process summary

	HV-CMOS	HR-CMOS
Technology node	180 nm	180 nm
Supply voltage	1.8 V	1.8 V
Applied bias	-60 V	6 V
Collecting electrode	Large deep n-well including PMOS devices	Small n-well isolated from electronics (use of deep p-well)
Isolated PMOS devices	No	Yes
Substrate resistivity	~20 Ωcm	1 – 8 k Ωcm (for epitaxial layer)
Depleted region thickness	~10 μm (simulated)	~10 μm (simulated)



Summary

- 180 nm HV-CMOS process:
 - N-well including the PMOS devices is also the sensor's cathode
 - Noise injection to the sensor can occur by using CMOS circuitry
 - Complicated to isolate digital from analog domain and sensor while keeping the detection efficiency close to 100%
 - Large collecting electrode → larger depleted volume, but also larger detector capacitance
 - Deep n-well to p-well junction capacitance also adds a significant contribution to the sensor capacitance [6]
 - A larger sensor capacitance indicates a higher analog power consumption for a given SNR & bandwidth [7]:
 - For a given SNR and bandwidth: $P \sim \left\{ \frac{C}{Q} \right\}^m, 2 \leq m \leq 4$
 - $m \sim 2$ in weak inversion
 - $m \sim 4$ in strong inversion

- 180 nm HR-CMOS process with high resistivity epitaxial layer:
 - Collecting n-well isolated from electronics → Possible to use CMOS circuitry and separate power domains
 - Smaller collecting electrode → smaller detector capacitance
 - In the case of designing longer pixels, one solution would be to segment the long pixel into sub-pixels, and thus having multiple collecting diodes, with multiple front-ends [8]



Future steps

- Characterisation of C3PD samples with higher substrate resistivity
 - Layout was modified in order to achieve a higher breakdown voltage
 - Larger depletion depth is expected thanks to higher substrate resistivity
 - Samples are expected to be received and tested in the coming months

- Design of a monolithic chip for the CLIC tracker
 - Requirements:
 - 7 μm single point resolution in one dimension
 - 1 – 10 mm strip length
 - Energy measurement with approximately 5 bit precision
 - 10 ns time slicing, with a counter depth of approximately 8 bit
 - Silicon thickness $\leq 200 \mu\text{m}$
 - Power consumption $< 150 \text{ mW/cm}^2$ (After power pulsing)
 - Study and design of basic building blocks is on-going
 - As presented above, the 180 nm HR-CMOS process is more optimised for this application
 - Design effort is therefore focused on this process



References

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